

IPC-6013E

Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards

Developed by the Flexible Circuits Specifications Subcommittee (D-12) of the Flexible Circuits Committee (D-10) of IPC

Supersedes:

IPC-6013D September 2017 IPC-6013D Amendment 1 April 2018 Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

Tel 847 615.7100 Fax 847 615.7105

Table of Contents

1 SC	OPE 1	3.2.1	Laminates and Bonding Materials	7
1.1	Statement of Scope	3.2.2	External Bonding Materials	7
1.2	Purpose	3.2.3	Other Dielectric Materials	7
1.3	Performance Classification, Board Type,	3.2.4	Metal Foils	7
	and Installation Usage	3.2.5	Metal Planes/Cores	8
1.3.1	Classification	3.2.6	Base Metallic Plating Depositions and	
1.3.2	Printed Board Type		Conductive Coatings	8
1.3.3	Installation Uses	3.2.7	Final Finish Depositions and Coatings -	0
1.3.4	Selection for Procurement	2.2.0	Metallic and Non-Metallic	
1.3.5	Material, Plating Process and Final Finish 2	3.2.8	Polymer Coating (Solder Mask)	
1.4	Terms and Definitions	3.2.9	Fusing Fluids and Fluxes.	
1.4.1	As Agreed Upon Between User and	3.2.10	Marking Inks	
	Supplier (AABUS)	3.2.11	Hole Fill Insulation Material	
1.4.2	Button Plating	3.2.12	Heatsink Planes, External	
1.4.3	Cover Material	3.2.13	Via Protection	
1.4.4	Target Land (Via Bottom Land) 4	3.2.14	Embedded Passive Materials	
1.4.5	Capture Land (Via Top Land)4	3.3	Visual Examination	. 13
1.4.6	Microvia	3.3.1	Profile	. 13
1.4.7	Core	3.3.2	Construction Imperfections	. 14
1.4.8	Design Data 4	3.3.3	Plating and Coating Voids in the Hole	. 18
1.5	Interpretation 4	3.3.4	Lifted Lands	. 18
1.6	Presentation 4	3.3.5	Marking	. 18
1.7	Design Data Protection	3.3.6	Solderability	. 19
1.8	Revision Level Changes 5	3.3.7	Plating Adhesion	. 20
	PLICABLE DOCUMENTS5	3.3.8	Edge Board Contact, Junction of Gold Plate to Solder Finish	. 20
2.1	IPC5	3.3.9	Strain Relief (Rigid to Flex Transition)	
2.2	Joint Industry Standards 6	3.3.10	Workmanship	
2.3	Other Publications 6	3.4	Dimensional Requirements	
2.3.1	American Society for Testing and Materials 6	3.4.1	Hole Size, Hole Pattern Accuracy and	0
2.3.2	Underwriters Lab 6	01111	Pattern Feature Accuracy	. 20
2.3.3	National Electrical Manufacturers Association6	3.4.2	Annular Ring and Breakout (External)	. 21
2.3.4	American Society for Quality	3.4.3	Bow and Twist (Individual Rigid or Stiffener	
2.3.5	AMS7		Portions Only)	. 24
2.3.6	American Society of Mechanical Engineers 7	3.4.4	Array Sub-Pallets.	. 25
2.3.7	Federal7	3.5	Conductor Definition	. 25
3 RE	QUIREMENTS7	3.5.1	Conductor Width and Thickness	. 25
3.1	General	3.5.2	Conductor Spacing	. 25
3.2	Materials Used in this Specification	3.5.3	Conductor Imperfections	. 25

3.5.4	Conductive Surfaces	3.12	Rev	work
3.6	Structural Integrity	4 QUA	LITY	Y ASSURANCE PROVISIONS
3.6.1	Thermal Stress Testing	4.1		neral
3.6.2	Requirements for Microsectioned Coupons	4.1.1	Qua	alification
	or Production Boards	4.1.2	San	nple Test Coupons
3.7	Solder Mask Requirements	4.2	Acc	ceptance Testing and Frequency
3.7.1	Solder Mask Coverage	4.2.1		O Zero Acceptance Number Sampling Plan 52
3.7.2	Solder Mask Cure and Adhesion47	4.2.2		Feree Tests
3.7.3	Solder Mask Thickness	4.3		ality Conformance Testing
3.8	Electrical Requirements	4.3.1		upon Selection
3.8.1	Dielectric Withstanding Voltage 47	E NOT		59
3.8.2	Electrical Continuity and Isolation Resistance 48	5.1		
3.8.3	Circuit/PTH Shorts to Metal Substrates 48			lering Data
3.8.4	Moisture and Insulation Resistance (MIR) 48	5.2	Sup	perseded Specifications
3.9	Cleanliness	APPEN	DIX A	A
3.9.1	Cleanliness Prior to Solder Mask Application 48			Figures
3.9.2	Cleanliness After Solder Mask, Solder, or Alternative Surface Coating Application 48	Figure 3	8-1A	Transition Zone14
3.9.3	Cleanliness of Inner Layers After Oxide	Figure 3	8-1B	Transition Zone
	Treatment Prior to Lamination	Figure 3	3-2	Unacceptable Cover Material Coverage16
3.10	Special Requirements	Figure 3	3-3	Solder Wicking and Plating Penetration18
3.10.1	Outgassing	Figure 3	8-4a	Annular Ring Measurement (External)
3.10.2	Fungus Resistance			for PTHs
3.10.3	Vibration	Figure 3	8-4b	Annular Ring Measurement (External)
3.10.4	Mechanical Shock	E. 0		for Unsupported Holes
3.10.5	Impedance Testing	Figure 3		Breakout of 90° and 180°
3.10.6	Coefficient of Thermal Expansion (CTE)49	Figure 3		Conductor Width Reduction
3.10.7	Thermal Shock	Figure 3	5-'/	Major and Minor Access Holes for Flexible Printed Boards
3.10.8	Surface Insulation Resistance (As Received) 49	Figure 3	8-8	Squeeze-Out of Cover Film Adhesive
3.10.9	Metal Core (Horizontal Microsection) 50	8		and Ooze-Out of Covercoat24
3.10.10	Ionic (Resistivity of Solvent Extract) 50	Figure 3	3-9	Missing material or skips in the bead of
3.10.11	Rework Simulation 50			adhesive squeeze-out at coverlay edges 24
3.10.12	Bending Test 50	Figure 3	3-10	Unnecessary Copper Between Conductor and Nodule of Conductor
3.10.13	Flexible Endurance 50	Figure 3	2 11	Isolated Reductions of
3.10.14	Bond Strength (Unsupported Lands) 51	rigure)-11	Conductor Thickness
3.10.15	Bond Strength (Stiffener)	Figure 3	3-12	Rectangular Surface Mount Lands
3.10.16	Destructive Physical Analysis 51	Figure 3	3-13	Round Surface Mount Lands
3.10.17	Design Data Protection	•		Printed Board Edge Connector Lands 27
3.10.18	Performance Based Testing for Microvia	•		Plated Hole Microsection
	Structures – Structural Integrity During Thermal Stress	-		(Grinding/Polishing) Tolerance 30
3.11	Repair	Figure 3	3-16	An Example of Plating to Target Land
3.11.1	Circuit Repair			Separation
3.11.1	Circuit Kepaii			

	Separation at External Foil	Figure 3-45	Exclusion of Separations in Microvia Target Land Contact Dimension43
_	Copper Crack Definition	Figure 2 16	Unintended Piercing of Microvia Target
Figure 3-19	Examples of Thermal Zones for Microsection Evaluation of Laminate Attributes	rigule 3-40	Land (Laser Drilled)
Figure 3-20	Measurement for Etchback	Figure 3-47	Intentional Piercing of Microvia Target Land (Mechanically Drilled2)
Figure 3-21	Measurement for Dielectric Removal 34	Figure 3-48	Measurement of Total Copper
Figure 3-22	Smear Removal Allowance	1 iguic 3-40	Thickness When Selective Hole
Figure 3-23	Measurement Locations for Fluoropolymer		Plating is Specified
	Resin Smear	Figure 3-49	Metal Core to PTH
	Negative Etchback	Figure 3-50	Measurement of Minimum
Figure 3-25	Plating Folds/Inclusions – Minimum		Dielectric Spacing
	Measurement Points	Figure 3-51	Fill Material in Blind/Through Vias When Cap Plating Not Specified
Figure 3-26	Annular Ring Measurement (Internal) 37	Figure 2.52	Void in Fill Material at
Figure 3-27	Microsection Rotations for	rigure 3-32	Hole Wall Interface
E: 2.20	Breakout Detection	Figure 3-53	Bending Test
•	Comparison of Microsection Rotations 38	Č	
Figure 3-29	Example of Non-Conforming Dielectric Spacing Reduction Due to Breakout at		Tables
	Microvia Target Land	Table 1-1	Default Requirements
Figure 3-30	Surface Copper Wrap Measurement for	Table 3-1	Internal or External Metal Planes 8
	Filled Holes (Over Foil)	Table 3-2	Final Finish, Plating and Coating Requirements
Figure 3-31	Surface Copper Wrap Measurement for	Table 3-3	Surface7 and Hole Copper Plating Minimum
E: 2.22	Filled Holes (Over Laminate)	14016 3-3	Requirements for Through-Holes11
_	Wrap Copper (Acceptable)	Table 3-4	Hole Copper Plating Minimum
Figure 3-33	Wrap Copper Removed by Excessive Processing, e.g. Sanding/Planarization/		Requirements for Buried Vias > 2 Layers,
	Etching (Not Acceptable)		and Blind Vias11
Figure 3-34	Copper Cap Thickness	Table 3-5	Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)12
Figure 3-35	Copper Cap Filled Via Height (Bump) 41	Table 3-6	Hole Copper Plating Minimum Requirements
Figure 3-36	Copper Cap Depression (Dimple) 41	1aoic 3-0	for Buried via cores (2 layers)
Figure 3-37	Copper Cap Plating Voids	Table 3-7	Covercoat Adhesion
Figure 3-38	Nonconforming Via fill Between Copper Cap Plating Layers	Table 3-8	Solder Wicking / Plating Penetration Limits
Figure 3-39	Acceptable Via Fill Between Copper Cap	Table 3-9	Plating and Coating Voids
S	Plating Layers	14010 5 7	Visual Examination
Figure 3-40	Example of Acceptable Voiding in a Cap	Table 3-10	Edge Board Contact Gap20
	Plated, Copper Filled Via	Table 3-11	Minimum Etch Annular Ring
Figure 3-41	Example of Acceptable Voiding in a Copper Filled Microvia without Cap Plating 42	Table 3-12	Allowable Squeeze-Out of Coverlay Adhesive and Ooze-Out of Covercoat 24
Figure 3-42	Example of Nonconforming Void in a Cap Plated, Copper Filled Microvia	Table 3-13	Minimum Solderable Annular Ring on
Figure 3-43	Example of Nonconforming Void in a	Table 3-14	Land Area
	Copper Filled Microvia		
Figure 3-44	Microvia Contact Dimension	Table 3-15	PTH Integrity After Stress31

IPC-6013E September 2021

Table 3-16	Cap Plating Requirements
Table 3-17	Microvia Contact Dimension (Laser Drilled)
Table 3-18	Microvia Contact Dimension (Mechanically Drilled)
Table 3-19	Internal Layer Foil Thickness after Processing
Table 3-20	Thickness of External Conductor of the Finished Printed Board after Plating 45
Table 3-21	Solder Mask Adhesion
Table 3-22	Dielectric Withstanding Test Voltages 48
Table 3-23	Insulation Resistance
Table 4-1	Qualification Testing
Table 4-2	C=0 Sampling Plan per Lot Size55
Table 4-3	Acceptance Testing and Frequency55
Table 4-4	Quality Conformance Testing59

September 2021 IPC-6013E

Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards

1 SCOPE

1.1 Statement of Scope This specification covers qualification and performance requirements of flexible printed boards. The flexible printed board may be single-sided, double-sided, multilayer, or rigid-flex multilayer. All of these constructions may or may not include stiffeners, plated-through holes (PTHs), and blind/buried vias.

The flexible or rigid-flex printed board may contain build up High Density Interconnect (HDI) layers. The printed board may contain embedded active or passive circuitry with distributive capacitive planes, capacitive or resistive components conforming to IPC-6017.

The rigid section of the printed board may contain a metal core or external metal heat frame, which may be active or nonactive. Revision level changes are described in 1.7.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of flexible printed boards designed to IPC-2221 and IPC-2223.

1.3 Performance Classification, Board Type, and Installation Usage

- **1.3.1 Classification** This specification recognizes that flexible printed boards will be subject to variations in performance requirements based on end-use. These performance classes (Class 1, Class 2, and Class 3) are defined in IPC-6011.
- **1.3.2 Printed Board Type** Performance requirements are established for the different types of flexible printed boards, classified as follows:
- Type 1 Single-sided flexible printed boards containing one conductive layer, with or without stiffeners.
- Type 2 Double-sided flexible printed boards containing two conductive layers with PTHs, with or without stiffeners.
- Type 3 Multilayer flexible printed boards containing three or more conductive layers with PTHs, with or without stiffeners.
- Type 4 Multilayer rigid and flexible material combinations containing three or more conductive layers with PTHs.
- Type 5 Flexible or rigid-flex printed boards containing two or more conductive layers without PTHs.

1.3.3 Installation Uses

- *Use A* Capable of withstanding flex during installation.
- Use B Capable of withstanding continuous flexing for the number of cycles as specified on the procurement documentation.
- *Use C* High temperature environment (over 105 °C [221 °F]).
- Use D UL Recognition. See UL 94 and UL 796F.
- **1.3.4 Selection for Procurement** For procurement purposes, performance class and installation usage **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that the supplier can fabricate the flexible printed boards and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

Note: If the drawing specifies the requirement in words, designators are not required.

The procurement documentation **shall** specify the thermal stress test method and the number of cycles (in relation to reflow profiles in IPC-TM-650, Method 2.6.27) to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.2, 3.6.1.3 and 3.6.1.4. If not specified (see 5.1), the default **shall** be per Table 1-1.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

- Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1)
- Conventional SnPb reflow processes (see 3.6.1.2)
- Lead-free reflow processes (see 3.6.1.3 and 3.6.1.4)

IPC-6013E September 2021

IPC-6016, a sectional performance specification for HDI printed boards, was canceled by the IPC. Relevant HDI conformance and acceptance criteria has been transferred to this revision of this specification.

The addition of IPC-2221 Appendix A conformance coupons (beginning with Revision B of the design standard) by the printed board manufacturer to the manufacturing panel **shall** be AABUS.

1.3.4.1 Selection (Default) The procurement documentation **shall** specify those requirements that are a result of the selection process within this specification. This includes all references to "AABUS". If the requirement selection is not made in accordance with the procurement documentation, Ordering Data (see 5.1), Customer Drawing and/or supplier control plan (SCP), then the default requirements in Table 1-1 **shall** apply.

Table 1-1 Default Requirements

Category	Default Selection
Performance Class	Class 2
Installation Usage	Use A
Material	Fabricator defined
Final Finish	Finish X (Electrodeposited tin lead, fused or solder coated) or alternate Finish ENIG allowed on designs (drawings) with Initial Release on or after January 01, 2021.
Minimum Starting Foil	1/2 oz. for all internal and external layers. For plated HDI layers – ¼ oz. for all layers (internal or external)
Copper Foil Type	Fabricator defined
Plated Component Hole Diameter Tolerance	(±) 100 μm [3,937 μin]
Plated Via Hole Diameter Tolerance	(+) 80 μm [3,150 μin], (-) no requirement, (may be totally or partially plugged)
Non-plated Hole Diameter Tolerance	(±) 80 μm [3,150 μin]
Conductor Width tolerance	Class 2 requirements per para. 3.5.1
Conductor Spacing tolerance	Class 2 requirements per para. 3.5.2
Dielectric Separation	Minimum rigid dielectric spacing shall be 90 μ m [3,543 μ in]. Minimum flexible dielectric spacing shall be within 20% of the selected thickness
Lateral Conductor Spacing	100 μm [3,937 μin] minimum
Marking Ink	Contrasting color, nonconductive
Solder Mask	Not applied, if not specified
Solder Mask, specified	Class T of IPC-SM-840 if class not specified
Solderability Test	Per 3.3.6, Category 2 for SnPb and Category A for Pb-free of J-STD-003
Test Voltage, Isolation Resistance	Per IPC-9252
Qualification not specified	See IPC-6011
Profile tolerance	0.5 mm [0.0197 in] for all external edges
Thermal Stress Test	IPC-TM-650, Method 2.6.8, Condition A or, if utilizing polyester flexible material, Condition C per 3.6.1

1.3.5 Material, Plating Process and Final Finish

- **1.3.5.1** Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.
- **1.3.5.2 Plating Process** The copper plating process used to provide the main conductor in the holes is identified by a single number as follows:
- 1) Acid copper electroplating only
- 2) Pyrophosphate copper electroplating only
- 3) Acid and/or pyrophosphate copper electroplating