



IPC-2226A

# **Sectional Design Standard for High Density Interconnect (HDI) Printed Boards**

Developed by the IPC-2221/2222 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

***Supersedes:***  
IPC-2226 - April 2003

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

# Table of Contents

<b>1 SCOPE</b> .....	1	4.4.1 Embedded Resistors .....	12
1.1 Purpose .....	1	4.4.2 Embedded Capacitors .....	12
1.2 Document Hierarchy .....	1	4.4.3 Embedded Inductors .....	12
1.3 Presentation .....	1	4.5 HDI in Flexible Printed Boards .....	12
1.4 Interpretation .....	1	<b>5 MECHANICAL/PHYSICAL PROPERTIES</b> .....	13
1.5 Classification of HDI Types .....	1	5.1 HDI Feature Size .....	13
1.5.1 Core Types .....	1	5.1.1 Minimum Hole Sizes for PTH Vias .....	14
1.5.2 HDI Types .....	1	5.2 Construction Types .....	14
1.6 Producibility Level .....	1	5.2.1 HDI Type I Constructions – 1[C]0 or 1[C]1 ...	14
1.7 Via Formation .....	2	5.2.2 HDI Type II Constructions – 1[C]0 or 1[C]1 ...	15
1.8 Design Features .....	2	5.2.3 HDI Type III Constructions – $\geq 2[C] \geq 0$ .....	16
<b>2 APPLICABLE DOCUMENTS</b> .....	2	5.2.4 HDI Type IV Constructions – $\geq 1 [P] \geq 0$ .....	18
2.1 IPC .....	2	5.2.5 Type V Constructions (Coreless) – Using Layer Pairs .....	18
<b>3 GENERAL REQUIREMENTS</b> .....	3	5.2.6 Type VI Constructions .....	19
3.1 Terms and Definitions .....	3	<b>6 ELECTRICAL PROPERTIES</b> .....	19
3.1.1 Microvia .....	3	<b>7 THERMAL MANAGEMENT</b> .....	19
3.1.2 Capture Land (Via Top Land) .....	3	7.1 Thermal Management Concerns for Bump Interconnects on HDI .....	21
3.1.3 Target Land (Via Bottom Land) .....	3	7.1.1 Junction to Case Thermal Models .....	22
3.1.4 Stacked Microvias .....	3	7.2 Thermal Flow Management Through HDI Substrate .....	23
3.1.5 Staggered Microvias .....	3	<b>8 COMPONENT AND ASSEMBLY ISSUES</b> .....	25
3.1.6 Variable Depth Microvia .....	4	8.1 General Attachment Requirements .....	25
3.2 Design Tradeoffs .....	4	8.1.1 Flip Chip Design Considerations .....	25
3.3 Design Layout .....	4	8.2 Test Point Spacing (Electrical Test) .....	25
3.3.1 Design Considerations .....	5	<b>9 HOLES/INTERCONNECTIONS</b> .....	26
3.4 Density Evaluation .....	5	9.1 Microvias .....	26
3.4.1 Routability Prediction Methods .....	5	9.1.1 Microvia Formation .....	26
3.4.2 Design Basics .....	6	9.2 Via Interconnect Variations .....	29
3.4.3 HDI Routing Density Factors .....	7	9.2.1 Stacked Microvias .....	29
<b>4 MATERIALS</b> .....	10	9.2.2 Stacked Vias .....	29
4.1 Material Selection .....	10	9.2.3 Staggered Vias .....	29
4.1.1 Reinforced Material Considerations .....	10	9.2.4 Variable Depth Vias/Microvias .....	30
4.1.2 Non-Reinforced Material Considerations .....	10	<b>10 GENERAL CIRCUIT FEATURE REQUIREMENTS</b> .....	30
4.2 Material Description by Type .....	10	10.1 Conductor Characteristics .....	30
4.2.1 Dielectric Materials .....	10	10.1.1 Balanced Conductors .....	30
4.2.2 Materials for Conductive Paths (In-Plane or Inter-Plane) .....	11	10.2 Land Characteristics .....	30
4.2.3 Materials with Dielectric and Conductive Functionality .....	11	10.3 Via and Land Density .....	30
4.3 Copper Foil .....	11		
4.4 Embedded Electronic Components .....	12		

10.3	Trade Off Process .....	31
10.3.1	Wiring Factor Process .....	31
10.3.2	Input/Output (I/O) Variables .....	32
<b>11</b>	<b>DOCUMENTATION .....</b>	<b>32</b>
<b>12</b>	<b>QUALITY ASSURANCE .....</b>	<b>32</b>

### Figures

Figure 1-1	Color Key .....	2
Figure 3-1	Microvia Definition .....	3
Figure 3-2	Capture and Target Land (Microvia) .....	3
Figure 3-3	Staggered Via .....	3
Figure 3-4	Staggered Microvias .....	3
Figure 3-5	Variable Depth Microvias .....	4
Figure 3-6	Feature Pitch and Feature Size Defining Channel Width .....	6
Figure 3-7	Feature Pitch and Conductor per Channel Combinations .....	7
Figure 3-8	Electromagnetic Field Effect of a Signal Conductor .....	8
Figure 3-9	Example of Feasibility Study of Where Components are Dispersed .....	9
Figure 3-10	Example Placement of Voltage and Ground Planes .....	9
Figure 3-11	Routing and Via Grid for BGA package (100 PIN, 0.8 mm pitch example) .....	10
Figure 5-1	Type I HDI Construction .....	15
Figure 5-2	Type II HDI Construction .....	15
Figure 5-3	Type III HDI Construction .....	16
Figure 5-4	Type III HDI Construction with Stacked Microvias .....	17
Figure 5-5	Type III HDI with Staggered Microvias .....	17
Figure 5-6	Type III HDI with Variable Depth Blind Vias ...	18
Figure 5-7	Type IV HDI Construction .....	18
Figure 5-8	Coreless Type V HDI Construction .....	19
Figure 5-9	Type VI Construction .....	19
Figure 7-1	HDI Thermal Path Relationships .....	20
Figure 7-2	Thermal Management of Chip Scale and Flip Chip Parts Mounted on HDI .....	21
Figure 7-3	Bump Interconnect Equivalent Model .....	21

Figure 7-4	Wire Bond Example .....	22
Figure 7-5	Approximate Thermal Model for Wire Bond ....	22
Figure 7-6	Flip Chip Example .....	22
Figure 7-7	Approximate Thermal Model for Flip Chip .....	23
Figure 7-8	Chip Underfill Example .....	23
Figure 7-9	Approximate Thermal Model for Chip Underfill .....	23
Figure 7-10	Thermal Paste Example .....	23
Figure 7-11	Approximate Thermal Model for Thermal Paste .....	23
Figure 7-12	Thermal Resistance .....	24
Figure 7-13	Parallel Resistances .....	24
Figure 7-14	Metallic Thermal Properties .....	25
Figure 8-1	Flip Chip Connection .....	25
Figure 9-1	Summary of the Manufacturing Processes for PIDs, Laser, and Plasma Methods of Via Generation .....	27
Figure 9-2	Microvia Manufacturing Processes .....	27
Figure 9-3	Cross-Sectional Views of Methods to Make HDI with Microvias .....	28
Figure 9-4	Examples of Commercially Produced PID Boards .....	28
Figure 9-5	HDI Boards that Employ Conductive Pastes as Vias .....	29
Figure 9-6	Stacked Microvias .....	29
Figure 9-7	Stacked Vias .....	29
Figure 9-8	Staggered Microvias .....	30
Figure 9-9	Isometric View of Staggered Vias .....	30
Figure 9-10	Variable Depth Vias/Microvias .....	30
Figure 10-1	Wiring Process Flow Chart .....	31

### Tables

Table 3-1	PCB Design/Performance Tradeoff Checklist .....	4
Table 5-1	Typical Feature Sizes for HDI Construction .....	13
Table 5-2	Recommended Minimum Drill Hole Size .....	14
Table 7-1	Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip) .....	21
Table 7-2	Typical Bump (150 $\mu$ m) Thermal Resistance Multilayer Metal Chips .....	21
Table 9-1	Annular Rings (Minimum) .....	26

# Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

## 1 SCOPE

This standard establishes requirements and considerations for the design of organic and inorganic high density interconnect (HDI) printed boards and structures for component mounting and interconnections.

**1.1 Purpose** The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of IPC-2221. In addition, when the core material reflects requirements identified in the sectional standards (IPC-2222, IPC-2223, and IPC-2225), that information becomes a mandatory part of this standard.

The standard provides recommendations for signal, power, ground, and mixed distribution layers, dielectric separation, via formation and metallization requirements and other design features that are necessary for HDI substrates.

**1.2 Document Hierarchy** Document hierarchy **shall** be in accordance with the generic standard IPC-2221.

**1.3 Presentation** All dimensions and tolerances in this standard are represented in SI (metric) units with Imperial units following as a hard conversion for reference only (e.g., 0.01 cm [0.0039 in]). In instances of metric based components, dimensions in this standard are represented in SI (metric) units only to prevent an accumulation of errors in rounding with Imperial units. When using predominately metric components, IPC highly recommends doing design layout in a metric environment.

**1.4 Interpretation** Interpretation **shall** be in accordance with the generic standard IPC-2221.

**1.5 Classification of HDI Types** Classification **shall** be by category in accordance with the requirements based on end use and as stated in 1.5.1 and 1.5.2 of this standard.

**1.5.1 Core Types** When HDI products utilize core interconnections, the core type(s) and their materials **shall** be in accordance with IPC-2222 for rigid and IPC-2223 for flexible core interconnections. For passive or constraining core boards the materials **shall** be in accordance with IPC-2221.

**1.5.2 HDI Types** The design designation system of this standard recognizes the six industry approved design types (see 5.2) used in the manufacture of HDI printed boards. The designations in this section determine the HDI design type by defining the number and location of HDI layers that may or may not be combined with a substrate (core [C] or passive [P]).

For instance, an HDI printed board with two layers of HDI on one side of the core and one layer of HDI on the other side of the core would be 2 [C] 1.

The following definitions apply to all forms of HDI. **Blind vias may exist in all types.**

**TYPE I** 1 [C] 0 or 1 [C] 1 – with through vias connecting the outer layers (see 5.2.1).

**TYPE II** 1 [C] 0 or 1 [C] 1 – with buried vias in the core and may have through vias connecting the outer layers (see 5.2.2).

**TYPE III**  $\geq 2$  [C]  $\geq 0$  – may have buried vias in the core and may have through vias connecting the outer layers (see 5.2.3).

**TYPE IV**  $\geq 1$  [P]  $\geq 0$  – where P is a passive substrate with no electrical connection (see 5.2.4).

**TYPE V** Coreless constructions using layer pairs (see 5.2.5).

**TYPE VI** Alternate constructions (see 5.2.6).

**1.6 Producibility Level** When appropriate, this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are: