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Amendment 1

Qualification and Performance Specification for Rigid Printed Boards

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A standard developed by IPC

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1249
Tel. 847.615.7100 Fax 847.615.7105
www.ipc.org

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- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

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Qualification and Performance Specification for Rigid Printed Boards

2 APPLICABLE DOCUMENTS

Append the following to 2.1 IPC:

IPC-4553 Specification for Immersion Silver Plating for Printed Circuit Boards

3.2.6.1 Electroless Depositions and Conductive Coatings

Replace the paragraph with:

Electroless depositions and conductive coatings **shall be** sufficient for subsequent plating processes and may be either electroless metal, vacuum deposited metal, or metallic or nonmetallic conductive coatings. Electroless nickel/immersion gold plating (ENIG) **shall** be in accordance with IPC-4552. Measurement location and extent **shall** be AABUS.

Caution: Immersion gold thicknesses above 0.125 µm [4.925 µin] can indicate an increased risk of having compromised the integrity of the nickel undercoat due to excessive corrosion. Due to the influence of the design pattern and chemistry process variability, acceptance of the solderability coupon may not represent the part. Correlation of thickness measurements across the pattern is strongly encouraged to demonstrate uniformity of the coating thickness.

Table 3-2 Final Finish, Surface Plating and Coating Thickness Requirements

Replace Table as follows:

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage & Solderable[4]	Coverage & Solderable[4]	Coverage & Solderable[4]
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable[4]	Coverage & Solderable[4]	Coverage & Solderable[4]
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold for edge-board connectors and areas not to be soldered - minimum	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold on areas to be soldered - maximum	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) - minimum	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]
N	Nickel - Electroplate for Edge Board Connectors - minimum	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier[1] - minimum	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	Organic Solderability Preservative	Solderable[4]	Solderable[4]	Solderable[4]
ENIG	Electroless Nickel - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]
	Immersion Gold (Solderable Surface)	Solderable[6]	Solderable[6]	Solderable[6]
	Immersion Gold (Other) - minimum	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
IS	Immersion Silver	Solderable[4,7]	Solderable[4,7]	Solderable[4,7]
IT	Immersion Tin	Solderable[4]	Solderable[4]	Solderable[4]

Code	Finish	Class 1	Class 2	Class 3
C	Bare Copper	As indicated in Table 3-7 and/or Table 3-8		
	Through-Holes			
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin areas	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]
	Blind Vias			
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]
	Microvias[3] (Blind and Buried)			
	Copper[2] - minimum average	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Minimum thin area	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	6 µm [236 µin]
	Buried Via Cores			
	Copper[2] - minimum average	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	Minimum thin area	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	7 µm [276 µin]
	Buried Vias (>2 layers)			
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]

[1]Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
[2]Copper plating (1.3.4.2) thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 section on copper plating thickness for hole walls.
[3]Blind microvias are vias that <0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink-formation followed by a plating operation. All performance characteristics for plated holes, as defined in this document, **shall** be met. The values given for blind and buried microvias in Table 3-2 are not applicable for stacked microvias. As of the publication of this specification, there is little known about this structure and the reliability results are not consistent with buried and blind microvias. Stacked microvias may also require different inspection criteria.
[4]See also 3.3.6.
[5]Wrap copper plating for filled plated holes **shall** be in accordance with 3.6.2.11.1.
[6]See also 3.2.6.1.
[7]See also 3.2.6.7.

3.2.6.7 Other

Change title to "Other Metals and Coatings," delete "immersion silver" and renumber to 3.2.6.8.

Append new 3.2.6.7 paragraph as follows:

3.2.6.7 Immersion Silver Plating Immersion silver plating **shall** be in accordance with IPC-4553. Unlike other surface finishes, immersion silver plating is available in two very distinctive but acceptable versions - a thin silver deposit and a thicker silver deposit. It is imperative that the supplier of the printed circuit boards inform the user of the immersion silver plating as to which type of silver they are supplying. Surface thickness measurements, when required for immersion silver, **shall** be in accordance with IPC-4553.

NOTE: Pad size for thickness measurements are defined in IPC-4553 and apply for both thin and/or thick silver deposits. Immersion silver finishes are not recommended for "contact surfaces" of Class 3 products.

3.2.6.8 Electrodeposited Copper

Renumber to 3.2.6.9

3.3.2.1 Measling

Replace paragraph as follows:

Measling is acceptable for Class 1, 2 and 3 end product, with the exception of high-voltage applications as defined by the customer. Refer to IPC-A-600 for more information.

Append notation as follows:

Note: The reader should be aware that, at the time of publication of this amendment to this specification, the IPC-A-610 and IPC-J-STD-001 assembly standards take exception to the bare board measling criteria for Class 3 in this specification.

3.4.3 Bow and Twist

Replace second sentence as follows:

End products **shall be** assessed in the delivered form.

3.6 Structural Integrity

Replace second and third sentences as follows:

Although the A and B or A/B coupons are assigned for this test, production boards may be used in lieu of the A and B or A/B coupons. Areas selected from boards **shall** contain holes and copper features so that all criteria within this specification can be evaluated.

Figure 3-8 Typical Microsection Evaluation Specimen (Three Plated-Through Holes)

Remove parenthetical "Three Plated-Through Holes" from the figure title.

3.6.2.11 Plating/Coating Thickness

Add new subsection 3.6.2.11.1 as follows:

3.6.2.11.1 Copper Wrap Plating Copper wrap plating minimum as specified in Table 3-2 **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required (see Figures 3-13 and 3-14). Reduction of wrap-plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-15).

Add new Figure 3-13 as follows:

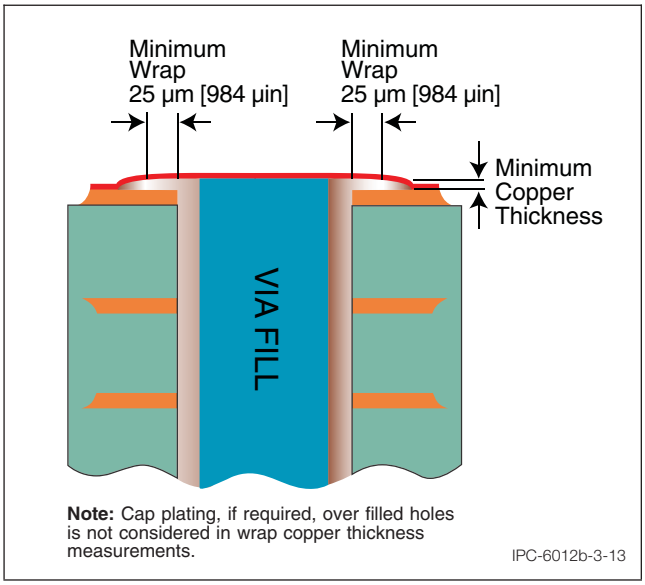

Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes)

Add new Figure 3-14 as follows:

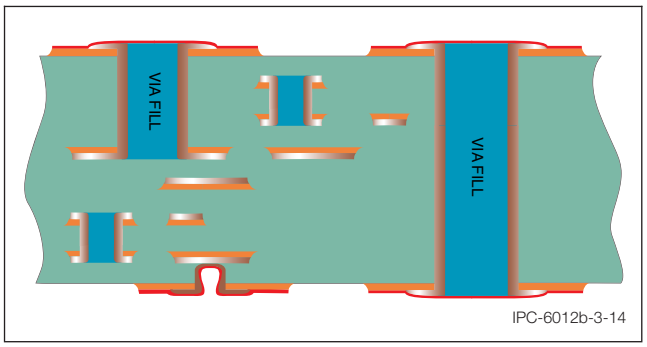

Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable)

Add new Figure 3-15 as follows:

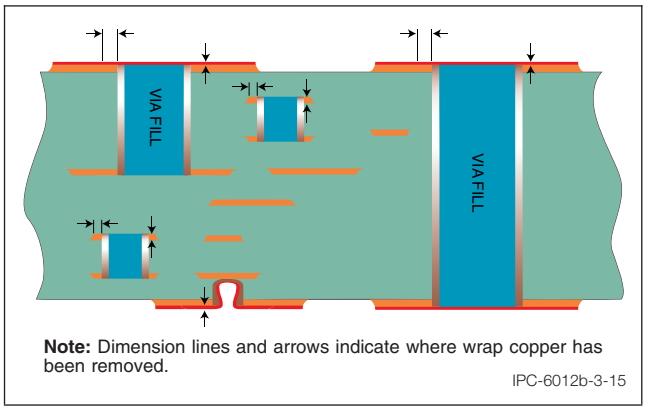

Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

Renumber existing Figure 3-13, Metal Core to Plated-Through Hole Spacing, to Figure 3-16

Renumber existing Figure 3-14, Measurement of Minimum Dielectric Spacing, to Figure 3-17.

3.7.2 Solder Resist Cure and Adhesion

Replace first sentence as follows:

The cured solder mask coating **shall not** exhibit tackiness, delamination, bubbles or blistering to the following extent;

3.8 Electrical Requirements

Replace sentence as follows:

When tested as specified in Table 4-3 and Table 4-4, the printed boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.10.1 Outgassing

Replace subsection as follows:

The degree of outgassing **shall** have a Total Mass Loss (TML) of less than one percent (1%) and Collectible Volatile Condensable Material (CVCM) of less than one tenth of one percent (0.1%). Mass loss **shall** be determined on test coupons or production boards of representative substrates when tested in accordance with IPC-TM-650, Method 2.6.4

Table 4-3 Acceptance Testing and Frequency

Append superscript notation to Solderability, Hole, as follows:

Hole[7]	3.3.6		A or A/B or S	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Panel

Append following note at bottom of Table 4-3:

7. Hole solderability testing not required for Type 2 double-sided boards without plated-through holes.

Append superscript notation to Structural Integrity After Stress Type 2 (Microsection) section header as follows:

Structural Integrity After Stress Type 2 (Microsection)[8]

Append following note at bottom of Table 4-3:

8. Cross sectioning not required for Type 2 double-sided boards without plated-through holes for plated-through hole evaluation.