Microvia Weak Interface Failures
Current Understanding and Mitigation

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The Defect in Pictures

Crack at layer 12-13 interface

L12-13, 500X, Unetched
L12-13, 500X, Etched
**Historical Quality Controls**

**PCB Level**
- Cross section analysis
- 6 solder floats
- 10 reflow cycles
- Air-Air T-Shock

**Product Level**
- T-Shock
- T-Cycle
- Burn-in

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- Difficult to assess microvia reliability based on structure of stackup
- All measured before and after the stimulus is applied.
- Burn-in has continuous monitoring but temperature well below Tg of typical PCB laminate
Board In-Situ Reflow Results

- 224.6°C
- 184.0°C
- 73 second open

S1: $y = 0.0725x + 17.357$
$R^2 = 0.9986$
$\alpha = 0.0042$
Product Level Failure Characteristics

- Intermittent in nature
- More often at hot temperatures vs. cold temperatures
- After storage of finished product
- After field deployment
- Unpredictable reliability
Current Mitigations - Test

Implement

IPC-TM-650 2.6.27A
# Current Mitigations – HDI Designs

<table>
<thead>
<tr>
<th>Level</th>
<th>PCB Design Approach</th>
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<tbody>
<tr>
<td>Preferred</td>
<td>Staggered microvia only</td>
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<tr>
<td></td>
<td>2-stack maximum</td>
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<tr>
<td></td>
<td>3L HDI = single offset with 2-stack</td>
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<tr>
<td></td>
<td>4L HDI = two offset 2-stacks</td>
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<tr>
<td></td>
<td>Minimize 2 &lt; N ≤ 3 stack</td>
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<tr>
<td>Unacceptable</td>
<td>Unlimited 2 &lt; N ≤ 3 stack</td>
</tr>
<tr>
<td></td>
<td>N &gt; 3 stack</td>
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Current Mitigations – PCB Fabrication
Summary

• Stacked microvias can fracture at the metallurgical interfaces during reflow
• Product level failure unpredictable
• Historical industry standard test methods are not effective in detecting failures
• IPC TM-650 2.6.27A technique duplicates assembly reflow and reliably detects potential problems
• Failures can be minimized by PCB design approach
• Root cause unknown; Industry in containment mode
• IPC V-TSL-MVIA team formed to identify root cause and determine appropriate corrective actions