JOINT INDUSTRY STANDARD
IMPLEMENTATION OF FLIP CHIP AND CHIP SCALE TECHNOLOGY

COORDINATED BY THE SURFACE MOUNT COUNCIL
# Table of Contents

1 **SCOPE** .......................................................... 1
   1.1 Purpose .................................................................. 1
   1.2 Categorization ..................................................... 1

2 **TECHNOLOGY OVERVIEW** ........................................... 1
   2.1 History of Flip Chip ............................................... 1
   2.1.1 Hybrid Thick Film Packages ................................ 3
   2.1.2 Hybrid Thin Film Packages .................................. 4
   2.1.3 Multilayer Ceramic Substrate (MLC) ..................... 4
   2.1.4 Thin Film on Multilayer Ceramic ........................... 5
   2.1.5 Thin Film on Organic Epoxy/Glass Laminate .......... 5
   2.1.6 Chip on Flexible Printed Board ............................ 5
   2.1.7 Thin Film on Silicon .......................................... 5
   2.1.8 Characteristics of Flip Chip Technology ............... 6
   2.2 Introduction to Chip Scale Packaging ....................... 7
   2.2.1 Chip Scale Grid Array Packages ......................... 9
   2.2.2 Peripheral Ledged Chip Scale Packages (CSP-P) ........ 13
   2.2.3 Advantages and Disadvantages of Chip Scale Technology ........................................... 14

3 **APPLICATIONS OF FLIP CHIP AND CHIP SCALE** ........... 16

4 **DESIGN CONSIDERATIONS** ......................................... 17
   4.1 Chip Size Standardization ...................................... 17
   4.1.1 Bump Site Standards ........................................ 17
   4.1.2 Peripheral Lead Standards ................................... 18
   4.1.3 Package Size Standards ...................................... 18
   4.2 General Considerations for Flip Chips ....................... 18
   4.2.1 Final Metal .................................................... 18
   4.2.2 Passivation .................................................... 18
   4.2.3 Pad Limiting Metals ......................................... 19
   4.2.4 Solder Bump ................................................... 20
   4.2.5 Existing Chip Designs ........................................ 21
   4.2.6 I/O Capability ................................................ 21
   4.2.7 Alphabet Particle Emissions (Soft Errors) .............. 22
   4.2.8 Edge Seal Design ............................................. 23
   4.3 General Consideration for Chip Scale ....................... 23
   4.3.1 Chip Scale Grid Arrays (CSP-A) .......................... 23
   4.3.2 Peripheral Ledged Chip Scale Packages (CSP-P) ....... 24
   4.4 Substrate Structure Standard Grid Evolution .............. 24
   4.4.1 Footprint Design ............................................. 25
   4.4.2 Design Guide Checklist ..................................... 25
   4.4.3 Footprint Population ......................................... 28
   4.5 Design Output Requirements .................................. 29

4.5.1 Final Metal Reticle Mask ..................................... 30
4.5.2 Passivation (Terminal Via) Reticle Mask and Plan ........ 30
4.5.3 Unit Cell Design ............................................. 30
4.5.4 Printed Board Land Pattern Design ....................... 30
4.6 Electrical Design .............................................. 30
4.6.1 Equivalent Circuitry .......................................... 30
4.6.2 Final Metal Traces ........................................... 31
4.6.3 Inductance and Capacitance ................................. 34
4.6.4 High Frequency Performance ............................... 34
4.7 Thermal Design ................................................ 34
4.7.1 Bump Interconnect Thermal Model ......................... 35

5 **MATERIAL PROPERTIES AND PROCESSES** .................... 37
   5.1 Solder Bumping ................................................ 37
   5.1.1 Solder Evaporation ......................................... 37
   5.1.2 Solder Electroplating ....................................... 37
   5.1.3 Solder Paste Deposition .................................... 38
   5.1.4 Conductive Paste Method .................................. 38
   5.2 Conductive Adhesives ......................................... 38
   5.2.1 Design Issues ................................................. 39
   5.2.2 Anisotropic Adhesive Details ............................... 40
   5.3 Solder Bump Evaluation ........................................ 40
   5.4 Other Bumping Techniques and Materials .................. 41
   5.4.1 Board Process Attach ....................................... 41
   5.4.2 Gold Bumping ............................................... 41
   5.4.3 Gold Bump Flip Chip ........................................ 41
   5.4.4 Indium-Based Bumps ......................................... 41
   5.4.5 Bump Transfer ............................................... 41
   5.4.6 Stud Bumping (Ball Bonding) .............................. 42
   5.5 Chip Materials ................................................ 42
   5.6 Other Bumping Process Considerations ..................... 43
   5.6.1 Redistribution ................................................ 43
   5.6.2 Electrostatic Discharge (ESD) ............................. 43
   5.7 Handling, Shipping and Storage ............................. 43

6 **Mounting and Interconnection Structures** ....................... 43
   6.1 Background .................................................... 44
   6.2 Mounting Structures General Considerations ............. 45
   6.3 Interconnection Substrate Material Choices ............... 48
   6.3.1 Rigid Organic Substrates .................................. 48
   6.3.2 Flexible Laminate ........................................... 49
   6.3.3 Inorganic Substrates ....................................... 49
   6.4 Surface Finish Properties ..................................... 50
   6.4.1 Chemical plating finishes (electrolytic and electroless) ........................................... 50
   6.4.2 Thick film metallic finishes ............................... 51
8.0 Flip Chip Test and Burn-in Methodology

8.1 Known Good Die
8.1.1 IC Quality
8.1.2 IC Reliability
8.2 KGD Techniques for Flip Chip
8.2.1 IBM’s R3
8.2.2 MCNC’s Burn-in and Test Substrate (BATS)
8.2.3 IBM’s Dendrite Temporary Chip Attach (TCA)
8.3 Known-Good Mounting and Interconnection Structure
8.3.1 Testing Techniques
8.4 Product Verification
8.4.1 Standard Test Access Port and Boundary Scan Architecture

9 Requirements for Reliability
9.1 Robustness of Products to Use
9.1.1 Chip Scale Package Robustness and Reliability
9.2 Reliability Factors
9.2.1 Wear Out Mechanisms
9.2.2 Solder Bump Mechanical Reliability
9.2.3 Reliability Modeling
9.3 Reliability Testing
9.3.1 Wear-Out Mechanisms
9.3.2 Reliability Factors
9.3.3 Event Related Failures
9.4 Design for Reliability (DfR)
9.4.1 Damage Mechanisms and Failure of Solder Attachments
9.4.2 Reliability Prediction Modeling
9.4.3 DfR-Process
9.4.4 Validation and Qualification Tests
9.4.5 Screening Procedures

10 Standardization
10.1 Standards for Development
10.2 Flip Chip Development and Performance Standards
10.2.1 Flip Chip IC/Component Design
10.2.2 Mechanical Outline Standards
10.2.3 Performance Requirements for Bumps
10.2.4 Physical Flip Chip Testing Requirements
10.2.5 Trays for Flip Chip (Shipping and Delivery)
10.2.6 Configuration Management
10.3 Standard on Mounting of Substrate Design and Performance
10.3.1 Design Standard for Flip Chip or Chip Scale Package Mounting
10.3.2 Qualification and Performance of Organic Mounting Structures intended for Flip Chip Mounting
10.3.3 Qualification and Performance of Inorganic Mounting Structures Intended for Flip Chip Mounting
10.3.4 Qualification, Quality Conformance, and Inprocess Test Methods used for Organic/Inorganic Flip Chip Mounting Structures
10.4 Flip Chip/Substrate Assembly Design and Performance Standards
10.4.1 Flip Chip Assembly Design
10.4.2 Assembly Performance Requirements
10.4.3 Assembly Test Methods
10.4.4 Qualification and Performance of Rework and Repair of Flip Chip Assembly
10.4.5 Assembly Reliability
10.5 Standards for Material Performance
10.5.1 Underfill Material Requirements
10.5.2 Passivation Material Requirements
10.5.3 Encapsulation Material Requirements
10.5.4 Adhesives Used for Flip Chip Assembly
10.5.5 Flux for Flip Chip Mounting Applications

11 Future Needs
11.1 Critical Factor: Manufacturing Infrastructure
11.1.1 Materials
11.1.2 Equipment
11.1.3 Design ................................................................. 89
11.2 Critical Factor: Bump Attachment and Bonding ...................... 90
11.2.1 Dimensional Control ............................................. 90
11.2.2 Metallurgical Integrity ........................................... 90
11.2.3 Cleanliness of Bumping Site .................................... 90
11.3 Critical Factor: Testing Scenarios .................................. 90
11.3.1 Critical Environmental Testing ................................. 90
11.3.2 Die Testing for KGD ............................................. 90
11.3.3 Inspection and Process Control Assurance .............. 91
11.4 Total Quality Management and Manufacturing (TQMM) ....... 91

Figures
Figure 2−1 Basic Metallurgy/Glass Design for SLT Transistors ................. 2
Figure 2−2 Chip Collapse and Edge Shorting Problem During Solder Reflow Joining and Two Solutions .................................................. 2
Figure 2−3 Flip Chip with Silver Bump Stand-Off......................... 2
Figure 2−4 Thick Film Glass Dam Preventing Solder Flow and Collapse in First C4 Application ................................................. 2
Figure 2−5 Early IBM Hybrid Thick Film Module Mixing Copper Ball SMT Transistors and C4 Integrated Circuit. (12 mm) .................. 3
Figure 2−6 Thin Film Chromium-Copper-Chromium on Ceramic (MC) ............................................................ 3
Figure 2−7 Cross-Section of Cofired Alumina Multilayer Ceramic Package ............................................................ 3
Figure 2−8 Full Area Array C4 Configuration Microprocessor with 762 Solder Bumps in a 29x29 Array ............................................................ 4
Figure 2−9 Depopulated C4 Array on Chip .................................... 4
Figure 2−10 Area Array C4 Configuration (a) 11x11 Full Array with Cantilevered Silicon, (b) SEM View .................................................. 5
Figure 2−11 Structure of Hybrid IC Using Solder Bump and Cross-Sections ............................................................ 6
Figure 2−12 Uncapped 50 mm Multi-Chip Module (MCM)............. 6
Figure 2−13 IBM Thermal Conduction Module with 100-130 Flip Chips and Hat with Piston Assemblies ............................................. 6
Figure 2−14 Effect of TCE Mismatch on Solder Fatigue Life ......... 7
Figure 2−15 AT&T Silicon-on-Silicon Packaging System ............. 7
Figure 2−16 Cut-away of IBM Glass/Ceramic TCM with Polyimide/Thin Film Surface Redistribution Layer ..................... 8
Figure 2−17 C4 Life Extension by Use of Filled Epoxy Resins with Matching Expansivity (Hitachi) ................................. 8
Figure 2−18 IBM SLIC Chip-on-Card Technology ............................. 9
Figure 2−19 Bridging the Gap ................................................ 9
Figure 2−20 Chip Scale Grid Array Package (CSP-A) .................. 9
Figure 2−21 Example of Chip Scale ....................................... 10
Figure 2−22 Micro BGA .................................................. 10
Figure 2−23 Mini BGA .................................................. 11
Figure 2−24 SLIC Chip Scale Grid Array .................................. 11
Figure 2−25 Chip Scale Package ........................................ 12
Figure 2−26 Resin Encapsulated LSI Chip with Bumps ................. 12
Figure 2−27 Peripheral Area Array Converter ............................ 13
Figure 2−28 Cutaway View of an MSMT Packaged IC ................. 14
Figure 2−29 MSMT Posts in Saw Lane .................................. 14
Figure 2−30 MSMT Posts in Bonding Pad Area ......................... 14
Figure 2−31 Cross-Sectional View of an MSMT Package ............. 15
Figure 2−32 Close-up Photo of MSMT Posts, Encapsulant and Bottom of the Chip .................................................. 15
Figure 2−33 Chip Scale Peripheral Package ............................... 15
Figure 4−1 Flip Chip Connection ......................................... 17
Figure 4−2 Mechanical and Electrical Connections .................... 17
Figure 4−3 Joined Chip with Chip Underfill ................................ 18
Figure 4−4 A Solder Bump Flip Chip Connection ....................... 18
Figure 4−5 Two Simple Chips, Showing Original Pad Locations and Rerouted Bumps ............................................. 19
Figure 4−6 Redistribution of a Single Metal Layer Device ............ 19
Figure 4−7 Passivation (Cross-Section) ................................... 19
Figure 4−8 Schematic Plan View of Bump ................................ 20
Figure 4−9 Example of Pad Limiting Metal ............................... 20
Figure 4−10 Initial C4 Bump .............................................. 21
Figure 4−11 A C4 Bump After Reflow .................................... 21
Figure 4−12 Recommended DCA Grid Pitch (250 μm Grid, 150 μm Bumps) .................................................. 21
Figure 4−13 Interconnect Density (Peripheral vs. Area Array) ......... 22
Figure 4−14 Alpha Particle Emission Track and E/H Pairs .......... 23
Figure 4−15 Distortion of Depletion by Alpha Particles ............... 23
Figure 4−16 Chip Edge and Polyimid Seal ............................... 23
Figure 4−17 MSMT Post Configurations .................................. 24
Figure 4−18 Standard Grid Structure ...................................... 25
Figure 4−19 Bump Footprint Planning ..................................... 26
Figure 4−20 Alignment to Visual/Sensitive Chip Structures .......... 27
Figure 4−21 Minimum Pitch from Bump to Passivation Seal (‘A’−1½2 finished bump diameter, plus alignment to tolerances, plus desired minimum) .................................................. 28
Figure 4−22 Redundant Footprint ......................................... 29
Figure 4−23 Design Shrink Footprint ...................................... 29
Figure 4−24 Signal and Power Distribution Position ..................... 30
Figure 4−25 Nested I/O Footprints ........................................ 30
Figure 4−26 Typical Bump Passivation Reticle Mask Format .......... 31
Figure 4−27 Product Unit Cell Plan (example) ............................ 31
Figure 4−28 Printed Board Flip Chip or Grid Array Land Patterns .... 32
Figure 4−29 MSMT Land Drawing and Dimensions .................... 32
Figure 4−30 Bump Electrical Path (Redistributed Chip) ............... 33
Figure 4−31 Bump Equivalent Circuit (Redistributed Chip) ......... 33
Figure 4−32 Final Metal Trace and Underlying Traces (Cross Section) .................................................. 34
Figure 4−33 Thermal/Electrical Analogy ............................................ 35
Figure 4−34 Bump Interconnect Equivalent Model ................................ 35
Figure 4−35 Thermal Paste Example .................................................. 36
Figure 4−36 Approximate Thermal Model for Thermal Paste .............................................................. 36
Figure 4−37 Chip Underfill Example .................................................. 36
Figure 4−38 Approximate Thermal Model for Chip Underfill .............................................................. 36
Figure 5−1 Photomicrograph of As-Plated Solder Pads .............................................................. 37
Figure 5−2 Photomicrograph of Solder Bumps .................................................. 38
Figure 5−3 An Example of Fine Line Stencil Printing .............................................................. 39
Figure 5−4 Gold Bumped IC Adhesively Attached to a Glass Substrate .................................................. 42
Figure 5−5 Newly Developed Chip on Glass Technology .............................................................. 42
Figure 5−6 Schematic Cross-Sectional View of Connection for Chip on Glass .............................................................. 42
Figure 5−7 Redistribution of a Peripheral Pattern .............................................................. 43
Figure 5−8 ESD Path to Ground .............................................................. 43
Figure 6−1 Packaging Efficiency .............................................................. 44
Figure 6−2 Exploded View of a Substrate for Flip Chip or Chip Scale Applications .............................................................. 46
Figure 6−3 Wire Routing Ability of Different Design Rules for One and Two Sided PWBs .............................................................. 47
Figure 6−4 Conductor Routing Comparison .............................................................. 47
Figure 9−1 Chip Scale Package Lead Compliance .............................................................. 64
Figure 9−2 Fracture Due to Fatigue/Creep Interaction .............................................................. 67
Figure 9−3 Example of Solder Bump Fatigue Curves .............................................................. 67
Figure 9−4 Thermal Cycling Frequency Threshold vs. Temperature .............................................................. 68
Figure 9−5 Compliant Lead Alternative to Underfill .............................................................. 69
Figure 9−6 Lognormal Distribution of Thermal Cycle Failures .............................................................. 70
Figure 9−7 Effect of $\alpha$ on Reliability .............................................................. 71
Figure 9−8 Acceleration Factor Shift of Lognormal Distribution .............................................................. 72
Figure 9−9 Thermal Cycling Test Profile .............................................................. 73
Figure 9−10 Pre-Conditioning Thermal Profile .............................................................. 74
Figure 9−11 Depiction of the Effects of the Accumulating Fatigue Damage in Solder Joint Structure .............................................................. 77
Figure 10−1 Semiconductor Design .............................................................. 84
Figure 10−2 Mechanical Outlines .............................................................. 84
Figure 10−3 Bump Performance .............................................................. 84
Figure 10−4 Flip Chip and Chip Scale Test Methods .............................................................. 84
Figure 10−5 Flip Chip/Chip Scale Carrier Trays .............................................................. 84
Figure 10−6 Flip Chip/Chip Scale Configuration Management .............................................................. 85
Figure 10−7 Mounting Structures Design .............................................................. 85
Figure 10−8 Organic Mounting Structure Performance .............................................................. 85
Figure 10−9 Inorganic Mounting Structure Performance .............................................................. 86
Figure 10−10 Mounting Structure Test Methods .............................................................. 86
Figure 10−11 Assembly Design Configuration .............................................................. 86

Figure 10−12 Assembly Performance Requirements .............................................................. 86
Figure 10−13 Assembly Test Methods .............................................................. 87
Figure 10−14 Assembly Rework and Repair .............................................................. 87
Figure 10−15 Assembly Reliability .............................................................. 87
Figure 10−16 Underfill Material Performance .............................................................. 87
Figure 10−17 Passivation Material Performance .............................................................. 87
Figure 10−18 Encapsulation Material Performance .............................................................. 88
Figure 10−19 Flip Chip/Chip Scale Adhesives .............................................................. 88
Figure 10−20 Flux Qualification and Performance .............................................................. 88

Tables
Table 3−1 Commercial Flip Chip and Chip Scale Applications .............................................................. 16
Table 3−2 Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die .............................................................. 16
Table 4−1 Commonly Used PLM Systems .............................................................. 20
Table 4−2 C4 Bump Diameter and Minimum Pitch Options .............................................................. 21
Table 4−3 Alpha Particle Emissions of Semiconductor Materials .............................................................. 22
Table 4−4 Chip Edge Seal Dimensions (Typical) .............................................................. 23
Table 4−5 Design rules for substrates for Chip Scale Technology .............................................................. 25
Table 4−6 Terminal Via and Final Metal Via Pitch .............................................................. 27
Table 4−7 Final Metal Signal Trace (30 µm) .............................................................. 34
Table 4−8 Final Metal Power Trace (60 µm) .............................................................. 34
Table 4−9 Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip) .............................................................. 35
Table 4−10 Typical Bump (150 µm) Thermal Resistances Multi-Layer Metal Chips .............................................................. 36
Table 6−1 Comparison of Selected Material Properties .............................................................. 48
Table 6−2 Inorganic Substrate Characteristics .............................................................. 50
Table 9−1 Product Categories and Use Environments .............................................................. 65
Table 9−2 Coefficients of Thermal Expansion .............................................................. 66
Table 9−3 Typical Heights (Joined) .............................................................. 66
Table 9−4 Acceleration Factor Values for Example 1 .............................................................. 71
Table 9−5 Representative Realistic Worse Case Use Environments for Surface Mounted Electronics and Recommended Accelerated Testing for Surface Mount Attachments by Most Common Use Categories .............................................................. 75
Implementation of Flip Chip and Chip Scale Technology

1 SCOPE
This document describes the implementation of flip chip and related chip scale semiconductor packaging technologies. The areas discussed include: design considerations, assembly processes, technology choices, application, and reliability data. Chip scale packaging variations include: flip chip, High Density Interconnect (HDI), Micro Ball Grid Array (µBGA), Micro Surface Mount Technology (MSMT) and Slightly Larger than Integrated Circuit Carrier (SLICC).

1.1 Purpose
This document is intended to provide general information on implementing flip chip and chip scale technologies for creating single chip or multichip modules (MCM), IC cards, memory cards and very dense surface mount assemblies.

1.2 Categorization
Flip chip is categorized as versions of a tin-lead (SnPb) solder bump process, and alternative solutions that use other forms of chip bond site bumping.

Chip scale technology is categorized as semiconductor chip structures that have been made robust to facilitate ease of chip handling, testing and chip assembly. The chip scale technologies have common attributes of minimal size, no more than 1.2X the area of the original die size, and are direct surface mountable.

2 TECHNOLOGY OVERVIEW
Flip chip and chip scale technology relate to methods used to provide an efficient technique for interconnecting semiconductor die to a substrate. Over the years flip chip technology has grown in stature and expanded into the more generic area of chip scale technology. In addition, many new techniques for mounting bare die were also established. Today, enhancements of the semiconductor die, which ruggedize the product to facilitate ease of handling and testing, have established another level of packaging technology in which many companies can participate.

2.1 History of Flip Chip
Flip chip solder bump interconnection technology is over 30 years old. It was first conceived and developed in 1960-61 by IBM for the Solid Logic Technology (SLT) hybrid electronic circuitry in IBM’s System 360 computers introduced in April 1964.

At that time, standard transistor packaging used hermetically sealed metal cans with glass sealed wires emerging from a header upon which the germanium or silicon chip was metallurgically backbonded. Manual thermocompression wire bonding to the chip was the common technique.

Although transistor technology was much more reliable than vacuum tube technology that preceded it, the packaging and interconnection technologies were weak. Faulty manual wire bonds, purple plague (gold-aluminum intermetallic formation), and aluminum corrosion of thin film interconnections on the chip, even in hermetic packages, were all reliability concerns. In addition, manufacturability and productivity were deficient.

SLT transistors and diodes were glass passivated at the wafer level to protect aluminum wiring from the environment. Glass frits of borosilicate glass were fused on the surface of transistor wafers after the aluminum wiring was formed. The glass film obviated the need for a hermetic enclosure because the transistor was sealed at the chip level.

Consistent with maintaining a hermetic seal was the idea of etching via holes in the glass where electrical connections were to be made, and hermetically resealing the holes with an overlapping, larger pad of metal films. The first film, typically chromium, was used to create a good bond to glass and aluminum.

Subsequent metal films, typically copper and gold, were deposited to provide wettability and solderability for a ball of metal alloy that was to be melted on the pad. Originally, the ball was an alloy of Au-Sn eutectic which melted at 360°C; therefore, the pad was called the ball-limiting metallurgy because the melted ball would not wet the glass beyond the area of the pad. Later the ball or bump became a solder bump with an embedded copper ball “stand-off,” shown in figure 2-1.

The packaging concept required that thick film electrodes or wires be screened and fired on alumina substrates. Originally, the thick film was glass fritted Au-Pt paste; later it became Ag-Pd. The wiring was hot dip tinned with 90Pb-10Sn solder to improve conductance and to interconnect the active and passive components. For each transistor, three of the screened wires were to terminate in a spot that would be the mirror image of the chip bumps.

After each chip site was fluxed with a droplet of sticky water white rosin flux, the chip was picked up and placed on the solder coated electrodes face down or “flipped” compared to normal chip placement. Subsequently, the substrate was heated in a furnace to remelt the solder coating,