IPC J-STD-001GS-AM1

Space and Military Applications Electronic Hardware Addendum to IPC J-STD-001G Requirements for Soldered Electrical and Electronic Assemblies

Amendment 1

Developed by the J-STD-001 Space and Military Electronic Assemblies Task Group (5-22as) of the Assembly & Joining Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

Space and Military Applications Hardware Addendum to J-STD-001G, Amendment 1, Requirements for Soldered Electrical and Electronic Assemblies

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Table 1 J-STD-001GS, Amendment 1, Space and Military Applications Requirements

<table>
<tr><th>J-STD-001G AM1 Reference</th><th>Space Applications Requirement</th></tr>
<tr><td>8</td><td>CLEANING AND RESIDUE REQUIREMENTS
Unless otherwise specified by design, or by the User, the acceptability of the residue condition shall be determined at the point of the manufacturing process for each assembly just prior to the application of conformal coating, or on the final assembly if conformal coating is not applied.</td></tr>
<tr><td>8.1</td><td>Qualified Manufacturing Process Unless otherwise specified by the User, the Manufacturer shall qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues. Objective evidence shall be available for review. See J-STD-001 Appendix C for examples of objective evidence. Rework processes shall be included in the process qualification.
The use of the 1.56 µg/NaCl equivalence/cm^2 value for resistivity of solvent extract (ROSE), with no other supporting objective evidence, is not considered an acceptable basis for qualifying a manufacturing process (see IPC-WP-019).</td></tr>
<tr><td>8.1.1</td><td>Cleaning Designator Unless otherwise specified by the User/Design Authority, the Manufacturer should specify a cleaning designator that establishes the cleaning option and process control tests for manufacturing residues. The cleaning designator is a 2-digit (minimum) code that describes the cleaning and process control testing required for assemblies under this standard. The code begins with the letter ‘‘C’’ and then a dash followed by two or more digits. The first digit represents the cleaning option:
Table 8-1 Designation of Surfaces to be Cleaned
<table><tr><td>0</td><td>No surfaces to be cleaned</td></tr><tr><td>1</td><td>One side (solder source side) of assembly to be cleaned</td></tr><tr><td>2</td><td>Both sides of assembly to be cleaned</td></tr></table>
The second and any subsequent digits define the requirements for process control of residues:
Table 8-2 Residue Testing for Process Control
<table><tr><td>0</td><td>No test required</td></tr><tr><td>1</td><td>Test for rosin residues required (see 8.6)</td></tr><tr><td>2</td><td>Test for ionic residues required (see 8.2)</td></tr><tr><td>3</td><td>Test for surface insulation resistance (Note 1)</td></tr><tr><td>4</td><td>Test for surface organic contaminants (Note 1)</td></tr><tr><td>5</td><td>Other testing (Note 1)</td></tr></table>
Note 1: As agreed between Manufacturer and User if required.
In the absence of a specified cleaning designator, the designator C-22 shall apply to printed board assemblies. A cleaning designator of C-00 specifies a ‘‘no clean’’ process with no testing for residues. A cleaning designator of C-223 specifies a printed board assembly requiring cleaning on both sides, in addition to ionic residue and surface insulation resistance (SIR) testing. Cleanliness designator C-10 and the visual requirements for cleanliness (see 8.4 Foreign Object Debris (FOD) and 8.5 Visual Residues of this addendum) shall apply to designs incorporating discrete solder terminations, e.g., solder cups, wire splices, or wire/braid, not terminated to a printed board assembly.</td></tr>
<tr><td>8.2</td><td>Ionic Process Monitoring When a manufacturing process has been defined and qualified per 8.1 Qualified Manufacturing Process of this addendum, and when ionic residue testing is required, ionic residue testing shall be controlled as follows:</td></tr>
<tr><td>8.2.1</td><td>Sampling Plan The Manufacturer shall determine an objective sampling plan (see IPC-9194 for guidance) for measuring ionic residues of the process by using ROSE testing per IPC-TM-650, Method 2.3.25, or other methods as agreed between Manufacturer and User. The sampling plan shall define the test frequency.</td></tr>
<tr><td>8.2.2</td><td>Control Limits The Manufacturer shall determine an Upper Control Limit (UCL) for ionic residue process testing based on the results of 8.1 Qualified Manufacturing Process of this addendum, and have objective evidence available for review.</td></tr>
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