IPC J-STD-001FS

Space Applications Electronic Hardware Addendum to IPC J-STD-001F Requirements for Soldered Electrical and Electronic Assemblies

Developed by the Space Electronic Assemblies J-STD-001 Addendum Task Group (5-22as) of the Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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The following reference numbers are to J-STD-001E Clauses that are modified or added in this Addendum.

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0.1 Scope This Addendum provides requirements to be used in addition to, and in some cases, in place of, those published in IPC J-STD-001F to ensure the reliability of soldered electrical and electronic assemblies that must survive the vibration and thermal cyclic environments getting to and operating in space.

0.1.1 Purpose When required by procurement documentation/drawings, this Addendum supplements or replaces specifically identified requirements of IPC J-STD-001, Revision F of July 2014.

0.1.2 Precedence The contract takes precedence over this Addendum, referenced standards and User-approved drawings. In the event of a conflict between this Addendum and the applicable documents cited herein, this Addendum takes precedence. Where referenced criteria of this Addendum differ from the published IPC J-STD-001F, this Addendum takes precedence. In the event of conflict between the requirements of this Addendum and the applicable assembly drawing(s)/documentation, the applicable User approved assembly drawing(s)/documentation take precedence. See Table 1 of this Addendum, clauses 1.7 Order of Precedence and 1.7.1 Conflict.

0.1.3 Existing or Previously Approved Designs This Addendum **shall not** constitute the sole cause for the redesign of previously approved designs. When drawings for existing or previously approved designs undergo revision, they should be reviewed and changes made that allow for compliance with the requirements of this Addendum.

0.1.4 Use This Addendum is not to be used as a standalone document.

Where criteria are not supplemented, the Class 3 requirements of IPC J-STD-001F **shall** apply. Where IPC J-STD-001F criteria are supplemented or new criteria are added by this Addendum, the clause is listed in J-STD-001FS, Table 1, Space Applications Requirements, and the entire IPC J-STD-001F clause is replaced by this Addendum except as specifically noted.

The clauses modified by this Addendum do not include subordinate clauses unless specifically stated, e.g., 1.4 does not include 1.4.1. Clauses, Tables, Figures, etc., in IPC J-STD-001F that are not listed in this Addendum are to be used as-published.

0.1.5 Lead-Free Tin For the purpose of this document, lead-free tin is defined as tin containing less than 3 percent lead by weight as an alloying constituent. Solder alloy SnAg3.7 is exempt from this requirement. See Table 1 of this Addendum, clause 3.2.

0.1.6 Use of Lead-Free Tin The use of components, assemblies, packaging technology, mechanical hardware, and materials meeting any of the following conditions **shall** be prohibited unless documented and controlled through a User approved Lead Free Control Plan (LFCP) incorporating either a replating or hot solder dip (HSD) process that completely replaces the lead-free tin finish, or a minimum of two mitigation measures.

- Lead-free tin plating, metallization, etc., on external surfaces of parts, mechanical parts, etc., or in internal cavity surfaces, i.e.: hybrid, relay crystal cans, MEMS, etc.
- Any components, printed circuit assemblies (PCAs), etc., assembled with lead-free tin solder alloys except SnAg3.7, see paragraph 3.2.

0.1.6.1 Lead Free Control Plan The Lead Free Control Plan (LFCP) **shall** document controls and processes that assures that assemblies containing lead-free tin solder alloys and/or component finishes will perform as intended within the expected parameters of the mission, e.g., environment, duration, etc. At a minimum, the LFCP **shall:**

a. Document the use of lead-free tin technology and prevent its use without review and approval by the User prior to implementation.

b. Incorporate a minimum of two mitigation measures when the lead-free tin finish is not completely replaced through a replating or HSD process.

c. Include any special design requirements, mitigation measures, test and qualification requirements, quality inspection and screening, marking and identification, maintenance, and repair processes.

d. Require review and approval by the User prior to implementation.

The following documents may be helpful when developing the LFCP:

- GEIA-STD-0005-1, Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder
- GEIA-STD-0005-2, Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems
- GEIA-HB-0005-1, Program Management / Systems Engineering Guidelines For Managing The Transition To Lead-Free Electronics
- GEIA-HB-0005-2, Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Lead-free Solder and Finishes
- GEIA-STD-0006, Requirements for Using Solder Dip to Replace the Finish on Electronic Piece Parts

0.1.6.2 Mitigation Components, sub-assemblies, assemblies, and mechanical hardware identified as having lead-free tin surfaces, plating, metallization, etc., but which by package design or engineering decision are not protected