ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

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Report on Round Robin Study to Correlate Interconnect Stress Test (IST) with Thermal Stress/Microsectioning Evaluations for Detecting the Presence of Inner-Layer Separations

Developed by the Post Separation Task Group (D-33c) of the Rigid Printed Board Committee (D-30) of IPC

Users of this technical report are encouraged to participate in the development of future revisions.

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REPORT ON ROUND ROBIN STUDY TO CORRELATE INTERCONNECT STRESS TEST (IST) WITH THERMAL STRESS/ MICROSECTIONING EVALUATIONS FOR DETECTING THE PRESENCE OF INNER-LAYER SEPARATIONS

SECTION 1 — INTRODUCTION

OBJECTIVE

The objective of this round robin was to provide the industry with a test method that removes the subjectivity of microsection evaluation after Thermal Stress exposure for detecting the presence of inner-layer separations in plated-through holes and gives greater reproducibility than current optical evaluations.

The purpose of this test program is to determine the ability of Interconnect Stress Testing (IST) to induce and measure inner-layer separation and to correlate IST with Thermal Stress/microsection testing. The two specific test methods used were IPC-TM-650, Methods 2.6.26 - DC Current Induced Thermal Cycling Test, and 2.6.8 - Thermal Stress of Plated-Through Holes.

The goal was to assess IST use as a test for incoming inspection in lieu of Thermal Stress.

BACKGROUND

The IPC D-33c Post Separation Task Group was formed in the fall of 1989. It had the following objectives:

- Provide a forum for discussion regarding detection of separation between inner-layers and plated-through hole wall copper.
- Establish a round robin.
- Distribute a questionnaire regarding:
  - Occurrence of inner-layer separation.
  - Microsection processes used to determine presence of inner-layer separation.
- Determine capability of test methods within testers.
- Collect Field Failure information.

The need for such a group was based on the fact many bare boards were found to have inner-layer separation after assembly processing which was not detected by the lot acceptance testing at the board shop level.

From 1989 to 1991 a questionnaire was developed, disseminated and analyzed. It then became apparent that there were many different approaches to making and evaluating microsections.

In 1991 a charter for a subsequent round robin was developed. The charter was to evaluate the use of microsections to find very fine inner-layer separations. Samples were built which were known to have varying degrees of inner-layer separation after Thermal Stress exposure for this round robin. Conclusions from that initial round robin are as follows:

- There was agreement between testers on inner-layer separations > than approximately 2.5 µm [100 µin].
- There was no agreement between testers on inner-layer separations < approximately 0.8 µm [30 µin].
- Microsections must be etched to verify that observations made in the as polished condition are inner-layer separations.
- Agreement between testers is possible when testers evaluate the same mounts.
- The samples prepared of the coupon set without any thermal stress did not show any inner-layer separations. This was consistent for all laboratories involved in the round robin.
- There was no consensus regarding observations in the ‘‘as polished’’ condition.
  - Improper etching can obscure fine-line inner-layer separations.
  - Scanning Electron Microscopy analysis of the same samples did not show a one to one correlation between lines observed as polished and confirmed inner-layer separations after etching.