ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

IPC-MC-790

Guidelines for Multichip Module Technology Utilization

Developed by the IPC Multichip Module Subcommittee of the Hybrid and Related Technologies Committee of IPC

About this document

This document published by IPC is for informational purposes and can serve as a baseline for selecting an appropriate MCM technology. It is not intended to be a standard and in fact, this document is expected to evole with significant technological developments.

This document reports on work which has been done by a variety of individuals and organizations concerned with increasing system performance and reliability through multichip module technology. You, as the reader, are invited to review the content of this document and communicate your comments and ideas for additional details that may serve the industry to the appropriate trade associations or technical societies. In this way, the infrastructure necessary to implement this new philosophy for packaging will make its way forward.

Thanks to Chairman Phil Marcoux, ISHM and IPC are in the process of a detailed update program. It is expected that the result of this effort will culminate in a hardbound version that will provide an excellent reference tool. IPC will also consider future review of the MC-790 as more information becomes available. You are invited to participate in any of the revision or update processes.

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

Table of Contents

Section 1 Technology Overview
1.0 INTRODUCTION 1
1.1 Multichip Module Classification 3
1.2 Materials Data 6
1.3 Advantages and Disadvantages of Multichip Modules 6
1.4 Design Cycle 6
1.5 Assembly Options 10
1.6 Substrate (Interconnect Carrier) 11
1.7 Thermal Issue 11

Section 2 Multichip Module General Design Considerations
2.0 INTRODUCTION 13
2.1 Materials 13
2.2 Components 19
2.3 Multichip Module Design Layout 22
2.4 Packaging and Higher-Level Assembly 26
2.5 Electrical Design Guidelines 29

Section 3 MCM-C Design Considerations (Ceramic/Glass Based Materials)
3.0 INTRODUCTION 32
3.1 Layout 32
3.2 Conductor Pattern 32
3.3 Conductor Routing 32
3.4 Land Patterns 35
3.5 Wire Bonds 35
3.6 Vias 36
3.7 Resistors 36
3.8 Substrate Requirements 40

Section 4 MCM-L Design Considerations (Organic Based Materials)
4.0 INTRODUCTION 44
4.1 Design Layout 44
4.2 Conductor Pattern 45
4.3 Land Pattern 49
4.4 Holes 54
4.5 Resistors 56
4.6 Substrate Materials 57

Section 5 MCM-D Design Considerations (Deposited Dielectric Films on Various Base Materials)
5.0 INTRODUCTION 61
5.1 Layout 61
5.2 Conductor Pattern 62
5.3 Conductor Routing 62
5.4 Land Patterns 63
5.5 Vias 63
5.6 Resistors 63
5.7 Integrated Circuit Die (Chips) 68
5.8 Dielectrics 68
5.9 Substrates 68

Section 6 Wire Bond Technology
6.0 INTRODUCTION 73
6.1 Design for Wire Bonding 73
6.2 Components 74
6.3 Wire Bonding 75

Section 7 Tape Automated Bonding (TAB) Technology
7.0 INTRODUCTION 80
7.1 Inner Lead Bonding (ILB) 80
7.2 Outer Lead Bonding (OLB) 81

Section 8 Flip Chip Bonding Attachment Techniques
8.0 INTRODUCTION 87
8.1 Design for Flip Chip 87
8.2 Thermal Considerations 88
8.3 Interconnection 89
8.4 Alternative to Flip-Chips 89

Section 9 Design for Test, Modification, and Repair
9.0 INTRODUCTION 91
9.1 Design for Test 91
9.2 Design for Modification and Repair 92
9.3 Minimizing Rework/Repair 93

Section 10 Environmental Protection
10.0 INTRODUCTION 94
10.1 Conformal Coating 94
10.2 Encapsulation 96
10.3 Plastic Packaging 97
10.4 Laminated Modules (Smart Cards) 98
10.5 Metal Enclosures 98

Section 11 Reliability Engineering Guidelines
11.0 INTRODUCTION 104
11.1 Reliability Data 104
11.2 Reliability Definitions 104
11.3 Constant Failure Rate 105
11.4 Failure Rate of Multiple-Element Systems 106
11.5 Accelerated Life Testing 106

11.6 Failure Mechanisms in MCMs 107
11.7 Construction Analysis 108
11.8 Other Reliability Tests 108

Section 12 Applications

12.0 INTRODUCTION 109
12.1 Current Applications 109

Section 13 Reference Documents

13.0 REFERENCE DOCUMENTS 120
13.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC) 120
13.2 Electronic Industries Association (EIA) .. 120
13.3 Department of Defense (DoD) 121
13.4 American National Standards Institute (ANSI) 121
13.5 American Society for Testing Materials (ASTM) 121

Section 14 Terms and Definitions

14.0 Terms and Definitions 122

Figures

Figure 1–1 Typical pin count per integrated circuit 2
Figure 1–2 Forecast system clock speed increase 1987–92 3
Figure 1–3 Price/density relationships 4
Figure 1–4 Interconnection density vs. line technology 5
Figure 1–5 Expansion of Packaging Materials 8
Figure 1–6 Conductivity of Packaging Materials 8
Figure 1–7 Methods of 3D die integration 10
Figure 1–8 Eight-Layer MCM-L 12
Figure 2–1 Resistor paste stability 23
Figure 2–2 Inductance/wire length relationships 23
Figure 2–3 Example of total thermal resistance calculation 31
Figure 2–4 Thermal resistance during heat spreading ... 31
Figure 3–1 Sequence of events for MCM layout 32
Figure 3–2 Final configuration of MCM-C using wire bonding 33
Figure 3–3 Orientation for conductor-resistor patterns 34
Figure 3–4 Land and conductor geometries 34
Figure 3–5 Conductor interconnects external to the dielectric 35
Figure 3–6 Spacing between adjacent conductors running over a dielectric edge 35
Figure 3–7 Preferred parallel conductor design running over a dielectric edge 35
Figure 3–8 Overlap between top and bottom conductors over a dielectric edge 35
Figure 3–9 Examples of die bonds and wire bonds in multilayer designs 35
Figure 3–10 Nominal dimensions for chip mounting lands (see Table 3–2) 37
Figure 3–11 Wire bond land sizes and locations 38
Figure 3–12 Nominal via window dimensions 38
Figure 3–13 Illustration of various multilayer via designs .. 38
Figure 3–14 Routing conductors through multiple dielectric layers 39
Figure 3–15 Use of a blind through-hole land 39
Figure 3–16 Preferred thick-film resistor configurations 39
Figure 3–17 Thick-film screened resistor size and location 39
Figure 3–18 Thick-film resistor length/width/power 40
Figure 3–19 Preferred layout for matched thick-film resistors 40
Figure 3–20 Preferred layout for trimming of thick-film resistors 41
Figure 4–1 Etched conductor characteristics 46
Figure 4–2 Conductor thickness and width for internal and external layers (inches) 48
Figure 4–3 Conductor spacing optimization between lands 50
Figure 4–4 Large conductive layers with isothermal conductors 50
Figure 4–5 Examples of modified land shapes 51
Figure 4–6 External annular ring 51
Figure 4–7 Internal annular ring 51
Figure 4–8 Typical thermal relief in planes 52
Figure 4–9 Clearance area in planes, mm [in] conductors 52
Figure 4–10 Solder resist windows 53
Figure 4–11 Chip resistor 53
Figure 4–12 Land patterns for rectangular chip resistors, mm [in] 54
Figure 4–13 Solder fillet formation 54
Figure 4–14 Etched resistor shape 57
Figure 4–15 Dielectric layer thickness measurement 59
Figure 5–1 Sequence of events for MCM layout 62
Figure 5–2 Orientation for conductor-resistor patterns 62
Figure 5–3 Land and conductor geometries 63
Figure 5–4 Nominal thin-film conductor and land dimensions (see Table 5-3) 64
Figure 5–5 Nominal dimensions for chip mounting lands (see Table 5-4) 65
Figure 5–6 Exit land/alignment/misalignment considerations 65
Figure 5–7 Recommended approach for identifying exit leads/pins for standard packages 66
Figure 5–8 Nominal thin-film resistor design dimension (see Table 5-5) 67
Figure 5–9 Nominal thin-film resistor dimensions showing resistor-to-conductor spacing (see Table 5-5) 67
Figure 5–10 SiO_2 on silicon MCM-D substrate 69
Figure 5–11 BCB on silicon MCM-D 70

Figure 5–12 Polyimide MCM-D on copper (or aluminum) base ... 70
Figure 5–13 Polyimide MCM-D on ceramic ... 71
Figure 6–1 Wire bonding guidelines ... 73
Figure 6–2 Ball bonding layout features ... 73
Figure 6–3 Mechanics of ultrasonic wire bonding ... 77
Figure 6–4 Hydrogen torch flame-off shown with electrostatic ball for application ... 78
Figure 6–5 Typical ball bonding cycle ... 79
Figure 7–1 Excising of leaded die from tape carrier ... 80
Figure 7–2 TAB mounting options ... 82
Figure 7–3 Solder reflow ... 82
Figure 7–4 Single point TAB bonding wedge ... 83
Figure 7–5 Laser augmented thermosonic TAB bonding tool ... 84
Figure 7–6 Trapezoidal trench TAB lead bonding tool ... 84
Figure 7–7 Deep narrow groove waffle pattern TAB bonding tool tip ... 85
Figure 7–8 In-line and cross TAB lead bonding tool ... 86
Figure 7–9 In-line and cross TAB lead bonding tool ... 86
Figure 8–1 Typical flip chip ... 87
Figure 8–2 The IBM ‘‘Thermal Conduction Module’’ ... 88
Figure 8–3 Beam leaded IC wafer ... 89
Figure 8–4 Individual beam-leaded IC ... 89
Figure 8–5 Beams welded to substrate ... 89
Figure 8–6 Micro SMT package–cross sectional view ... 90
Figure 8–7 Micro SMT package–added metallized cap ... 90
Figure 10–1 Plastic molded multichip ... 100
Figure 10–2 Multichip IC exploded view ... 100
Figure 10–3 Matrix of substrates ... 101
Figure 11–1 Exponential failure rate distribution ... 105
Figure 11–2 Typical ‘‘bathtub’’ failure curve for electrical components ... 105
Figure 12–1 Technology life chart ... 109
Figure 12–2 DEC multichip module ... 110
Figure 12–3 Dow ... 112
Figure 12–4 MCC ... 112
Figure 12–5 Unistructure—A flexible leaded component packs two megabytes of memory into the area of one 256K chip. ... 113
Figure 12–6 Advanced packaging system ... 113
Figure 12–7 Memory module—NEC ... 114
Figure 12–8 AT&T ... 114
Figure 12–9 Prototype fiber optic transmitter ... 114
Figure 12–10 Z-systems. MCM designed for avionics computer, with diffused components in silicon substrate and PGA package. ... 115
Figure 12–11 Polycon silicon-on-silicon MCM designed for military application, using BCB dielectric and aluminum metalization. ... 115
Figure 12–12 Simple MCM utilizing four chips and TAB technology. Package sealing is accomplished with seam or laser welding. ... 115
Figure 12–13 Rockwell 5-million-instruction-per-second dual processor on a silicon substrate, 25-micrometer lines, and four metalization layers. ... 115
Figure 12–14 An example of an inexpensive MCM-L ... 116
Figure 12–15 An example of an MCM-C, which is termed by some ‘‘a conventional thick-film hybrid’’ — Fujitsu ... 116
Figure 12–16 ADC574P converter ... 117
Figure 12–17 Advanced packaging systems ... 118
Figure 12–18 T.I. ... 118
Figure 12–19 Irvine Sensors Corp. ... 119

Tables

Table 1–1 Characterization of Selected MCM Market Segments ... 1
Table 1–2 Multichip Interconnect Attributes by Classification Multichip Modules ... 7
Table 1–3 General Multichip Material Properties ... 7
Table 1–4 End Use Environments ... 9
Table 2–1 Conductor System Attributes ... 15
Table 2–2 Film Resistor Characteristics ... 16
Table 2–3 Dielectric Comparisons ... 16
Table 2–4 Typical Solder Systems ... 17
Table 2–5 Properties of Adhesives ... 19
Table 2–6 Derating Guidelines ... 21
Table 2–7 Ceramic As-Fired Dimensions ... 25
Table 2–8 Dimensional Tolerance ... 25
Table 2–9 Typical Materials Thermal Conductivity ... 27
Table 3–1 Dimensional Constraints for Thick-Film Conductors and Lands ... 34
Table 3–2 Chip Mounting Lands ... 36
Table 3–3 Interconnection Technique Substrate Temperatures ... 38
Table 3–4 Nonphysical Substrate Selection Criteria ... 41
Table 3–5 Physical Characteristics of Substrates ... 42
Table 4–1 Typical Values to Be Added or Subtracted from the Desired Nominal Conductor Width ... 47
Table 4–2 Electrical Conductor Spacing ... 49
Table 4–3 Conductor Width Tolerances mm [in] ... 49
Table 4–4 Minimum Standard Fabrication Allowance ... 50
Table 4–5 Annular Rings (Minimum) ... 51
Table 4–6 Minimum Hole Location Tolerances ... 54
Table 4–7 Plated-Through Hole Aspect Ratios ... 55
Table 4–8 Minimum Plated-Through Hole ... 55
Table 4–9 Minimum Drilled Hole Size ... 55
Table 4–10 Minimum Drilled Hole Size for Buried Vias ... 56
Table 4–11 Minimum Drilled Hole Size ... 56
Table 4–12 Clad Laminate Maximum Operating Temperatures ... 58
Table 4–13 Guide to Laminate Thickness ... 59

Table 4–14 Copper Foil/Film Requirements 60
Table 4–15 Metal Core Substrates 60
Table 5–1 MCM-D Material and Conductor Fabrication Options 61
Table 5–2 Electrical Characteristics.................................. 62
Table 5–3 Dimensional Constraints for Thin-film Conductors and Lands..................................... 63
Table 5–4 Chip Mounting Lands....................................... 64
Table 5–5 Nominal Dimensions for Thin-Film Resistors ... 66
Table 5–6 Properties of Dielectric Substrate Materials 69
Table 6–1 Aluminum and Gold Wire Sizes and Ratings ... 74
Table 6–2 Wire Bonding Comparisons 76
Table 9–1 Typical Functional Test Status 92
Table 10–1 Coating Thickness.. 94
Table 10–2 Thermal Properties of Encapsulating................ 97
Table 10–3 Mechanical Properties of Encapsulating and Coating Materials 98
Table 10–4 Electrical Properties of Encapsulating and Coating Materials...................................... 99
Table 10–5 Sealing Method Hermeticity............................ 101
Table 10–6 Mechanical Properties of Enclosure Materials... 102
Table 10–7 Thermal Properties of Enclosure Materials 102
Table 10–8 Physical Properties of Materials 102
Table 10–9 Viable Package Materials 103
Table 11–1 MCM Circuit Element Base Failure Rates (%/1000 hr) 107
Table 11–2 Statistical Factors for a 90% Lower Confidence Limit 107
Table 11–3 Comparative Failure Rates for Various Bonding Techniques (%/1000 hr)................... 108
Table 12–1 Chip-mounting Specs of Four Major Mainframes 111

Foreword

The developments over the past 8–10 years reflected in this document have resulted in a variety of new materials, structures, and interconnect methodologies. This ‘‘smorgasbord’’ of MCM technology is shown in Figure F–1. The selection of the elements that make up a structure to meet the systems level needs initially appears to be a difficult problem in the current environment. However, the choices available should be viewed as part of the beauty of this technology.

Initially, system requirements should be developed on a hierarchal basis. A simple high-level breakdown of a system is shown in Figure F–2. System requirements for cost, reliability and performance must be clearly understood in the context of the application and system environment. In this way, requirements are logically developed and an understanding of their interrelationships can be inferred or modeled.

The complexity of an MCM structure demands the development of requirements for the structure from system level considerations. The next step is to work with system partitioning concepts that make sense in terms of system cost and performance. For example, the designer should question whether it makes sense to use single chip packaging, manufacture a single module an a 10.2 cm [4 in] substrate, or four modules on a 5.1 cm [2 in] substrate. Perhaps the answer is the latter when cost is compared to performance requirements for the system. This process of system partitioning may require an iteration or two following the initial technology selection in order to develop accurate costs as the process of developing a module-based system progresses.

Following the development of system requirements and partitioning, a specific module can be synthesized which meets the systems needs through a balancing of module attributes related to cost, performance, and reliability. At this point, IPC-MC-790 can become a useful tool in understanding the various module options and the relationship of these attributes to a potential structure. this is done through the use of comparisons of interconnect and substrate properties, manufacturing costs and other criteria for MCM-L, MCM-D, and MCM-C as defined in section 1 of the document. Table F–1 shows these various module attributes and their relative weights for these general categories.

The selection of a general category is initially made through comparing system requirements to module attributes. This should be done in a quantitative fashion

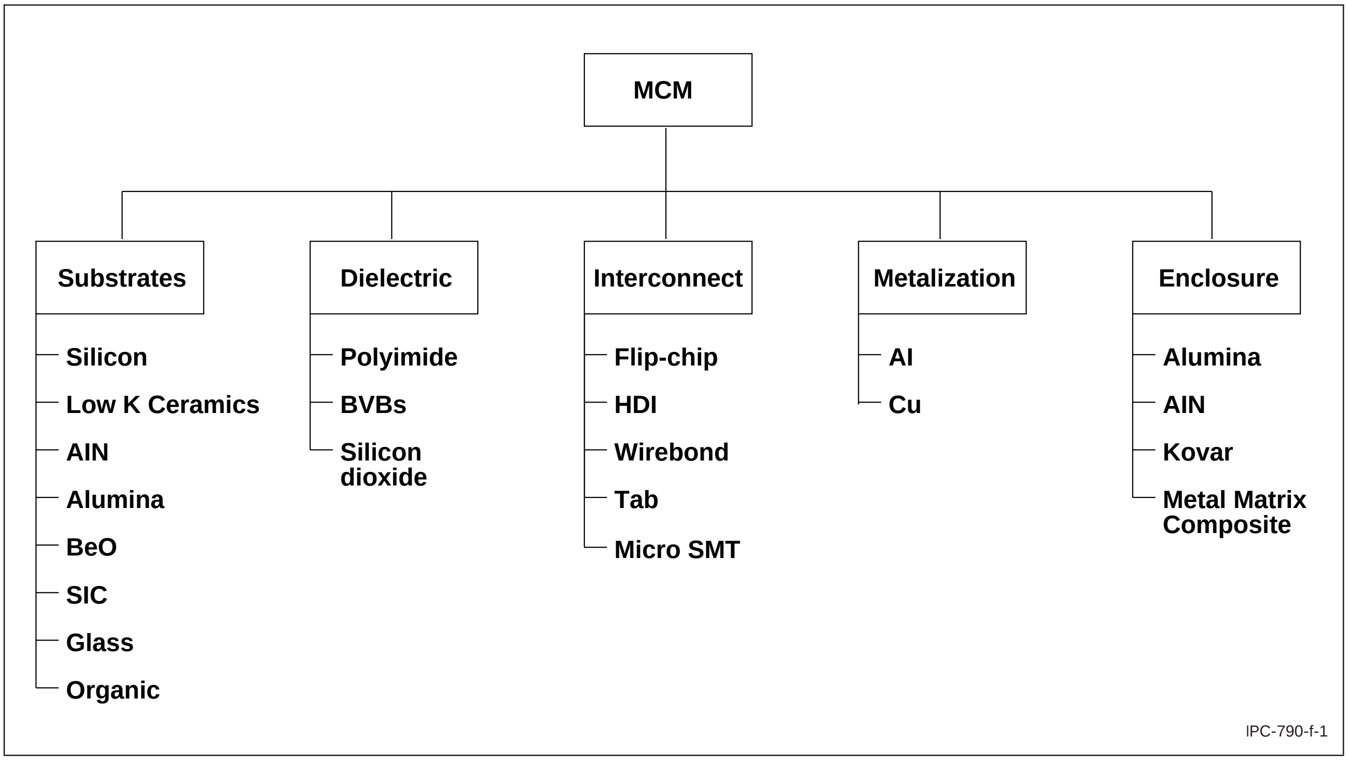

Figure F–1 MCM options

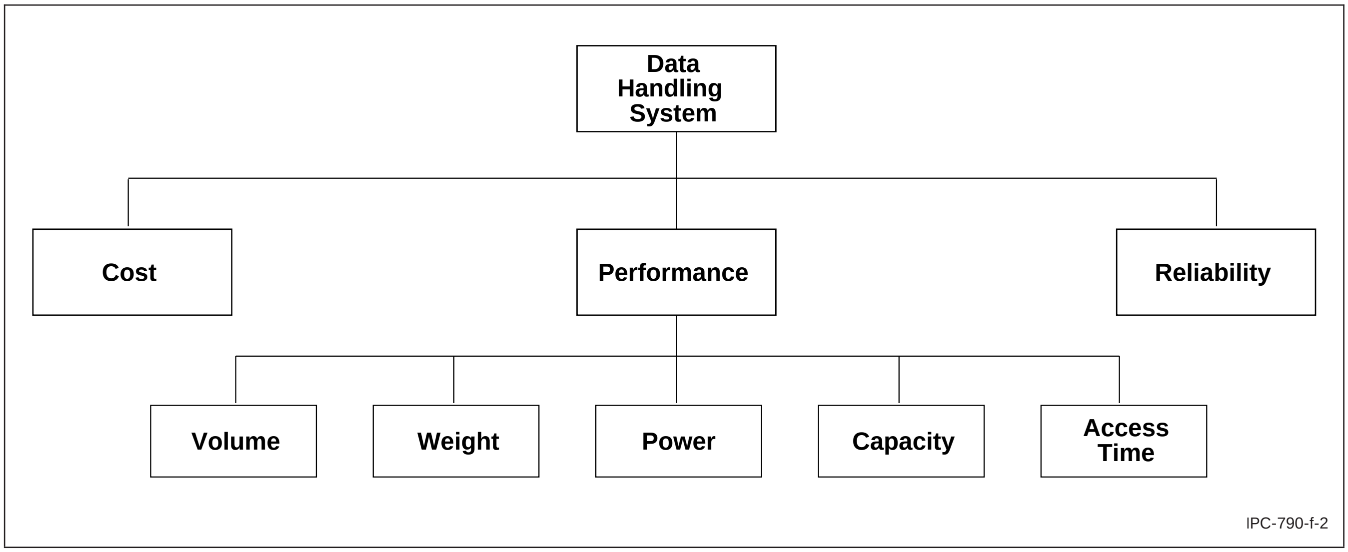

Figure F–2 Electronic system packaging hierarchy

Table F–1 Multichip Module Parameter Complexities

Parameter	Thick-film MCM-Circuits	Thin-film MCM-D circuits	MCM-L circuits
Performance	Medium	High	Medium
Design flexibility, digital	Medium	High	Medium
Analog	High	High	Low
Plastics	Low	Low	Medium
Power dissipation	High	High	Low
Frequency limit	Medium	High	Medium
Voltage Swing	Medium	Medium	Low
Size	Small	Smallest	Small
Package density	Medium	High	Medium
Reliability	High	High	High
Circuit development time (prior to prototype)	1- 2 month	2-3 month	1 month
1:1 design transfer from bench	Yes	Yes	Yes
Turnaround time for design change	2 weeks	4 weeks	2 weeks
Part cost, low quantity	High	Impractical	Medium
High quantity	Medium	Medium	Low
Cost of developing one circuit	Medium	High	Low
Capital outlay	Low	Medium	Low
Production setup and tooling costs	Low	Medium	Low

Section One
Technology Overview

1.0 INTRODUCTION

Electronic packaging continues to focus on the ever increasing need for higher electrical speed and higher interconnection density. In existing packaging concepts using printed board assemblies and individually packaged integrated circuits, performance may be sacrificed because of the signal path length needed to interconnect the semiconductors contained in the various packages.

In contrast to the above, improvements in speed, reliability, and density accompany the use of unpackaged integrated circuit chips on fine line interconnection substrates. A functional, packaged module exhibiting these attributes will be called a ‘‘Multichip Module’’ (MCM), and is the subject of this document. A variety of materials and techniques may be employed in creating an MCM. In section 2.0, various approaches are categorized, and the reader is led through a decision-making process to assist in the selection of the proper MCM technology for a given set of technical requirements. Later sections provide detailed information regarding each technology type.

The balance of this introduction discusses the drivers toward use of MCM’s, and the type of problems which may be resolved via MCM technology. The following key point should be assimilated: total cost is minimized when the best technological choice is made for packaging and interconnection.

There is an important drive to increase density in order to make the product smaller. Space restrictions exist in end-use environments ranging from aircraft to laptop computers and hand-held TVs. Another driver is the potential cost reduction available from reduction in material usage, or even from less real estate being employed, as may be the case in telephone exchanges. Table 1–1 shows MCM selection according to various market segments.

The heart of electronic performance capability is the integrated circuit and the increasing levels of integration being achieved. To capitalize on IC capability, we have already seen the move to surface mount packages with fine pitch I/O. For the same reason, direct attach, such as TAB, Flip-Chip, and Chip-On-Board, are also becoming important interconnection techniques.

Observations indicate that when single I/C chip mounting is used, a trend exists toward one package per 6.45 sq. cm. [1 sq. in] of substrate compared to 0.2 to 0.5 per 6.45 per sq. cm. [1 sq. in] for packaged I/Cs. Under these circumstances, the I/O count of the package becomes the major determinant of the interconnect density required. Figure 1–1 shows just how these individual IC chip I/Os are expected to increase.

While not totally separate from the density considerations, the issue of system speed presents some major challenges

Table 1–1 Characterization of Selected MCM Market Segments

Segment	Drivers	Personality	Price Elasticity
Electronic T&M	Precision	Industrial	Moderate
Logic Analysis	Precision, Miniaturization	Industrial	High
Global Positioning & Surveillance	Miniaturization Miniaturization	Military Commercial	Moderate High
Communications Satellites	Miniaturization	Commercial	Low
Telephone	Miniaturization	Commercial	Very High
Smart Sensors Weapons Systems Automotive Control Robotics	Miniaturization Miniaturization Miniaturization	Military Consumer Industrial	Moderate, Low Very High Moderate
Computing Systems Strategic/Tactical Mgmt. Info. Sys. Scientific Models	Speed Speed Speed	Military Commercial Industrial Academic Government	Low Moderate Low
Image Processing	Speed, Miniaturization	Industrial	Moderate
Engineering Workstations	Speed	Industrial	Very High
Laptops/Notebooks	Miniaturization	Consumer	Very High