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## Terms and Definitions, Test Methods, and Design Examples for Build-Up/High Density Interconnect (HDI) Printed Wiring Boards

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# Terms and Definitions, Test Methods, and Design Examples for Build-Up/High Density Interconnect (HDI) Printed Wiring Boards

## 1 SCOPE

This standard specifies printed wiring boards (PWBs) manufactured by the build-up process used primarily for electronic equipment (hereinafter build-up/high density interconnect (HDI) PWBs). The build-up/HDI PWB, as referred to herein, is defined as the printed board that is built up progressively with the conductor layers and insulating layers using techniques such as plating and printing. The build-up/HDI PWBs include substrates for semiconductor packages.

## 2 APPLICABLE DOCUMENTS

The following are documents referenced in this standard.

**JIS 8 7729** Erichsen Cupping Testers

**JIS C 0010** Environmental Testing Part 1: General and Guidance

**JIS C 5603** Terms and Definitions for Printed Circuits

**JIS K 5400** Testing Methods for Paints

**JIS K 7100** Standard Atmospheres for Conditioning and Testing of Plastics

**JIS K 7127** Testing Method for Tensile Properties of Plastic Films and Sheets

**JIS K 7209** Testing Methods for Water and Boiling Water Absorption of Plastics

## 3 DEFINITIONS OF STRUCTURES AND TERMS

The structures and terms used in this document are defined as follows.

**3.1 Structures** Names of structures and parts of the build-up printed boards are defined in Figure 3-1. For the names other than those defined herein, see the related standards (i.e., JIS C 5603). Other examples of structural elements and parts are shown in Figure 3-2, Figure 3-3, and Figure 3-4.

### 3.2 Terms and definitions

#### 3.2.1 General

**3.2.2 Planer Board** A substrate on which bare chips and surface- and insertion-mount components are mounted. After being mounted with these components, the substrate is no longer heated for mounting on other planar boards. It generally includes motherboards, daughter cards, etc.

**3.2.3 Module Board** A substrate on which bare chips and surface-mount components are mounted. After being mounted with these components, the substrate is expected to be mounted on other planar boards with heat.

### 3.3 Design

**3.3.1 Build-Up Via/Microvia** The general term for vias in build-up layers of build-up/HDI PWBs. It is a structure interconnecting electrically top and bottom conductors with a hole formed in the insulating layer and made conductive by plating or conductive paste printing.

**3.3.2 Conformal Via** A type of build-up via in which the conductor layer of a uniform thickness is formed conforming to the shape of a hole in the insulating layer.

**3.3.3 Filled Via** A type of build-up via in which the interior of the via is filled with a conductive material (see Figure 3-5).

**3.3.4 Stacked Via** A via formed by stacking one or more build-up vias/microvias on a build-up via/microvia that provides an interlayer connection between three or more conductive layers (see Figure 3-6).

**3.3.5 Skip Via** A via that directly connects conductive layers of build-up/HDI layers that are not adjacent with each other.

**3.3.6 Hole-Plugged Base Via** A plated-through hole (PTH) that is formed on the base of a build-up/HDI printed base-via board and is filled with a filler.

**3.3.7 Via Top Land** A land on the external layer side of a via (see Figure 3-2).

**3.3.8 Via Bottom Land** A land on the internal layer side of a via (see Figure 3-2).

**3.3.9 Landless Via** A via in which the land diameter is designed to be less than or equal to the via diameter (see Figure 3-7).