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*The Institute for  
Interconnecting  
and Packaging  
Electronic Circuits*

# IPC-D-859

## Design Standard for Thick Film Multilayer Hybrid Circuits

### **ANSI/IPC-D-859**

Original Publication  
December 1989

A standard developed by the Institute for Interconnecting  
and Packaging Electronic Circuits

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# Design Standard for Thick Film Multilayer Hybrid Circuits

## 1.0 SCOPE

This standard covers the requirements and considerations for the design of multilayer hybrid circuits based on industry manufacturing capabilities.

**1.1 Purpose** The purpose of this standard is to establish rules, principles, and other considerations for mechanical, electrical, and producible properties which the designer can use to select design features, and properties that will result in a multilayer hybrid circuit that will meet performance and cost requirements.

**1.2 Classification** When appropriate, this standard will provide three design complexity classes of features, tolerances, or measurements which reflect progressive increases in sophistication of tooling, materials, or processing and, therefore, progressive increases in cost. These classes are: A) Simple, B) Moderate, and C) Complex. The use of one class for a specific feature does not mean that other features must be of the same class. Selection should be based on the minimum need. In the event of conflict between the design requirements and the classes defined herein, the former shall take precedence and be reflected on the master drawing.

Design requirements such as precision, performance, and conductive pattern density determine class. Class definitions identify the precision needed to meet design/performance requirements of the hybrid circuit.

Classification of design complexity requirements should not be confused with the performance classification of end-item use, as referenced in other IPC documentation, such as IPC-HM-860, which refers to Class 1—consumer products; Class 2—general industrial; and Class 3—high reliability equipment types. The need to apply certain design concepts should depend on the complexity and precision required to produce a particular hybrid circuit. Any design class for any circuit characteristic may be applied to any of the end-product equipment categories and the classes described from each, as required. Therefore, a consumer product designated as Class 1 could require Class A, B or C design complexity for different attributes of the circuit.

**1.2.1 Circuit Type** The multilayer hybrid circuit types defined in the IPC-HM-860 include both refractory and nonrefractory metal co-fired types (Type I) and thick film and thin film inorganic types (Type II).

This standard will address only Type II(a), thick film inorganic multilayer hybrid circuits.

**1.3 Presentation** All dimensions and tolerances are expressed in metric [and inches, shown in brackets], and are not direct conversions. Users should employ a single system, and not intermix millimeters and inches. Reference information is shown in parentheses ( ).

## 2.0 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect, form a part of this document to the extent specified herein.

### 2.1 IPC

**IPC-T-50** Terms and Definitions

**IPC-D-300** Dimensions and Tolerance for Printed Wiring Applications

**IPC-D-310** Guidelines for Artwork Generation and Measurement Techniques

**IPC-D-325** End-Product Documentation for Printed Wiring Boards

**IPC-D-350** End Product Description in Numeric Form

**IPC-D-351** Printed Wiring Board Documentation in Digital Form

**IPC-D-352** Electronic Design Data Base Description for Printed Boards

**IPC-D-353** Automatic Test Information Description in Digital Form

**IPC-D-354** Library Format Description for Printed Board Digital Data Bases

**IPC-TM-650** Test Methods Manual

**IPC-SM-780** Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

**IPC-SM-782** Surface Mount Land Patterns (Configurations and Design Rules)

**IPC-CC-830** Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

**IPC-SM-840** Permanent Polymer Coating (Solder Mask) for Printed Wiring Boards

**IPC-HM-855** Microelectronics Design Guide

**IPC-HM-860** Specification for Multilayer Hybrid Circuits**2.2 Government Documents****2.2.1 Military****MIL-C-14450** Copper Plating (Electro-deposited)**MIL-M-38510** General Specification for Microelectronics**MIL-G-45204** Gold Plating (Electro-deposited)**MIL-P-81728** Plating, Tin-Lead (Electro-deposited)**MIL-STD-883** Test Methods and Procedures for Microelectronics**2.2.2 Federal****QQ-N-290** Nickel Plating (Electro-deposited)**QQ-S-571** Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy**2.3 Other Publications****2.3.1 ASTM****F 72** Gold Wire for Semiconductor Lead Bonding**F 487** Fine Aluminum—1% Silicon Wire for Semiconductor Lead Bonding**F 638** Fine Aluminum—1% Magnesium Wire for Semiconductor Lead Bonding**2.3.2 EIA****JEDEC Publication 95** Registered and Standard Outlines for Solid State Products**3.0 DESIGN CONSIDERATIONS**

The information contained in this document describes general and specific requirements for the design of thick film multilayer hybrid circuits intended to meet the performance and end product requirements of IPC- HM-860.

The success or failure of a hybrid design depends on many interrelated considerations. The effect of the following parameters on the design should be considered:

1. Equipment environmental conditions, such as ambient temperature, heat generated by the components, and ventilation.
2. Maintenance philosophy during the service life of the equipment, especially with respect to component placement that affects component accessibility.
3. Spacing between circuits particularly "mother board/

daughter board" designs that might affect placement on interconnecting lead frames.

4. Testing/fault location requirements that might affect component placement, conductor routing, connector contract allocations, etc.
5. If an assembly is to be repairable, consideration must be given to component/circuit density and the selection of board/conformal coating materials. In general, design should promote ease of package repair which must be initiated by delidding.

**3.1 Terms and Definitions** Definitions of all terms used herein shall be as specified in IPC-T-50 and as follows.

**Abrasive trimming** Trimming a film resistor to its nominal value by notching resistor with a finely adjusted stream of an abrasive material, such as aluminum oxide, directly against the resistor surface.

**Active trim** Trimming of a circuit element (usually a resistor) in a circuit that is electrically activated and operating to obtain a specified functional output for the circuit (see Functional trimming).

**Add-on component** Discrete or integrated prepackaged or chip components that are attached to a film circuit to complete the circuit functions.

**Analog circuits** Circuits that provide a continuous (vs. discontinuous) relationship between the input and output.

**Aspect ratio** The ratio between the length of a film resistor and its width; equal to the number of squares of the resistor.

**Back bonding** Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of back bonding is face down bonding.

**Back mounting** See *Back bonding*.

**Ball bond** A bond formed when a ball shaped end interconnecting wire is deformed by thermo-compression against a metallized land; also called "a nail head bond" from the appearance of the flattened ball.

**Beam lead** A long structural member not supported everywhere along its length and subject to the forces of flexure, one end of which is permanently attached to a chip device and the other end intended to be bonded to another material, providing an electrical interconnection or mechanical support or both.

**Beam lead device** An active or passive chip component possessing beam leads as its primary interconnection and mechanical attachment means to a substrate.

**Bond** An interconnection which performs a permanent electrical and/or mechanical function.

**Bond deformation** The change in the form of the lead produced by the bonding tool, causing plastic flow, in making the bond.