ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

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PWB Assembly Process Simulation for Evaluation of Electronic Components (Preconditioning IC Components)

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1.0 SCOPE

This document describes manufacturing process simulations for use with applicable component specifications to assure that electronic components can meet expected reliability requirements after exposure to assembly factory processes. It is not intended as an assembly production specification or a stand alone qualification document. The procedure consists of a set of assembly process simulations which can be performed by either the component user or manufacturer prior to reliability testing as specified in the applicable component qualification and reliability monitoring documents. The simulations include alternative conditions depending on the component type, physical characteristics and anticipated use.

It is expected that a single component would be evaluated for a subset of the alternative conditions. For example, large integrated circuit (IC) packages (e.g., PQFP's) might be qualified utilizing the lower of two reflow temperature ranges while smaller packages, which typically become much hotter during infrared or convection reflow, might be qualified for the higher range. Similarly, components with physical characteristics which prohibit total immersion cleaning would not be evaluated for this type of cleaning process.

Unless otherwise specified, this document applies to both surface-mount (SM) reflowed components and through-hole (TH) discrete and IC components, which are wave soldered or reflowed. For wave solder of SM ICs, user and supplier should work together to identify appropriate procedures. The document is intended to complement other industry documents, such as JESD22-A113 and IPC-SM-786 which define moisture sensitivity levels and surface mount ICs for a specific set of process conditions.

2.0 APPLICABLE DOCUMENTS

2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)[1]

IPC-AC-62 Aqueous Cleaning Handbook

1PC-OI-645 Standard for Visual Optical Inspection Aids

IPC-TM-650 Test Method Manual

TM-2.6.9.1 Test to Determine Sensitivity of Electronic Components to Ultrasonic Energy

TM-2.6.20 Assessment of Plastic Encapsulated Electronic Components for Susceptibility to Moisture/Reflow Induced Damage

IPC-SM-786 Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs

IPC-SM-817 General Requirements for Dielectric Surface Mounting Adhesives

2.2 Joint Industry Standards[1,2]

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Wires

ANSI-EIA-625 Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

2.3 Electronic Industries Association[2]

EIA-541 Packaging Material Standards for ESD Sensitive Items

JESD22-A113 Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing

JESD 42 Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

2.4 Military[3]

MIL-STD-1686 Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment (Excluding Electrically Initiated Explosive Devices)

MIL-HDBK-263 Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

MIL-HDBK-773 Electrostatic Discharge Protective Packaging

3.0 TERMS AND DEFINITIONS

MET = Manufacturer's Exposure Time: The compensation factor which accounts for the time after bake that the component manufacturer requires to process the components prior to bag seal. It also includes a default amount of time to account for shipping and handling.

1. Application for copies should be addressed to: IPC, 2215 Sanders Road, Northbrook, IL 60062.
2. Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.
3. DoD Standardization Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094