Generic Requirements for Surface Mount Design and Land Pattern Standard

Developed by the Surface Mount Land Patterns Subcommittee (1-13) of the Printed Board Design Committee (1-10) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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# Table of Contents

1 SCOPE ................................................................. 1
   1.1 Purpose ..................................................... 1
   1.2 Documentation Hierarchy ................................. 1
   1.2.1 Component and Land Pattern Family Structure .......... 1
   1.3 Performance Classification ............................. 2
   1.3.1 Productibility Levels ................................ 2
   1.4 Land Pattern Determination ............................. 2
   1.5 Terms and Definitions ................................... 3
   1.6 Revision Level Changes ................................. 5

2 APPLICABLE DOCUMENTS ........................................... 5
   2.1 IPC ....................................................... 5
   2.2 Electronic Industries Association ....................... 6
   2.3 Joint Industry Standards (IPC) ......................... 6
   2.4 International Electrotechnical Commission .......... 6
   2.5 Joint Electron Device Engineering Council (JEDEC) ... 6

3 DESIGN REQUIREMENTS ............................................ 6
   3.1 Dimensioning Systems ................................... 6
   3.1.1 Component Tolerancing ............................... 6
   3.1.2 Land Tolerancing ..................................... 9
   3.1.3 Fabrication Allowances ................................ 10
   3.1.4 Assembly Tolerancing ................................ 10
   3.2 Design Productibility ..................................... 20
   3.2.1 SMT Land Pattern ...................................... 20
   3.2.2 Standard Component Selection ....................... 20
   3.2.3 Circuit Substrate Development ....................... 20
   3.2.4 Assembly Considerations ............................. 20
   3.2.5 Provision for Automated Test ....................... 20
   3.2.6 Documentation for SMT ............................... 20
   3.3 Environmental Constraints ............................. 20
   3.3.1 Moisture Sensitive Components ..................... 20
   3.3.2 End-Use Environment Considerations ............... 20
   3.4 Design Rules ............................................. 22
   3.4.1 Component Spacing .................................... 22
   3.4.2 Single-and Double-Sided Board Assembly ........... 22
   3.4.3 Component Stand-Off Height for Cleaning .......... 24
   3.4.4 Fiducial Marks ........................................ 24
   3.4.5 Conductors ............................................ 26
   3.4.6 Via Guidelines ........................................ 26
   3.4.7 Standard Printed Board Fabrication Allowances ...... 29
   3.4.8 Panelization ........................................... 31

3.5 Outer Layer Surface Finishes .............................. 32
   3.5.1 Solder Mask Finishes ................................ 32
   3.5.2 Solder Mask Clearances .............................. 32
   3.5.3 Land Pattern Surface Finishes ....................... 34

4 COMPONENT QUALITY VALIDATION .............................. 36
   4.1 Validation Techniques ................................... 36

5 TESTABILITY ....................................................... 37
   5.1 Board and Assembly Test ................................. 37
   5.1.1 Bare-Board Test ........................................ 37
   5.1.2 Assembled Board Test ................................ 37
   5.2 Nodal Access ............................................. 37
   5.2.1 Test Philosophy ........................................ 37
   5.2.2 Test Strategy for Bare Boards ....................... 38
   5.3 Full Nodal Access for Assembled Board ............... 38
   5.3.1 In-Circuit Test Accommodation ...................... 39
   5.3.2 Multi-Probe Testing ................................... 39
   5.4 Limited Nodal Access ..................................... 39
   5.5 No Nodal Access .......................................... 39
   5.6 Clam-Shell Fixtures Impact ............................. 39
   5.7 Printed Board Test Characteristics ..................... 39
   5.7.1 Test Land Pattern Spacing ........................... 39
   5.7.2 Test Land Size and Shape ........................... 39
   5.7.3 Design for Test Parameters .......................... 39

6 PRINTED BOARD STRUCTURE TYPES ......................... 41
   6.1 General Considerations .................................. 41
   6.1.1 Categories ............................................. 41
   6.1.2 Thermal Expansion Mismatch ......................... 41
   6.2 Organic-Base Material .................................. 41
   6.3 Nonorganic Base Materials ............................. 41
   6.4 Alternative Printed Board Structures .................. 41
   6.4.1 Supporting-Plane Printed Board Structures ........ 41
   6.4.2 High-Density Printed Board Technology ............. 41
   6.4.3 Constraining Core Structures ....................... 41
   6.4.4 Porcelainized Metal (Metal Core) Structures ...... 41

7 ASSEMBLY CONSIDERATION FOR SURFACE MOUNT TECHNOLOGY (SMT) .................. 44
   7.1 SMT Assembly Process Sequence ......................... 44
   7.2 Substrate Preparation .................................... 44
   7.2.1 Adhesive Application ................................. 44
   7.2.2 Conductive Adhesive .................................. 44
   7.2.3 Solder Paste Application ............................. 45
   7.2.4 Solder Preforms ....................................... 45
8 IPC-7352 DISCRETE COMPONENTS

8.1 Chip Resistors (RESC) ........................................... 49
  8.1.1 Basic Construction ............................................. 49
  8.1.2 Marking .............................................................. 49
  8.1.3 Carrier Package .................................................. 49
  8.1.4 Resistance to Soldering Process
        Temperatures ...................................................... 49
8.2 Chip Capacitors (CAPC) ........................................... 50
  8.2.1 Basic Construction ............................................. 50
  8.2.2 Marking .............................................................. 50
  8.2.3 Carrier Package .................................................. 50
  8.2.4 Resistance to Soldering Process
        Temperatures ...................................................... 50
8.3 Inductors (INDC, INDM, INDP) ................................ 51
  8.3.1 Basic Construction ............................................. 51
  8.3.2 Marking .............................................................. 51
  8.3.3 Carrier Package Format ....................................... 51
  8.3.4 Resistance to Soldering Process
        Temperatures ...................................................... 51
8.4 Tantalum Capacitors (CAPT) ................................... 51
  8.4.1 Basic Construction ............................................. 51
  8.4.2 Marking .............................................................. 51
  8.4.3 Carrier Package Format ....................................... 51
  8.4.4 Resistance to Soldering Process
        Temperatures ...................................................... 51
8.5 Metal Electrode Face Diodes (DIOMELF, RESMELF) .... 52
  8.5.1 Basic Construction ............................................. 52
  8.5.2 Marking .............................................................. 52
  8.5.3 Carrier Package Format ....................................... 52
8.6 SOT23 .............................................................. 53
  8.6.1 Basic Construction ............................................. 53
  8.6.2 Marking .............................................................. 53
  8.6.3 Carrier Package Format ....................................... 53
  8.6.4 Resistance to Soldering Process
        Temperatures ...................................................... 53
8.7 SOT89 .............................................................. 53
  8.7.1 Basic Construction ............................................. 53
  8.7.2 Marking .............................................................. 53
  8.7.3 Carrier Package Format ....................................... 53
  8.7.4 Resistance to Soldering Process
        Temperatures ...................................................... 53
8.8 SOD123 .............................................................. 53
  8.8.1 Basic Construction ............................................. 53
  8.8.2 Marking .............................................................. 53
  8.8.3 Carrier Package Format ....................................... 53
  8.8.4 Resistance to Soldering Process
        Temperatures ...................................................... 53
8.9 SOT143 .............................................................. 53
  8.9.1 Basic Construction ............................................. 53
  8.9.2 Marking .............................................................. 53
  8.9.3 Carrier Package Format ....................................... 53
  8.9.4 Resistance to Soldering Process
        Temperatures ...................................................... 53
8.10 SOT223 ............................................................. 54
  8.10.1 Basic Construction ............................................. 54
  8.10.2 Marking .............................................................. 54
  8.10.3 Carrier Package Format ....................................... 54
  8.10.4 Resistance to Soldering Process
        Temperatures ...................................................... 54
8.11 TO252 (DPAK Type) .............................................. 54
  8.11.1 Basic Construction ............................................. 54
  8.11.2 Marking .............................................................. 54
  8.11.3 Carrier Package Format ....................................... 54
  8.11.4 Resistance to Soldering Process
        Temperatures ...................................................... 54
9 IPC-7353 GULLWING LEADED COMPONENTS,
    TWO SIDES ................................................................
  9.1 SOIC .................................................................. 55
        9.1.1 Basic Construction ............................................. 55
        9.1.2 Marking .............................................................. 55
        9.1.3 Carrier Package Format ....................................... 55
        9.1.4 Resistance to Soldering Process
              Temperatures ...................................................... 55
  9.2 SOP8/SOP63 (SSOIC) .............................................. 56
        9.2.1 Basic Construction ............................................. 56
9.2.2 Marking ......................................................... 56
9.2.3 Carrier Package Format .................................... 56
9.2.4 Resistance to Soldering Process Temperatures .......... 56
9.3 SOP127 (SOP-IPC-782) ........................................... 56
9.3.1 Marking .......................................................... 57
9.3.2 Carrier Package Format ....................................... 57
9.3.3 Resistance to Soldering Process Temperatures .......... 57
9.4 TSSOPs .............................................................. 57
9.4.1 Marking .......................................................... 57
9.4.2 Carrier Packages Format ...................................... 57
9.4.3 Resistance to Soldering Process Temperatures .......... 57
9.5 CFP127 .............................................................. 57
9.5.1 Marking .......................................................... 58
9.5.2 Carrier Packages Format ...................................... 58
9.5.3 Resistance to Soldering Process Temperatures .......... 58

10 IPC-7354 J-LEADED COMPONENTS, TWO SIDES .......... 58
10.1 Basic Construction .............................................. 58
10.2 Marking .......................................................... 58
10.3 Carrier Package Format ........................................ 58
10.4 Process Considerations ......................................... 59

11 IPC-7355 GULL-WING LEADED COMPONENTS, FOUR SIDES 60
11.1 BQFP (PQFP) .................................................... 61
11.1.1 Carrier Package Format ...................................... 61
11.2 SQFP/QFP .......................................................... 61
11.2.1 Carrier Package Format ...................................... 61
11.3 QFPR ............................................................... 61
11.3.1 Carrier Package Format ...................................... 61
11.4 CQFP ............................................................... 61
11.4.1 Carrier Package Format ...................................... 62

12 IPC-7356 J LEADED COMPONENTS, FOUR SIDES .......... 62
12.1 PLCC .............................................................. 63
12.1.1 Premolded Plastic Chip Carriers ......................... 63
12.1.2 Postmolded Plastic Chip Carriers ....................... 63
12.2 PLCCR ............................................................. 64
12.2.1 Premolded Plastic Chip Carriers ......................... 64
12.2.2 Postmolded Plastic Chip Carriers ....................... 64

13 IPC-7357 POST (DIP) LEADS, TWO SIDES ................. 64
13.1 Termination Materials .......................................... 64
13.2 Marking .......................................................... 65
13.3 Carrier Package Format ........................................ 66
13.4 Resistance to Soldering Process Temperatures .......... 66

14 IPC-7358 AREA ARRAY COMPONENTS (BGA, FBGA, CGA, LGA, Chip Array) 66
14.1 Area Array Configurations .................................... 66
14.1.1 BGA Packages ................................................. 66
14.1.2 Fine Pitch BGA Package (FBGA) ......................... 67
14.1.3 Ceramic Column Grid Arrays (CGA) .................... 68
14.1.4 Plastic Land Grid Arrays (LGA) ......................... 68
14.2 General Configuration Issues ................................. 68
14.2.1 Device Outlines .............................................. 68
14.2.2 Contact Matrix Options .................................... 68
14.2.3 Selective Depopulation ..................................... 69
14.2.4 Attachment Site Planning .................................. 69
14.2.5 Defining Contact Assignment ............................. 70
14.3 Handling and Shipping ......................................... 70
14.4 Land Pattern Analysis .......................................... 70
14.4.1 Land Approximation ......................................... 71
14.4.2 Total Variation ............................................... 72
14.4.3 Land Pattern Calculator .................................... 72
14.5 Chip Array Component Lead Packages ..................... 72
14.5.1 Concave Chip Array Packages ............................. 72
14.5.2 Convex Chip Array Packages ............................... 72
14.5.3 Flat Chip Array Packages .................................. 73

15 IPC-7359 NO LEAD COMPONENTS (QFN, PQFN, PSON, LCC) 74
15.1 LCC ............................................................... 74
15.1.1 Marking ........................................................ 74
15.1.2 Carrier Package Format .................................... 74
15.1.3 Process Considerations ..................................... 74
15.2 Quad Flat No-Lead (QFN) .................................... 74
15.2.1 Marking ........................................................ 76
15.2.2 Carrier Package Format .................................... 76
15.2.3 Process Considerations ..................................... 76
15.2.4 Solder Mask Considerations ................................. 76
15.3 Small Outline No-Lead (SON) ................................. 76
15.3.1 Marking ........................................................ 76
15.3.2 Carrier Package Format .................................... 77
15.3.3 Process Considerations ..................................... 77
15.3.4 Solder Mask Considerations ................................. 77
15.4 Small Outline and Quad Flat No Lead with Pullback Leads (PQFN, PSON) .......... 77

16 ZERO COMPONENT ORIENTATIONS .......................... 77
Generic Requirements for Surface Mount Design and Land Pattern Standard

1 SCOPE
This document provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet to meet the requirements of IPC J-STD-001, and also to allow for inspection, testing, and rework of those solder joints.

1.1 Purpose Although, in many instances, the land pattern geometries can be different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined with consideration to the attachment process being used. Designers can use the information contained herein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Land patterns are dimensionally defined and are a part of the printed board circuitry geometry, as they are subject to the producibility levels and tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

Note 1: The dimensions used for component descriptions have been extracted from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions.

Note 2: For a comprehensive description of the given printed board and for achieving the best possible solder joints to the devices assembled, the whole set of design elements includes, beside the land pattern definition:
- Soldermask
- Solder paste stencil
- Clearance between adjacent components
- Clearance between bottom of component and printed board surface, if relevant
- Keepout areas, if relevant
- Suitable rules for adhesive applications

The whole of design elements is commonly defined as “mounting conditions.” This standard defines land patterns and includes recommendations for clearances between adjacent components and for other design elements.

Note 3: Elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

Note 4: This standard assumes that the land pattern follows the principle that, even under worst case conditions, the overlap of the component termination and the corresponding soldering land will be complete.

Note 5: Heat dissipation aspects have not been taken into account in this standard. Greater mass may require slower process speed to allow heat transfer.

Note 6: Heavier components (greater weight per land) require larger lands; thus, adding additional land pattern surface will increase surface area of molten solder to enhance capabilities of extra weight. In some cases the lands shown in the standard may not be large enough; in these cases, considering additional measures may be necessary.

1.2 Documentation Hierarchy This standard identifies the generic physical design principles involved in the creation of land patterns for surface mount components, and is supplemented by a shareware IPC-7351 Land Pattern viewer that provides, through the use of a graphical user interface, the individual component dimensions and corresponding land pattern recommendations based upon families of components. The IPC-7351 Land Pattern Viewer is provided on CD-ROM as part of this standard. Updates to land pattern dimensions, including patterns for new component families, can be found on the IPC website (www.ipc.org) under “PCB Tools and Calculators.” See Appendix C for more information on the IPC-7351 Land Pattern Viewer.

1.2.1 Component and Land Pattern Family Structure The IPC-7351 provides the following number designation within this standard for each major family of surface mount components to indicate similarities in solder joint engineering goals:

- IPC-7352 – Discrete Components (CAP, RES, IND, DIO, LED)
- IPC-7353 – Gullwing Leaded Components, Two Sides (SOP, SOIC, SOD, SOT, TO)