IPC-7094A

Design and Assembly Process Implementation for Flip Chip and Die-Size Components

Developed by the Flip Chip Mounting Task Group (5-21g) of the Assembly & Joining Processes Committee (5-20) of IPC

Supersedes:
IPC-7094 - February 2009

Users of this publication are encouraged to participate in the development of future revisions.

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IPC

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Design and Assembly Process Implementation for Flip Chip and Die Size Components

1 SCOPE

This document describes the design and assembly challenges for implementing flip chip technology in a direct chip attach (DCA) assembly. The effect of bare-die or die-size components in a flip chip format has an impact on component characteristics and dictates the appropriate assembly methodology. This standard focuses on design, assembly methodology, critical inspection, repair and reliability issues associated with flip chip and die-size package technologies, including wafer-level ball grid array (WLBGA).

1.1 Target Audience and Intent The target audiences for this document are managers, design and process engineers as well as operators and technicians who deal with electronic assembly, inspection and repair processes. The intent is to provide useful and practical information to those who mount bare-die or die-size components in a DCA assembly or those who are considering flip chip process implementation.

1.2 Definition of Requirements The imperative form of action verbs is used throughout this document to identify acceptance requirements that may require compliance, depending on the Performance Classification of the hardware (see 1.3). To assist the User, these action verbs are in bold text.

a) The words ''**shall/shall not**'' are used whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** or **shall not** requirement for a Performance Class may be considered if sufficient technical rationale/objective evidence is supplied to the User to justify the exception.

b) The word ''should'' is used whenever a requirement is intended to express a provision that is nonmandatory and which reflects general industry practice and/or procedure.

1.3 Classification of Product The following is a general explanation of the three classes of hardware, (see J-STD-001 for details concerning the specific requirements for each of these classes).

IPC CLASS 1, General Electronic Products – Includes products suitable for applications in which the major requirement is function of the completed assembly.

IPC CLASS 2, Dedicated Service Electronic Products – Includes products for which continued performance and extended life is required and for which uninterrupted service is desired, but not critical. Typically, the end-use environment would not cause failures.

IPC CLASS 3, High-Performance Electronic Products – Includes products for which continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Each of these three classes most likely will have different reliability requirements as dictated by the end user and the intended use environment.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

1. www.ipc.org