Design and Assembly Process Implementation for Embedded Components

Developed by the Embedded Devices Process Implementation Subcommittee (D-55) of the Embedded Components Committee (D-50) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105
# Table of Contents

1 SCOPE ................................................................. 1  
1.1 Purpose ......................................................... 1  
1.2 Intent ............................................................ 1  
2 APPLICABLE DOCUMENTS ........................................ 1  
2.1 IPC ............................................................... 1  
2.2 Joint Industry Standards ..................................... 2  
2.3 ASME ............................................................ 2  
2.4 GEIA .............................................................. 2  
2.5 JEDEC ............................................................ 2  
2.6 IEC ................................................................. 2  
2.7 ISO/IEC ............................................................ 2  
3 GENERAL DESCRIPTION ........................................ 3  
3.1 Terms and Definitions ......................................... 4  
3.1.1 Active Device ................................................. 4  
3.1.2 Active Trimming ............................................. 4  
3.1.3 Capacitance* ................................................ 4  
3.1.4 Coefficient of Thermal Expansion ...................... 4  
3.1.5 Device ........................................................ 4  
3.1.6 Discrete Component* ...................................... 4  
3.1.7 Embedded Active Component (Device) .............. 4  
3.1.8 Embedded Component .................................... 4  
3.1.9 Embedded Component (Placed) ....................... 4  
3.1.10 Embedded Component (Formed) ...................... 4  
3.1.11 Embedded Component Base-Core (ECBC)* ......... 4  
3.1.12 Embedded Component Board Assembly (ECBA)* .... 4  
3.1.13 Embedded Component Printed Board (ECPB)* .......... 4  
3.1.14 Embedded Component Substrate* ..................... 4  
3.1.15 Embedded Substrate Testing* ......................... 4  
3.1.16 Embedded Passive ....................................... 4  
3.1.17 Embedded Passive Component (Device) ............ 5  
3.1.18 Embedded Substrate Board* ............................. 5  
3.1.19 Face Down Bonding* .................................... 5  
3.1.20 Face Up Bonding* ....................................... 5  
3.1.21 Integrated Passive Component ....................... 5  
3.1.22 Mounting Base* ........................................... 5  
3.1.23 Multilayer Printed Board (nonpreferred term, “multilayer printed circuit board”)* .................. 5  
3.1.24 Passive Array (Embedded)* ........................... 5  
3.1.25 Passive Component (Element) ....................... 5  
3.1.26 Passive Network (Embedded)* ....................... 6  
3.1.27 Printed Board (PB) ........................................ 6  
3.1.28 Printed Circuit .............................................. 6  
3.1.29 Printed Circuit Board .................................... 6  
3.1.30 Production Board ....................................... 6  
3.1.31 Production Panel (PP) ................................. 6  
3.1.32 Production Printed Board (PPB) ...................... 6  
3.1.33 Stacked Via/Microvia .................................... 6  
3.1.34 Temperature Delta (ΔT)* ................................. 6  
3.1.35 Temperature Coefficient of Capacitance* ............ 6  
3.1.36 Temperature Coefficient of Resistance* ............. 6  
3.1.37 Thermal Expansion Mismatch ......................... 6  
3.1.38 Thermal Resistance ....................................... 6  
3.2 Technology Overview ......................................... 6  
3.2.1 Passive (Resistors, Capacitors, Inductors, etc.) .......... 8  
3.2.2 Active (Transistors, Memory, Semiconductors, etc.) .... 9  
3.3 Embedded (Placed) Technology .......................... 10  
3.3.1 Passive (Resistors, Capacitors, Inductors, etc.) .......... 10  
3.3.2 Active (Transistors, Memory, Semiconductors, etc.) .... 10  
3.4 Material Requirements ........................................ 11  
3.4.1 Mounting Materials ....................................... 11  
3.4.2 Component Formation Materials ...................... 12  
3.4.3 Attachment Materials .................................... 12  
3.4.4 Encapsulation Materials .................................. 12  
3.5 Cost Analysis .................................................. 12  
3.5.1 Fabrication and Manufacturing Cost Modeling .......... 13  
3.5.2 Life Cycle Costs Impacted by Embedded Components .... 14  
3.6 Product Safety Design Considerations ................... 15  
3.7 Case Study and Decision Making .......................... 15  
3.7.1 General Case Study ....................................... 16  
3.7.2 Scenarios for Embedded Components .................. 16  
4 COMPONENT CONSIDERATIONS .................................. 16  
4.1 General Requirements ........................................ 16  
4.1.1 Part Robustness Evaluations ............................. 16  
4.1.2 Test Method Correlation .................................. 17  
4.1.3 Determining Values That Can Be Placed .......... 17  
4.2 Component Preparation ...................................... 17  
4.2.1 Passive Component Issues ............................... 17  
4.2.2 Semiconductor Die Issues ............................... 17  
4.2.3 Surface Redistribution .................................... 17  
4.2.4 Coefficient of Thermal Expansion ..................... 17  
4.3 Component Preparation ...................................... 17  
4.3.1 Determining Values That Can Be Placed .......... 17  
4.3.2 Component Preparation ................................. 17  
4.3.3 Surface Redistribution .................................... 17  
4.4 Component Preparation ...................................... 17  
4.4.1 Determining Values That Can Be Placed .......... 17  
4.4.2 Component Preparation ................................. 17  
4.4.3 Surface Redistribution .................................... 17  
4.5 Component Preparation ...................................... 17  
4.5.1 Determining Values That Can Be Placed .......... 17  
4.5.2 Component Preparation ................................. 17  
4.5.3 Surface Redistribution .................................... 17  
4.6 Component Preparation ...................................... 17  
4.6.1 Determining Values That Can Be Placed .......... 17  
4.6.2 Component Preparation ................................. 17  
4.6.3 Surface Redistribution .................................... 17  
4.7 Component Preparation ...................................... 17  
4.7.1 Determining Values That Can Be Placed .......... 17  
4.7.2 Component Preparation ................................. 17  
4.7.3 Surface Redistribution .................................... 17  
4.8 Component Preparation ...................................... 17  
4.8.1 Determining Values That Can Be Placed .......... 17  
4.8.2 Component Preparation ................................. 17  
4.8.3 Surface Redistribution .................................... 17  
4.9 Component Preparation ...................................... 17  
4.9.1 Determining Values That Can Be Placed .......... 17  
4.9.2 Component Preparation ................................. 17  
4.9.3 Surface Redistribution .................................... 17  
4.10 Component Preparation ...................................... 17  
4.10.1 Determining Values That Can Be Placed .......... 17  
4.10.2 Component Preparation ................................. 17  
4.10.3 Surface Redistribution .................................... 17
4.3 Post Process Validations ............................... 18
4.4 Known Good Die (KGD) ............................... 18

5 MATERIALS ................................................. 19
5.1 Organic Resins ........................................... 19
5.1.1 Multilayer PCB Stack-Up Design .................. 20
5.1.2 Selecting Relative Dielectric Constant .......... 20
5.2 Nonorganic Products .................................... 20
5.3 Conductor Characteristics (Copper Foil/Film) ...... 20
5.4 Component Forming Material .......................... 21
5.4.1 Embedded Passive Component Selection Criteria ......... 21
5.4.2 Formed Resistors ...................................... 21
5.4.3 Thick Film Resistor Cost and Performance ....... 22
5.4.4 Sheet Film Type Resistor Elements ............... 28
5.4.5 Embedded Capacitors ................................ 31
5.4.6 Formed Inductors ..................................... 34
5.4.7 Formed Active Components ....................... 37
5.5 Adhesives (Conductive/Nonconductive) ............ 37
5.5.1 Polymer Adhesives ...................................... 38
5.5.2 Dry-Film Adhesives .................................... 38
5.6 Solder and Other Attachment Materials ............. 38
5.7 Plating Material Properties (Characteristics, Application For Attachment) .... 39
5.7.1 Electrode Finish Compatibility ..................... 39

6 EMBEDDED COMPONENT PROCESS CHARACTERISTICS .......... 39
6.1 Forming Passive Components ....................... 39
6.1.1 Tolerance Capability Evaluations .................. 39
6.2 Forming Active Components ........................ 40
6.3 Placing Passive Components .......................... 40
6.3.1 Shape Configuration ................................... 40
6.3.2 Electrode Metallization ............................... 41
6.3.3 Shape and Configuration Considerations for Embedding .......... 41
6.3.4 Electrode Susceptibility .............................. 41
6.3.5 Component Encroachment ............................ 41
6.4 Placing Active Components ............................ 41
6.4.1 Attachment Techniques ............................... 42
6.4.2 Flip-Chip Attachment .................................. 42
6.4.3 Gold-to-Gold Interface (GGI) ...................... 42
6.4.4 Face-Up Microvia Interface ......................... 42
6.4.5 Protective Die Methods .............................. 43
6.5 Consideration for Combining Processes .......... 43
6.5.1 Mixed Component Types ............................. 44
6.5.2 Placement and Forming Combinations ............ 44

7 MOUNTING BASE OR BOARD STACKUP CONSIDERATIONS ................. 44
7.1 Mounting Base .......................................... 44
7.2 Surface Finish for Placed Components .............. 44
7.2.1 Electroless Nickel/Immersion Gold (ENIG) .... 44
7.2.2 Electroless Nickel/Electrolytic Palladium/Immersion Gold (ENEPIG) ................. 45
7.3 Organic Solderability Preservative (OSP) ......... 45
7.4 Electrolytic Nickel/Electrolytic Gold .............. 45
7.5 Direct Immersion Gold (DIG) ....................... 45
7.6 Immersion Silver ........................................ 45
7.7 Immersion Tin ............................................ 45
7.8 Copper .................................................. 45
7.9 Capacitor Component Formation Process .......... 45
7.9.1 Planar Capacitance .................................... 45
7.9.2 Plane Layer Separation ............................... 46
7.9.3 Discrete Formed Capacitor Element ............... 46
7.10 Component Attachment Process ..................... 46
7.11 Dielectric Encapsulation ............................. 47
7.12 Reinforced Prepreg ..................................... 48
7.13 Unreinforced Resin .................................... 49
7.14 Resin-Coated Copper (RCC) ......................... 50
7.15 Via Hole Preparation and Interconnectivity ....... 50
7.16 Additional Layers and Hole Preparation .......... 51
7.17 Embedded Structure Descriptions ................... 55
7.18 Embedded Structure Type A ......................... 56
7.19 Embedded Structure Type B .......................... 60
7.20 Embedded Structure Type C .......................... 63
7.21 Embedded Structure Type D .......................... 67
7.22 Embedded Structure Type E .......................... 71
7.23 Processes Parameters for Structure Type F1, Embedded Core Technology .......... 74

8 DESIGN METHODOLOGY ................................... 77
8.1 Total Circuit Consideration ............................ 77
8.1.1 Internal Component Mounting ..................... 80
8.1.2 External Component Mounting ..................... 80
8.1.3 Circuit Interfaces ..................................... 81
8.1.4 Internal Discrete Heat Sink ....................... 81
8.2 Layout Strategy ........................................... 81
8.2.1 Product Functional Description ................... 82
8.2.2 Engineering Actions .................................. 83
8.2.3 Design Density Analysis ............................. 86
8.2.4 Candidate for Embedding ......................... 86
8.2.5 Circuitry to be Embedded ............................ 89
8.3 PCB Layer Construction and Geometries .......... 91
8.3.1 Using Radius Bends and Blind/Buried Vias ....... 91
Figure 7-33  E1 Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides to complete the Embedded Component Printed Board ................................ 71
Figure 7-34  E1 Process Flow ........................................ 71
Figure 7-35  E2 Mounting base example with formed passive components inside the mounting base turning the product into a base-core ready for component mounting to complete an Embedded Component Board Assembly .......... 72
Figure 7-36  E2 Process Flow ........................................ 72
Figure 7-37  E3 Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides to complete the Embedded Component Printed Board ready for component mounting to complete an Embedded Component Board Assembly .... 73
Figure 7-38  E3 Process Flow ........................................ 73
Figure 7-39  Embedded Core Process Overview ............. 74
Figure 7-40  Core with Placed Active Component and Two Buildup Layers Forming an HDI Multilayer ........................................ 75
Figure 7-41  F1, SIP Example with Facedown Placed Passive and Active Components on Cu Foil Base and Accommodation for Mounting Components on Outer Surface .......... 75
Figure 7-42  F1 System-in-Package Process Flow .......... 76
Figure 7-43  F2, SiB Example with Embedded Facedown Placed Passive and Multiple Active Components on Cu Foil Base ........ 76
Figure 7-44  F2 System-in-Board Process Flow .......... 76
Figure 7-45  Variation F1, SiP with Embedded Processor ........................................ 76
Figure 8-1  Electronic Component Symbols and Associated Reference Designation ............. 77
Figure 8-2  Embedded Component Selection .................. 78
Figure 8-3  Four Layer PCB Artwork ................................ 79
Figure 8-4  Cavity in Dielectric For Higher Profile Components ........................................ 80
Figure 8-5  Face-up, In-Cavity Die Attach for Microvia Interface ........................................ 81
Figure 8-6  Wireless and Portable Market Drivers ........... 83
Figure 8-7  Functional Block Diagram Example ............ 84
Figure 8-8  Parts List Example Showing Four Assembly Variations .................................. 86
Figure 8-9  Example of a Standard Plug in Module Board Usable Area .................................. 87
Figure 8-10  Discrete Chip Component Sizes Compared to Attachment Techniques ........... 87
Figure 8-11  Examples of Various Stackup Layer Constructions .................................. 88
Figure 8-12  Example of Small Form Factor Final Assembly ........................................ 88
Figure 8-13  Basic Four-Layer Circuit Structure ............. 90
Figure 8-14  Ground Conductors Shielding for Sensitive Circuits .................................. 90
Figure 8-15  Solder Paste for Precision Dispensing ............. 92
Figure 8-16  Dry-Film Die Attach Material Dispensing on Semiconductor Wafer .................. 94
Figure 8-17  Thermoplastic Bonding Window ................... 96
Figure 8-18  Six Unit Panel ECPB with Clearance for Singulation Using Mechanical Routing .......... 96
Figure 8-19  Comparing Segmented Power Plane Topologies ................................... 98
Figure 8-20  Comparing PCB Via Variations ................... 100
Figure 8-21  Comparing Blind Via Fill Variations ............. 100
Figure 8-22  Wire-bond Termination for Face-up Embedded Active Die Element ................... 101
Figure 8-23  Comparing Contact Variation for Face-Down Embedded Die Assembly ........... 101
Figure 8-24  Flying Probe Test System ......................... 101
Figure 8-25  Comparing Hard Copy to Electronic Documentation .................................. 102
Figure 8-26  Standard Documentation Hierarchy Sectional Descriptions and Data Flow ........ 103
Figure 8-27  Documentation Package Grade Requirements ......................................... 104
Figure 8-28  Bill of Material Activity Requirement ............. 107
Figure 9-1  Interconnection Opens and Shorts Test .......... 108
Figure 9-2  Base Core Testing of Passive Components .................. 109
Figure 9-3  Device Embedded Substrate ......................... 109
Figure 11-1  Sample Test Patterns .................. 119
Figure B-1  SIPOS_EB0101 ........................................ 124
Figure B-2  Test Board Details ................................. 125
Figure B-3  Three Point Bend Test ......................... 126
Figure B-4  SPIOs_EB0301 .................................. 127
Figure B-5  Test Boards ......................................... 128
Figure B-6  Testing of the SPIOs_EB0301 Coupon ........... 129

Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 3-1</td>
<td>Passive Component Selection Criteria</td>
</tr>
<tr>
<td>Table 3-2</td>
<td>Common Thick and Thin-Film Ceramic Technologies</td>
</tr>
<tr>
<td>Table 3-3</td>
<td>Factors that Impact the Decision Process for Embedding Components</td>
</tr>
<tr>
<td>Table 3-4</td>
<td>Case Study Examples</td>
</tr>
<tr>
<td>Table 4-1</td>
<td>Bare Die Quality Classification</td>
</tr>
<tr>
<td>Table 5-1</td>
<td>Glass Reinforced Laminate Thickness and Tolerances (Data source: IPC-4101)</td>
</tr>
<tr>
<td>Table 5-2</td>
<td>Standard Copper Foil Thickness</td>
</tr>
<tr>
<td>Table 5-3</td>
<td>Formed Resistor Material Variations</td>
</tr>
<tr>
<td>Table 5-4</td>
<td>Resistance Summary</td>
</tr>
<tr>
<td>Table 5-5</td>
<td>Electrical Properties</td>
</tr>
<tr>
<td>Table 7-1</td>
<td>Compatible Finishes for Attaching Bottom Termination Components to an Embedded Component Substrate (ECS)</td>
</tr>
<tr>
<td>Table 7-2</td>
<td>Assembly Process Temperature Exposure Levels</td>
</tr>
</tbody>
</table>
Table 7-3  FR-4 Material Properties to Meet Assembly Exposures ......................................................... 47
Table 7-4  Examples of Non-FR-4 Material Properties to Meet Assembly Exposure ......................... 49
Table 7-5  Requirement Identification for Resin-Coated Copper .......................................................... 50
Table 7-6  Embedded Component Base-Core Descriptions ................................................................. 56
Table 7-7  F1 and F2 Embedded Component Base-Core Descriptions .................................................... 74
Table 8-1  General Rules for Decision Making ......................... 83
Table 8-2  Embedded Design Outsourcing Model Types ................................................................. 84
Table 8-3  Prepreg Material Style and Thickness Guide (Dimensions are shown in 1/1000 inches) ...... 89
Table 8-4  Key Design Measures for Suppressing EMI/RFI (Data source: Nexlogic Technologies) ........ 91
Table 8-5  Solder Alloy Composition Selection ................ 93
Table 8-6  Comparing Attachment Material Attributes ...... 93
Table 8-7  Comparing Adhesive Material Attributes Data source: AI Technology ......................... 95
Table 8-8  Copper Weight and Thickness ...................... 97
Table 8-9  External Layer Current Carrying Capacity Rating .................................................................. 97
Table 8-10 Internal Layer Current Carrying Capacity Rating .................................................................. 98
Table 8-11 File Segmentation and Functional Requirements .......................................................... 106
Table 9-1  Product Categories ........................................ 110
Table 9-2  Process Qualification Recommendation ........ 111
Table 9-3  Embedded Base-Core Repair and Modification Recommendations ...................................... 113
Table 10-1  Accelerated Testing for End Use Environments ............................................................ 116
Table 10-2  Temperature Cycling Requirements, Mandated and Preferred Test Parameters within Mandated Conditions ................................................................. 117
Design and Assembly Process
Implementation for Embedded Components

1 SCOPE
This document describes the design and assembly challenges for implementing passive and active components, in either formed or placed methodology, into a printed board. The completed structure including internal electronic components is ready for surface mount and/or through-hole component attachment. The multilayered structure becomes a complete product ready for further processing in an assembly process and can be made from organic, inorganic (ceramic) or both types of material.

1.1 Purpose The target audiences for this document are managers, design and process engineers, and technicians who develop electronic assemblies that include an embedded component printed board as a part of the product. The purpose is to provide useful and practical information to those who are involved in the decision making of either formed or placed, passive or active components and to help establish inspection techniques, testing processes, and reliability validations.

1.2 Intent This document, although not a complete recipe, identifies many of the characteristics that influence the successful implementation of a robust embedded component process. In many applications, the variation between forming and placing methods and materials are reviewed with the intent to highlight significant differences that relate to the decision as to when, why, or how to establish the quality and reliability of the final product. The information also establishes the robustness that the embedded portion of the product can survive the continued processing in order to complete an Embedded Component Printed Board Assembly.

An additional challenge in implementing the processes, along with all the varieties of electronic components, internal and external, is the need to meet the legislative directives that declare certain materials as hazardous to the environment. The requirements to eliminate these materials from electronic assemblies have caused component manufacturers to rethink the materials used for encapsulation, the plating finishes on the components and the metal alloys used in the assembly attachment process.

2 APPLICABLE DOCUMENTS

2.1 IPC

IPC-J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies
IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies
IPC-D-356 Bare Substrate Electrical Test Data Format
IPC-QL-653 Certification of Facilities that Inspect/Test Printed Boards, Components and Materials
IPC-SM-784 Guidelines for Chip-on-Board Technology Implementation
IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments
IPC-2316 Design Guide for Embedded Passive Device Printed Boards
IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology
IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-4562 Metal Foil for Printed Wiring Applications

1. www.ipc.org