Qualification and Performance Specification for High Frequency (Microwave) Printed Boards

Developed by the High Speed/High Frequency Board Performance Subcommittee (D-22) of the High Speed/High Frequency Committee (D-20) of IPC

**Supersedes:**
IPC-6018B – November 2011
IPC-6018A – January 2002
IPC-6018 – January 1998

Users of this publication are encouraged to participate in the development of future revisions.

Contact:
IPC
# Table of Contents

1 **SCOPE** ................................................................. 1

1.1 Statement of Scope ............................................. 1

1.2 Purpose ............................................................. 1

1.3 Performance Classification and Types .................. 1

1.3.1 Classifications ................................................ 1

1.3.2 Printed Board Type ......................................... 1

1.3.3 Selection for Procurement ............................... 1

1.3.4 Material, Plating Process and Final Finish ........ 3

1.4 Terms and Definitions ........................................ 3

1.4.1 White Spots .................................................... 3

1.4.2 Hybrid (Composite) Printed Board .................... 3

1.4.3 As Agreed Between User and Supplier (AABUS) .... 3

1.4.4 High Density Interconnects (HDI) ....................... 3

1.5 Interpretation ..................................................... 4

1.6 Presentation ....................................................... 4

1.7 Revision Level Changes ...................................... 4

1.8 Master Drawing .................................................. 4

2 **APPLICABLE DOCUMENTS** .................................... 4

2.1 IPC ........................................................................ 4

2.2 Joint Industry Standards ...................................... 6

2.3 Federal ............................................................... 6

2.4 American Society for Testing and Materials ....... 6

2.5 Underwriters Lab ................................................. 6

2.6 National Electrical Manufacturers Association .... 7

2.7 American Society for Quality ............................... 7

2.8 AMS ................................................................. 7

2.9 American Society of Mechanical Engineers ....... 7

3 **REQUIREMENTS** .................................................. 7

3.1 General .............................................................. 7

3.2 Materials Used in this Specification .................. 7

3.2.1 Laminates and Bonding Material for Multilayer or Mixed Dielectric Printed Boards .................................................. 7

3.2.2 External Bonding Materials ............................ 7

3.2.3 Other Dielectric Materials ............................... 7

3.2.4 Metal Foils ....................................................... 7

3.2.5 Metal Core/Backed ......................................... 8

3.2.6 Base Metallic Plating Depositions and Conductive Coatings .................................................. 8

3.2.7 Final Finish Depositions and Coatings – Metallic and Nonmetallic .................................................. 8

3.2.8 Polymer Coating (Solder Mask) ....................... 12

3.2.9 Fusing Fluids and Fluxes .................................. 12

3.2.10 Marking Inks .................................................. 12

3.2.11 Hole Fill Insulation Material ......................... 12

3.2.12 Metal and/or Composite, External ................ 12

3.2.13 Via Protection ................................................ 12

3.2.14 Embedded Passive Materials ....................... 12

3.3 Visual ................................................................. 12

3.3.1 Edges of Microwave Printed Boards ............... 12

3.3.2 Laminate Imperfections ................................... 12

3.3.3 Plating and Coating Voids in the Hole ............. 13

3.3.4 Lifted Lands ..................................................... 14

3.3.5 Marking .......................................................... 14

3.3.6 Solderability ..................................................... 14

3.3.7 Plating Adhesion ............................................. 14

3.3.8 Edge Printed Board Contact, Junction of Gold Plate to Solder Finish .................................................. 15

3.3.9 Workmanship .................................................. 15

3.4 Printed Board Dimensional Requirements .......... 15

3.4.1 Hole Size, Hole Pattern Accuracy, Pattern Feature Accuracy and Slots .................................................. 15

3.4.2 Annular Ring and Breakout (External) ............... 16

3.4.3 Bow and Twist ................................................ 17

3.5 Conductor Definition ........................................ 18

3.5.1 Undercutting ................................................... 18

3.5.2 Conductor Widths and Thicknesses and Spacing .................................................. 18

3.5.3 Conductive Surfaces ........................................ 19

3.6 Structural Integrity ............................................. 21

3.6.1 Thermal Stress Testing ..................................... 22

3.6.2 Requirements for Microsectioned Coupons or Printed Boards .................................................. 23

3.7 Solder Mask Requirements on non-PTFE laminates .................................................. 36

3.7.1 Solder Mask Coverage .................................... 36

3.7.2 Solder Mask Cure and Adhesion ....................... 37

3.7.3 Solder Mask Thickness ..................................... 37

3.8 Electrical Requirements ....................................... 37

3.8.1 Dielectric Withstanding Voltage ..................... 37

3.8.2 Electrical Continuity and Isolation Resistance .................................................. 38

3.8.3 Circuit Shorts ................................................... 38

3.8.4 Circuit/PTH Shorts to Metal Substrate .......... 38

3.8.5 Moisture and Insulation Resistance (MIR) .......... 38

3.8.6 Dielectric Withstanding Voltage After MIR .... 38
3.9 Cleanliness ......................................................... 38  
3.9.1 Cleanliness Prior to Solder Mask  
Application .......................................................... 38  
3.9.2 Cleanliness After Solder Mask, Solder, or  
Alternative Surface Coating Application ........... 38  
3.9.3 Cleanliness of Inner Layers After Oxide  
Treatment Prior to Lamination ....................... 38  
3.10 Special Requirements ................................. 38  
3.10.1 Outgassing ..................................................... 39  
3.10.2 Fungus Resistance ........................................... 39  
3.10.3 Vibration ....................................................... 39  
3.10.4 Mechanical Shock ......................................... 39  
3.10.5 Impedance Testing ......................................... 39  
3.10.6 Coefficient of Thermal Expansion (CTE) ..... 39  
3.10.7 Thermal Shock ............................................... 39  
3.10.8 Surface Insulation Resistance  
(As Received) ...................................................... 39  
3.10.9 Wire Bond Adhesion ........................................ 39  
3.10.10 Die Bond Adhesion ......................................... 39  
3.10.11 Rework Simulation ................................. 40  
3.10.12 Metal Core (Horizontal Microsection) ....... 40  
3.10.13 Peel Strength Requirements (For Foil  
Laminated Construction Only) ......................... 40  
3.10.14 Destructive Physical Analysis .................. 40  
3.10.15 Lap Shear .................................................... 40  
3.11 Repair .......................................................... 40  
3.11.1 Circuit Repairs .............................................. 40  
3.12 Rework .......................................................... 40  

4 QUALITY ASSURANCE PROVISIONS .................. 40  
4.1 General .......................................................... 40  
4.1.1 Qualification .................................................. 41  
4.1.2 Sample Test Coupons ..................................... 41  
4.2 Acceptance Tests ............................................. 42  
4.2.1 C=0 Zero Acceptance Number Sampling  
Plan .......................................................... 42  
4.2.2 Referee Tests ................................................. 42  
4.3 Quality Conformance Testing ....................... 42  
4.3.1 Coupon Selection ........................................... 42  

5 PACKAGING ......................................................... 47  

6 NOTES ........................................................... 47  
6.1 Ordering Data .................................................. 47  
6.2 Superseded Specifications ............................. 47

Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 3-1</td>
<td>Microvia Definition</td>
<td>8</td>
</tr>
<tr>
<td>Figure 3-2</td>
<td>Adhesive Band Near Exposed Conductor</td>
<td>15</td>
</tr>
<tr>
<td>Figure 3-3</td>
<td>Annular Ring Measurement (External)</td>
<td>17</td>
</tr>
<tr>
<td>Figure 3-4</td>
<td>Breakout of 90° and 180°</td>
<td>17</td>
</tr>
<tr>
<td>Figure 3-5</td>
<td>Usage of Modified Land Shapes in Breakout Conditions</td>
<td>17</td>
</tr>
<tr>
<td>Figure 3-6</td>
<td>Example of Intermediate Target Land in a Microvia</td>
<td>17</td>
</tr>
<tr>
<td>Figure 3-7</td>
<td>Conductor Edge Definitions</td>
<td>18</td>
</tr>
<tr>
<td>Figure 3-8</td>
<td>Undercut</td>
<td>18</td>
</tr>
<tr>
<td>Figure 3-9</td>
<td>Rectangular Surface Mount Lands</td>
<td>20</td>
</tr>
<tr>
<td>Figure 3-10</td>
<td>Round Surface Mount Lands</td>
<td>20</td>
</tr>
<tr>
<td>Figure 3-11</td>
<td>Printed Board Edge Connector Lands</td>
<td>21</td>
</tr>
<tr>
<td>Figure 3-12</td>
<td>Plated Hole Microsection (Grinding/Polishing) Tolerance</td>
<td>22</td>
</tr>
<tr>
<td>Figure 3-13</td>
<td>An Example of Plating to Target Land Separation</td>
<td>23</td>
</tr>
<tr>
<td>Figure 3-14</td>
<td>Separations at External Foil</td>
<td>25</td>
</tr>
<tr>
<td>Figure 3-15</td>
<td>Crack Definition</td>
<td>25</td>
</tr>
<tr>
<td>Figure 3-16</td>
<td>Plating Folds/Inclusions – Minimum Measurement Points</td>
<td>25</td>
</tr>
<tr>
<td>Figure 3-17</td>
<td>Typical Microsection Evaluation Specimen</td>
<td>26</td>
</tr>
<tr>
<td>Figure 3-18</td>
<td>Measurement for Dielectric Removal</td>
<td>26</td>
</tr>
<tr>
<td>Figure 3-19</td>
<td>Etchback in Contact with PTFE Layer</td>
<td>27</td>
</tr>
<tr>
<td>Figure 3-20</td>
<td>Measurement Locations for PTFE Resin Smear</td>
<td>27</td>
</tr>
<tr>
<td>Figure 3-21</td>
<td>Negative Etchback</td>
<td>28</td>
</tr>
<tr>
<td>Figure 3-22</td>
<td>Annular Ring Measurement (Internal)</td>
<td>28</td>
</tr>
<tr>
<td>Figure 3-23</td>
<td>Microsection Rotations for Breakout Detection</td>
<td>29</td>
</tr>
<tr>
<td>Figure 3-24</td>
<td>Comparison of Microsection Rotations</td>
<td>29</td>
</tr>
<tr>
<td>Figure 3-25</td>
<td>Example of Nonconforming Dielectric Spacing Reduction Due to Breakout at Microvia Target Land</td>
<td>30</td>
</tr>
<tr>
<td>Figure 3-26</td>
<td>Surface Copper Wrap Measurement for Filled Holes</td>
<td>30</td>
</tr>
<tr>
<td>Figure 3-27</td>
<td>Surface Copper Wrap Measurement for Nonfilled Holes</td>
<td>30</td>
</tr>
<tr>
<td>Figure 3-28</td>
<td>Wrap Copper in Type 4 Printed Board (Acceptable)</td>
<td>31</td>
</tr>
<tr>
<td>Figure 3-29</td>
<td>Wrap Copper Removed by Excessive Sanding/Planarization/Etching (Not Acceptable)</td>
<td>31</td>
</tr>
<tr>
<td>Figure 3-30</td>
<td>Copper Cap Thickness</td>
<td>32</td>
</tr>
<tr>
<td>Figure 3-31</td>
<td>Copper Cap Filled Via Height (Bump)</td>
<td>32</td>
</tr>
<tr>
<td>Figure 3-32</td>
<td>Copper Cap Depression (Dimple)</td>
<td>32</td>
</tr>
<tr>
<td>Figure 3-33</td>
<td>Copper Cap Plating Voids</td>
<td>32</td>
</tr>
<tr>
<td>Figure 3-34</td>
<td>Example of Acceptable Voiding in a Cap Plated, Copper Filled Microvia</td>
<td>33</td>
</tr>
<tr>
<td>Figure 3-35</td>
<td>Example of Acceptable Voiding in a Copper Filled Microvia without Cap Plating</td>
<td>33</td>
</tr>
<tr>
<td>Figure 3-36</td>
<td>Example of Nonconforming Void in a Cap Plated, Copper Filled Microvia</td>
<td>33</td>
</tr>
<tr>
<td>Figure 3-37</td>
<td>Example of Nonconforming Void in a Copper Filled Microvia</td>
<td>33</td>
</tr>
<tr>
<td>Figure 3-38</td>
<td>Microvia Contact Dimension</td>
<td>33</td>
</tr>
</tbody>
</table>
Figure 3-39 Exclusion of Separations in Microvia Target Land Contact Dimension .......... 33
Figure 3-40 Penetration of Microvia Target Land .................. 34
Figure 3-41 Metal Core to PTH Spacing ................................ 35
Figure 3-42 Measurement of Minimum Dielectric Spacing ........................................ 35
Figure 3-43 Fill Material in Blind/Through Vias When Cap Plating Not Specified ........ 36

Tables

Table 1-1 Default Requirements ................................................. 2
Table 1-2 Technology Adder Examples .......................................... 2
Table 3-1 Metal Core Substrate ................................................. 8
Table 3-2 Maximum Limits of SnPb Solder Bath Contaminant .............. 9
Table 3-3 Final Finish and Coating Requirements .......................... 10
Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Buried Vias > 2 Layers, Through-Holes, and Blind Vias .............. 11
Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried) ....................................... 11
Table 3-6 Surface and Hole Copper Plating Minimum Requirements for Buried via cores (2 layers) ........................................ 11
Table 3-7 Plating and Coating Voids Visual Examination ................... 13
Table 3-8 Edge Board Contact Gap ........................................... 15
Table 3-9 Minimum Annular Ring ............................................ 16
Table 3-10 Maximum Percent of Allowable Conductor Width Deviations .................... 18
Table 3-11 Percent of Allowable Conductor Space Deviations ....................... 19
Table 3-12 Percent of Allowable Conductor Width Reduction Caused By Pin Holes .......... 19
Table 3-13 Percent of Reduction In Dielectric Material Thickness .................. 19
Table 3-14 Plated-Through Hole Integrity After Stress .................. 24
Table 3-15 Cap Plating Requirements for Filled Holes .................. 32
Table 3-16 Microvia Contact Dimension .................................... 34
Table 3-17 Internal Layer Foil Thickness after Processing ..................... 34
Table 3-18 External Conductor Thickness after Plating .................. 35
Table 3-19 Solder Mask Adhesion ............................................ 37
Table 3-20 Dielectric Withstanding Voltages .................................. 37
Table 3-21 Insulation Resistance ............................................ 38
Table 4-1 Qualification Test Coupons .......................................... 41
Table 4-2 C=0 Sampling Plan per Lot Size .................................. 42
Table 4-3 Acceptance Testing and Frequency ................................ 43
Table 4-4 Quality Conformance Testing ...................................... 47
Qualification and Performance Specification for High Frequency (Microwave) Printed Boards

1 SCOPE

1.1 Statement of Scope  This specification covers end product inspection and test of high frequency (microwave) printed boards for microstrip, stripline, mixed dielectric and multilayer stripline applications with or without buried/blind vias, and metal cores. The printed board may contain embedded active or passive circuitry with distributive capacitive planes, capacitive or resistive components conforming to IPC-6017. The printed board may contain build up High Density Interconnect (HDI) layers.

1.2 Purpose  The purpose of this specification is to provide requirements for qualification and performance of high frequency (microwave) printed boards.

1.3 Performance Classification and Types

1.3.1 Classifications  This specification establishes acceptance criteria for the performance classification of high frequency printed boards based on customer and/or end-use requirements. Printed boards are classified by one of three general Performance Classes as defined in IPC-6011.

1.3.1.1 Requirement Deviations  Requirements deviating from these heritage classifications shall be as agreed between user and supplier (AABUS).

1.3.1.2 Space and Military Avionics Requirement Deviations  Space and military avionics performance classification deviations are provided in the IPC-6018CS Addendum and are applicable when the addendum is specified within the procurement documentation.

1.3.2 Printed Board Type  This specification will define eight types of high frequency (microwave) printed boards.

Type 1 – Single Sided
Type 2 – Double Sided
Type 3 – Homogeneous Dielectric Multilayer Construction
Type 4 – Mixed Dielectric Multilayer
Type 5 – Homogeneous Dielectric Multilayer with blind and/or buried vias
Type 6 – Mixed Dielectric Multilayer with blind and/or buried vias
Type 7 – Metal and/or composite backed printed boards, single sided or double sided
Type 8 – Multilayer metal and/or composite backed or core printed boards with or without blind and/or buried vias

1.3.3 Selection for Procurement  For procurement purposes, Performance Class shall be specified in the procurement documentation.

The documentation shall provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

The procurement documentation should specify the thermal stress test method to be used to meet the requirement of 3.6.1. Selection shall be from those depicted in 3.6.1.1, 3.6.1.1.1, 3.6.1.2 and 3.6.1.3. If not specified (see 6.1), the default shall be per Table 1-1.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

* Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1 and 3.6.1.1.1)
* Conventional (eutectic) reflow processes (see 3.6.1.2)
* Lead-free reflow processes (see 3.6.1.3)

IPC-6016, a sectional performance specification for HDI printed boards, was cancelled by the IPC. Relevant HDI conformance and acceptance criteria has been transferred to this revision of this specification.