Cleanliness Guidelines for Printed Board Fabricators

Developed by the Bare Board Cleanliness Assessment Task Group (5-32c) within the Cleaning and Coating Committee (5-30) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105
# Table of Contents

1 SCOPE ........................................................................ 1
  1.1 Introduction ........................................................... 1
  1.2 Why Printed Board Cleanliness is Important .... 1
  1.3 Terms and Definitions ........................................... 2

2 APPLICABLE DOCUMENTS .................................... 2
  2.1 IPC ......................................................................... 2
  2.2 American Society for Testing and Materials ...... 3

3 WATER QUALITY ..................................................... 3
  3.1 Cleaning Additives ................................................ 4

4 PREVENTATIVE MAINTENANCE ............................ 5

5 HANDLING AND ASSOCIATED SOILS ............... 5

6 FABRICATION PROCESSES ................................... 6
  6.1 Raw Material Selection – Laminate .......... 6
  6.2 Raw Material Storage ........................................... 7
  6.3 Copper Clad Laminate Preparation .......... 7
  6.4 Clean and Apply Inner Layer Photoresist .... 7
  6.5 Expose and Develop Photoresist ............. 8
  6.6 Etch Inner Layers .................................................. 8
  6.7 Outer Layer Imaging ............................................ 9
  6.8 Strip Photoresist .................................................... 9
  6.9 Layup for Lamination .......................................... 9
  6.10 Lamination .......................................................... 10
  6.11 Drill Holes .......................................................... 10
  6.12 Deburring, Etchback, and Desmear ........ 11
  6.13 Making Holes Conductive ......................... 11
  6.14 Application of Outer Layer Photoresist ...... 11
  6.15 Outer Layer Expose and Develop ........... 12
  6.16 Pattern Plate and Outer Resist ............... 12
  6.17 Etch Copper and Etch Resist Metal ........ 12
  6.18 Solder Mask Application and Development .. 13
  6.19 Processing Aids ................................................... 15
  6.20 Final Finish .......................................................... 15
  6.21 Outer Layer Marking ........................................... 16
  6.22 Depanelization and Routing .................... 16
  6.23 Electrical Test ...................................................... 17
  6.24 Packing / Board Storage / Shipment .......... 17

7 ASSESSING CLEANLINESS ................................. 17
  7.1 History of ROSE Testing ................................. 17
  7.1.1 Limitations .......................................................... 19
  7.1.2 ROSE and Printed Boards ....................... 20
  7.2 Ion Chromatography ........................................... 21
  7.2.1 Why IC Data is Better and Preferred .......... 21
  7.2.2 Why the Industry is Moving this Way ...... 21
  7.2.3 When to Test ....................................................... 22
  7.3 IPC-5704 ............................................................. 22
  7.3.1 Why These Ions? ................................................ 23
  7.3.2 IPC-5704 Samples .............................................. 24
  7.3.3 IPC-5704 Flexibility ........................................... 24
  7.3.4 Acceptance of IPC-5704 ............................. 24
  7.4 SIR Testing .......................................................... 25
  7.5 Other Tests .......................................................... 25
  7.5.1 Other Tests – Water Break Testing .......... 25
  7.5.2 Other Tests – Surface Energy ............... 25
  7.5.3 Other Tests – Water Drop Testing .......... 25
  (Comparative Tracking Index) .............. 25

8 REFERENCES ........................................................ 25

9 ACKNOWLEDGEMENTS ................................. 26

### Figures

- Figure 1-1 Examples of Dendritic Growth ................. 1
- Figure 1-2 Venn Diagram Illustrating Variables Affecting Electrochemical Failure ......................... 1
- Figure 6-1 Generic Fabrication Process for Multilayer Rigid Boards ............................................. 6
- Figure 6-2 Solder Mask Adhesion Problems Caused by Inadequate Rinse Prior to Application .......... 13
- Figure 6-3 Solder Mask Lifting from Conductor Due to Inadequate Rinse Prior to Application ........... 14
- Figure 6-4 Solder Mask Flaking Due to Inadequate Rinse Prior to Application ............................. 14
- Figure 6-5 Solder Mask Bubbling Due to Entrapped Volatiles .................................................... 14

### Tables

- Table 6-1 Develop and Strip Considerations ............... 8
- Table 7-1 Equivalence Factors for ROSE Testing Equipment ......................................................... 18
- Table 7-2 Inorganic Ions ........................................... 23
1 SCOPE

1.1 Introduction In many IPC standards development meetings, those individuals responsible for assessing the quality of incoming unpopulated printed boards have lamented the fact that bare printed board cleanliness is often an unknown quality parameter, often with undesired results. This is often due to the lack of understanding of materials and processes by the fabricator, or more often because the industry has driven margins so low that experienced process professionals cannot be retained by the fabricator.

Therefore, the IPC 5-32c Bare Board Cleanliness Task Group resolved to generate guidelines on those factors in the printed board fabrication process which can directly or indirectly affect the final cleanliness of packaged bare printed boards. This document is intended to be a general tutorial on items in the printed board fabrication process which can affect, directly or indirectly, cleanliness.

1.2 Why Printed Board Cleanliness is Important One of the aspects of printed board assembly reliability is electrochemical reliability, which is related to the residues left on an assembly. Some residues are benign while others are harmful. Electrochemical failure mechanisms are comprised of three elements: (1) an ionic residue; (2) an electrical potential or voltage gradient; and (3) moisture or humidity. All three must be present at some minimum level (which varies) for electrochemical failures to occur. Electrochemical failures are evidenced in two primary areas: (1) unacceptable leakage currents under humid conditions, and (2) electrochemical migration (dendritic growth). An example of dendritic growth can be seen in Figure 1-1.

The Venn diagram shown in Figure 1-2 is useful in understanding the relation between these three factors. The amount of impact can be visualized by considering the diameter of the individual circles to be proportional to the forcing function. As an example, if a device is operating in a very humid environment, the diameter of the humidity circle grows larger as does the electrochemical failure region. In addition, operating temperature and time can compound or accelerate these factors. Higher temperatures can increase dissolution of residues and can accelerate electrochemical reaction rates. If service lives are long, the risk of electrochemical failures increases.

Every printed board, or printed board assembly made from such boards, has a different cleanliness need. Unfortunately, not many assemblers or OEMs know how to determine how clean their assemblies have to be. There have been many instances where the present printed board cleanliness test methods, such as resistivity of solvent extract (ROSE) testing, have been inadequate to determine the true cleanliness of printed boards or assemblies.