Design Guide for the Packaging of High Speed Electronic Circuits

Developed by the IPC-2251 Task Group (D-21a) of the High Speed/High Frequency Committee (D-20) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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1 GENERAL

1.1 Purpose  The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope  The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal integrity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site (www.ipc.org).

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>ABT</td>
<td>Advanced Bipolar-CMOS Technology</td>
</tr>
<tr>
<td>AC</td>
<td>Advanced CMOS</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current (Time varying current)</td>
</tr>
<tr>
<td>ACQ</td>
<td>Advanced CMOS Quiet</td>
</tr>
<tr>
<td>ACT</td>
<td>Advanced CMOS TTL Compatible</td>
</tr>
<tr>
<td>ACTQ</td>
<td>Advanced CMOS TTL Compatible Quiet</td>
</tr>
<tr>
<td>AGP</td>
<td>Advanced Graphics Port Logic</td>
</tr>
<tr>
<td>AHC</td>
<td>Advanced High-Speed CMOS</td>
</tr>
<tr>
<td>AHCT</td>
<td>Advanced High-Speed CMOS TTL Compatible</td>
</tr>
<tr>
<td>ALS</td>
<td>Advanced Low Power Schottky Technology</td>
</tr>
<tr>
<td>AS</td>
<td>Advanced Schottky Technology</td>
</tr>
<tr>
<td>BCT</td>
<td>Bipolar-CMOS Technology</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>COB</td>
<td>Chip-On-Board</td>
</tr>
<tr>
<td>CTE</td>
<td>Coefficient of Thermal Expansion</td>
</tr>
<tr>
<td>CTE_{xy}</td>
<td>X and Y-Axis Coefficient of Thermal Expansion</td>
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<tr>
<td>CTE_{z}</td>
<td>Z-Axis Coefficient of thermal expansion</td>
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<tr>
<td>CTT</td>
<td>Center Tap Terminated Logic</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DIP</td>
<td>Dual In-line Package</td>
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<tr>
<td>DWB</td>
<td>Discrete Wiring Board</td>
</tr>
<tr>
<td>dV/dT</td>
<td>Delta Voltage/Delta Time (Edge Slew Rate)</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter Coupled Logic</td>
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<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
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<tr>
<td>ESD</td>
<td>Electro-Static Discharge</td>
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<tr>
<td>F</td>
<td>Fast Bipolar Logic Technology</td>
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<tr>
<td>FR-4</td>
<td>Flame Retardant Level 4, Epoxy Glass Dielectric Material</td>
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