



**IPC-2251**

# **Design Guide for the Packaging of High Speed Electronic Circuits**

Developed by the IPC-2251 Task Group (D-21a) of the High Speed/  
High Frequency Committee (D-20) of IPC

**Supersedes:**  
IPC-D-317A - January 1995  
IPC-D-317 - April 1990

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC  
2215 Sanders Road  
Northbrook, Illinois  
60062-6135  
Tel 847 509.9700  
Fax 847 509.9798

## Table of Contents

<b>1 GENERAL .....</b>	1	<b>4.4 Component Placement .....</b>	17
1.1 Purpose .....	1	4.4.1 Crosstalk Management.....	17
1.2 Scope .....	1	4.4.2 Impedance Control.....	17
1.3 Symbology, Terms and Definitions .....	1	4.4.3 Power Distribution .....	18
1.3.1 Symbology .....	1	4.4.4 Thermal Management .....	18
1.3.2 Terms and Definitions.....	2	4.4.5 System Cost.....	18
1.4 Units .....	6		
<b>2 APPLICABLE DOCUMENTS .....</b>	6		
<b>3 OVERVIEW .....</b>	6		
3.1 Decision Making Process .....	6	<b>5 ELECTRICAL CONSIDERATIONS .....</b>	18
3.2 Design Options.....	7	5.1 Power Distribution .....	18
3.2.1 System Electrical/Mechanical Constraints .....	7	5.1.1 System DC Model.....	18
3.2.2 Signal Integrity Design Constraints .....	8	5.1.2 Power Plane Impedance.....	19
3.2.3 System Electrical/Mechanical Requirements .....	9	5.1.3 Integrated Circuit Decoupling .....	20
3.3 Mechanical Requirements.....	9	5.1.4 Decoupling Capacitance and Plane Capacitance .....	22
3.3.1 Circuit Board.....	10	5.1.5 Device Power Dissipation.....	25
3.3.2 Hybrid.....	10	5.2 Permittivity .....	25
3.3.3 Component Packaging .....	10	5.2.1 Relative Permittivity .....	25
3.3.4 Thermal Management .....	10	5.2.2 Effective Relative Permittivity .....	25
3.3.5 Component Mounting .....	10	5.2.3 Frequency Dependence .....	26
3.4 Electrical Considerations .....	10	5.3 Lumped Capacitance Versus Transmission Line Environment .....	28
3.4.1 Power Distribution .....	10	5.4 Propagation Delay Time .....	30
3.4.2 Permittivity .....	10	5.4.1 Capacitive Line .....	30
3.4.3 Capacitive Versus Transmission Line Environment .....	11	5.4.2 Transmission Line.....	30
3.4.4 Propagation Time .....	11	5.5 Impedance Models .....	31
3.4.5 Characteristic Impedance .....	11	5.5.1 Microstrip .....	31
3.4.6 Signal Loading Effects.....	11	5.5.2 Embedded Microstrip.....	32
3.4.7 Crosstalk.....	12	5.5.3 Centered Stripline .....	33
3.4.8 Signal Attenuation.....	12	5.5.4 Dual-Stripline .....	33
<b>4 MECHANICAL CONSIDERATIONS.....</b>	12	5.5.5 Differential Pair Conductors .....	34
4.1 Printed Board .....	12	5.6 Loading Effects .....	36
4.1.1 Substrate Materials.....	12	5.6.1 Termination Resistors .....	36
4.2 Component Packaging .....	14	5.6.2 Reflections .....	36
4.2.1 Device.....	14	5.6.3 Minimum Separation.....	36
4.2.2 Connectors.....	14	5.6.4 Distributed Loading .....	38
4.2.3 Cables .....	15	5.6.5 Lumped Loading .....	39
4.3 Thermal Considerations .....	15	5.6.6 Radial Loading .....	40
4.3.1 System Level Impacts.....	15	5.6.7 Logic Signal Line Loading Models .....	41
4.3.2 Board Level Impacts.....	15	5.6.8 Timing Calculation.....	42
4.3.3 Device Level Impacts .....	16	5.7 Crosstalk.....	44
		5.7.1 Model.....	44
		5.7.2 Microstrip Transmission Line.....	46
		5.7.3 Embedded Microstrip Transmission Line .....	46
		5.7.4 Backward Crosstalk Amplitudes.....	46

5.7.5	Stripline .....	46	Figure 5-5	Capacitive and Transmission Line Current Pulses – A) is for a very short line and B) is for a long line .....	21
5.7.6	TTL/MOS Models.....	47	Figure 5-6	Fourier Transform .....	22
5.8	Signal Attenuation.....	47	Figure 5-7	Capacitor Equivalent Circuit .....	23
5.8.1	Resistive Losses (Skin Effect).....	47	Figure 5-8	(a) through (m) Typical Impedance Structures.....	27
5.8.2	Dielectric Losses.....	48	Figure 5-9	$\epsilon_r$ and tan $\delta$ versus frequency for FR-4.....	28
5.8.3	Rise Time Degradation .....	48	Figure 5-10	Capacitive Loading .....	30
5.9	Computer Simulation Program.....	49	Figure 5-11	Wire Over Reference Plane .....	31
5.9.1	Computer Simulation Models.....	49	Figure 5-12	Flat Conductor Surface Microstrip .....	32
5.10	Connectors .....	49	Figure 5-13	Flat Conductor Embedded Microstrip .....	32
5.10.1	Sensitivity .....	49	Figure 5-14	Flat Conductor Centered Stripline .....	33
5.10.2	Distributed Line Compensations .....	49	Figure 5-15	Wire Conductor Centered Stripline .....	33
5.10.3	Connector Types.....	49	Figure 5-16	Flat Conductor Dual Stripline (Asymmetrical Signals) .....	34
5.11	EMI Layout Considerations .....	49	Figure 5-17	Wire Conductor Differential Centered Stripline .....	34
5.11.1	Reasons for Considering EMI Layout .....	49	Figure 5-18	Flat Conductor Shielded Broadside Coupled Differential Stripline .....	35
5.11.2	Digital Edge Rates .....	50	Figure 5-19	Flat Conductor Nonshielded Broadside Coupled Differential Stripline .....	35
5.11.3	Suggested EMI Layout Practices .....	50	Figure 5-20	Flat Conductor Shielded Edge Coupled Differential Stripline .....	35
<b>6</b>	<b>PERFORMANCE TESTING .....</b>	<b>52</b>	Figure 5-21	Flat Conductor Shielded Edge Coupled Differential Dual Stripline .....	35
6.1	Impedance Testing .....	52	Figure 5-22	Flat Conductor Edge Coupled Differential Surface Microstrip .....	36
6.1.1	Principle of Impedance Testing Using a TDR .....	52	Figure 5-23	Flat Conductor Edge Coupled Differential Embedded Microstrip .....	36
6.1.2	Impedance Measuring Test Equipment .....	52	Figure 5-24	Net Illustrating Point Discontinuity Waveforms .....	37
6.2	Impedance Test Structures and Test Coupons ...	52	Figure 5-25	Addition of Two Pulses Traveling Opposite Directions .....	37
6.2.1	Test Structure Design.....	52	Figure 5-26	Distributed Line .....	38
6.2.2	Test Probes and Connections.....	53	Figure 5-27	Lumped Loading .....	39
6.2.3	Locating Impedance Test Structures .....	53	Figure 5-28	Short Distributively Loaded Cluster .....	39
6.2.4	A Simple Impedance Test Method .....	53	Figure 5-29	a) Lumped Loaded Transmission Line b) Equivalent Model .....	39
6.3	Stripline Impedance Test Coupon .....	53	Figure 5-30	Waveforms for a Lumped Capacitive Load ....	39
<b>Appendix A</b>	<b>.....</b>	<b>55</b>	Figure 5-31	Lumped Transmission Line .....	40
<b>Appendix B</b>	<b>.....</b>	<b>76</b>	Figure 5-32	Radial Loading .....	40
<b>Appendix C</b>	<b>.....</b>	<b>80</b>	Figure 5-33	Example Configuration .....	40
<b>Appendix D</b>	<b>.....</b>	<b>82</b>	Figure 5-34	Example of Radial Line .....	41

## Figures

Figure 3-1	High-Speed Packaging Design Concept .....	7	Figure 5-35	Net Configuration .....	41
Figure 4-1	Schematic of Information, Electrical Power and Enthalpy (Heat) Flows .....	16	Figure 5-36	Bus Configuration .....	41
Figure 4-2	Heat Flux vs. Component Area .....	16	Figure 5-37	Wired-AND Configuration .....	42
Figure 4-3	Component Placement Guideline .....	17	Figure 5-38	Multiple Reflections In A Transmission Line Between Two TTL Inverters .....	43
Figure 5-1	DC Distribution Model.....	18	Figure 5-39	Equivalent Circuit Example (top) with Corresponding Lattice Diagram (bottom) .....	44
Figure 5-2	DC Power Distribution System (Without Remote Sensing) .....	20	Figure 5-40	Predicted Driver (A) and Load (B) Waveforms for Figure 5-39 .....	44
Figure 5-3	Decoupling Impedance Modeling - Power Supply .....	20	Figure 5-41	Induced Crosstalk Voltages .....	45
Figure 5-4	Device Decoupling Model.....	21			

Figure 5-42	Crosstalk Voltages for a Line Terminated at Both Ends .....	45
Figure 5-43	Drivers and Receivers at a Common End .....	47
Figure 5-44	Drivers and Receivers at Opposite Ends.....	47
Figure 5-45	AC Noise Immunity for Selected TTL Families .....	48
Figure 6-1	TDR Impedance Test Coupon .....	54
Figure 6-2	Test Setup for Measuring Conductor Impedance (Suitable for Receiving Inspection) .....	54

**Tables**

Table 4-1	Wire Resistivity.....	13
Table 5-1	Copper Wire Characteristics .....	19
Table 5-2	Copper Busbar Resistances/ft .....	19
Table 5-3	Impedance for 0.1 $\mu$ F and 0.001 $\mu$ F DIP and 1206 Capacitors .....	23
Table 5-4	Typical Data for Some Logic Families .....	29
Table 5-5	Logic Model Classifications.....	36
Table 5-6	Connector Equivalent Bandwidth .....	50

# Design Guide for the Packaging of High Speed Electronic Circuits

## 1 GENERAL

**1.1 Purpose** The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

**1.2 Scope** The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal integrity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site ([www.ipc.org](http://www.ipc.org)).

## 1.3 Symbology, Terms and Definitions

### 1.3.1 Symbology

Symbol	Description
ABT	Advanced Bipolar-CMOS Technology
AC	Advanced CMOS
AC	Alternating Current (Time varying current)
ACQ	Advanced CMOS Quiet
ACT	Advanced CMOS TTL Compatible
ACTQ	Advanced CMOS TTL Compatible Quiet
AGP	Advanced Graphics Port Logic
AHC	Advanced High-Speed CMOS
AHCT	Advanced High-Speed CMOS TTL Compatible

IC	Integrated Circuit
K <sub>B</sub>	Backward Crosstalk
K <sub>F</sub>	Forward Crosstalk
L <sub>G</sub>	Ground Plane Inductance
L <sub>H</sub>	Low-High Signal Edge Transition
L <sub>P</sub>	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVCMOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology

ALS	Advanced Low Power Schottky Technology
AS	Advanced Schottky Technology
BCT	Bipolar-CMOS Technology
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE <sub>XY</sub>	X and Y-Axis Coefficient of Thermal Expansion
CTE <sub>Z</sub>	Z-Axis Coefficient of thermal expansion
CTT	Center Tap Terminated Logic
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
dV/dT	Delta Voltage/Delta Time (Edge Slew Rate)
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
F	Fast Bipolar Logic Technology
FR-4	Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs	Gallium Arsenide Technology
GTL	Gunning Transceiver Logic
GTL+	Gunning Transceiver Logic Plus
HC	High-Speed CMOS Technology
HCT	High-Speed CMOS TTL Compatible
HL	High-to-Low Signal Edge Transition
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IBuf	Input Buffer
IC	Integrated Circuit
K <sub>B</sub>	Backward Crosstalk
K <sub>F</sub>	Forward Crosstalk
L <sub>G</sub>	Ground Plane Inductance
L <sub>H</sub>	Low-High Signal Edge Transition
L <sub>P</sub>	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVCMOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology