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DFX Guidelines

Developed by the 1-14 DFX Subcommittee of the 1-10 Printed Board Design Committee of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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Design for Excellence (DFX) Guidelines

1 SCOPE

This document provides guidelines for establishing a best practice methodology for use in developing a formal DFX (Design for Manufacturing, Fabrication, Assembly, Testability, Cost, Reliability, Environment, Reuse) process for layout of printed board assemblies that utilize surface mount and through hole devices.

1.1 Purpose The document provides a DFX process framework to establish a discipline of design review necessary to perform a detailed analysis of manufacturability attributes commonly found in electronics hardware for fabrication and around which to model a printed board assembly.

1.2 Goals of This Document The goals of this document are to:

- Use a multi-discipline engineering assessment tactic on elements influencing DFX.
- Allow the user to establish standardized DFX checklist(s) for major design elements such as bare printed board fabrication, printed board assembly manufacturing, electrical testability, and elements influencing product reliability, reuse, and impact on environment.

1.3 Limitations of This Document Electronics hardware defined under this DFX review process is limited to features of influence on DFX for bare printed board and printed board assembly.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CH-65 Guidelines for Cleaning of Printed Boards and Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-325 Documentation Requirements for Printed Boards, Assemblies and Support Drawings

IPC-A-610 Acceptability of Electronic Assemblies

IPC-A-630 Acceptability Standard for Manufacture, Inspection, and Testing of Electronic Enclosures

IPC-SM-785 Guidelines for Accelerated Reliability Test of Surface Mount Solder Attachments

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPC-2221 Generic Standard on Printed Board Design

IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-2224 Sectional Standard for Design of PWBs for PC Cards

IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

IPC-2226 Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Guidelines for Stencil Design

1 www.ipc.org

IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies

IPC-7801 Reflow Oven Process Control Standard

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

2.2 SAE International[2]

GEIA-STD-0005-1 Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder

GEIA-STD-0005-2 Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems

2.3 IEEE[3]

IEEE Std 1500(TM)/IEC 62528 Standard Testability Method for Embedded Core-based Integrated Circuits

IEEE 1149.1 IEEE Standard for Test Access Port and Boundary-Scan Architecture

IEEE 1149.4 IEEE Standard for a Mixed-Signal Test Bus

IEEE 1149.5 IEEE Standard for Module Test and Maintenance Bus (MTM-Bus) Protocol

IEEE 1149.6 IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

IEEE 1149.7 IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

IEEE 1149.8.1 IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components

IEEE 1232 IEEE Standard for Artificial Intelligence Exchange and Service Tie to All Test Environments (AI-ESTATE)

IEEE 1450– IEEE Standard Test Interface Language (STIL) for Digital Test Vector Data

IEEE 1500 IEEE Standard Testability Method for Embedded Core-based Integrated Circuits

IEEE 1522 IEEE Standard for Testability and Diagnosability Characteristics and Metrics

IEEE 1532 IEEE Standard for In-System Configuration of Programmable Devices

IEEE 1581 IEEE Standard for Static Component Interconnection Test Protocol and Architecture

IEEE 1687 IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

IEEE 62525 (IEEE Std 1450) International Standard Test Interface Language (STIL) for Digital Test Vector Data

2.4 JEDEC[4]

JESD-B106-D Test Method B106C Resistance to Soldering Temperature For Through-Hole Mounted Devices

JESD22-A111 Evaluation Procedure for Determining Capability to Bottom Side Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices

2.5 Government

MIL-A-28870 General Specification for Assemblies, Electrical Backplane, Printed Wiring

MIL-P-50884 General Specification for Printed Wiring, Flexible and Rigid Flex

MIL-DTL-31000 Technical Data Packages

MIL-HDBK-454 General Guidelines for Electronic Equipment

MIL-STD-2119 Design Requirements for Printed-Wiring Electrical Backplane Assemblies

MIL-HDBK-2175 Department of Defense Handbook: Testability Handbook for Systems and Equipments (31-Jul-1995) [Supersedes MIL-STD-2175A]

2.6 Industry Standards and Guidelines

SMTA/TMAG Testability Guidelines 101E

2 www.sae.org
3 www.ieee.org
4 www.jedec.org