SURFACE MOUNT COUNCIL WHITE PAPER

Chip Mounting Technology (CMT)

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This Chip Mounting Technology (CMT) white paper is a status of the technology on various methodologies for mounting and interconnecting bare (unpackaged) active devices to various substrate materials. A review will be conducted of the currently available mounting techniques for Tape Automated Bonding, wire bonding, and Flip Chip, followed by an examination of the most commonly used substrate options of laminate, ceramic, and silicon. This paper, which represents the position of the Surface Mount Council, is being presented to describe the emerging integrated circuit chip mounting techniques that are emerging on the technology time horizon.

INTRODUCTION
The purpose of this paper is to investigate emerging chip attachment methods and define and classify the attachment methods for electronic systems designers and manufacturers today. The industry is on the threshold of the next generation of electronic packaging as the component density limitations of fine pitch technology are approached. Chip Mounting Technology is appearing on the technology horizon as a viable option to higher system densities. The name "Chip Mounting Technology" (CMT) was selected in keeping with the conventions of Through Hole Technology (THT), Surface Mount Technology (SMT), and Fine Pitch Technology (FPT). Throughout the paper, the terms "chip" and "device" will be used interchangeably to describe the integrated circuit die.

In the past decade, active device packaging has evolved from Through Hole Technology, with component leads on 2.54mm (.100") centers, to Surface Mount Technology with leads on 1.27mm (.050") and smaller centers. This has recently been followed by the evolution of Fine Pitch Technology with component leads on 0.63mm (.025") and 0.5mm (.020"). Through these evolutions the component package which contains the silicon die, or chip, has decreased in size while lead counts have increased dramatically. The reduction in die geometries has been the result of semiconductor technology improvements, particularly lithography. The package size reduction has been made possible by improvements in assembly capabilities. Through each evolutionary reduction in package size, component density on the various substrates has increased dramatically. The next evolution will call for simply removing the package, mounting the device to the substrate, and then making the interconnections to the substrate.

We recognize that there are some advanced electronics companies who have been practicing these "new" packaging concepts for years. If it were not for their pioneering efforts, technology would come to a standstill. The objective of this paper is to simply describe, and help bring the results of those innovative packaging efforts into the mainstream of electronic package design and manufacturing.

PACKAGING EVOLUTIONS
CMT as the next generation of
electronic packaging technology is a logical sequel to the earlier evolutions of component attachment methods. Electronic packaging began in the 1950's and has evolved through the following technologies to position the industry where it is today:

- Through Hole Technology (THT)
- Surface Mount Technology (SMT)
- Fine Pitch Technology (FPT)
- Tape Automated Bonding (TAB)
- Chip Mounting Technology (CMT)

The decision to use Chip Mounting Technology, the next generation of electronics packaging density, is driven by a number of factors. The following list, while not all inclusive, represents the major drivers. They are not ranked in any particular order of importance:

- Higher system operating frequencies
- Higher system packaging densities
- Increased input/output requirements
- Smaller lead pitches on devices
- Higher thermal loads and power dissipation
- Overall system size reductions

The incorporation of CMT does have some limitations which must be considered:

- Acquisition of 100% known good die
- Bare IC die handling
- Specialized assembly equipment required
- Chip encapsulation and metallurgy
- Manufacturing yields
- Advanced CAD tools required

### PACKAGING DRIVERS AND LIMITATIONS

**HIGHER FREQUENCY**

**Advantages:** One of the primary advantages of CMT in high frequency applications is the reduction of the distance between components. This translates directly to reduced signal propagation time in the system. In Figure 1 it can be seen that the interconnection between devices is a significant contribution (often over 50%) to system delays. When interconnect delays are reduced, overall system performance in terms of speed and noise reduction is greatly improved. As operating frequencies approach 100MHz, and device rise times shrink to 1 nanosecond and less, it will become necessary to reduce wiring delays.

**Disadvantages:** None.

**HIGHER SYSTEM DENSITY**

**Advantages:** CMT allows a significantly greater number of components or electrical functions to fit in a given space than Surface Mount or Fine Pitch technology. The benefit is a smaller system, or more functions in the same size system. The high density packaging afforded by CMT is also much lighter in weight, should weight be a consideration. Fundamentally, higher system densities result in lower system delays because chip-to-chip distances are reduced.

**Disadvantages:** This packaging technology may be very difficult or impossible to repair or rework after assembly and test. Therefore many assemblies employing CMT may tend to be modular and disposable in the event of a failure.

**INCREASED I/O COUNTS**

**Advantages:** Another obvious advantage of CMT is that the high Input/Output requirements of large chips can be handled with a relative amount of ease through the high density interconnection strategies described in this paper. There is no package level of interconnect available that would require the small I/O pitch of the chip itself to be brought out to the comparatively large lead pitch typically found on a Surface Mount package. Therefore, the maximum I/O counts of chips destined for CMT could be much greater than, for example, those destined for Fine Pitch packages.

**Disadvantages:** The higher interconnect density will drive substrate geometries down and layer
counts up, both of which make high yield manufacturing more difficult.

SMALLER LEAD PITCHES
Advantages: Most logic device packages with high I/O counts are available in Fine Pitch packages with lead pitches as stated above. In the package geometry trends in Table 1, we see device pitch decreasing over time, forcing substrate geometries down accordingly. Through these decreases, the component packing density can be increased on the substrate in terms of connections per square inch or per square centimeter. The budgetary component density calculations in Table 2 can assist in the decision making process by predicting whether or not the components will fit within the given substrate real estate area. There is a decision point at 100 connections per square inch, or greater, where the design engineer will leave the realm of SMT and cross over into CMT.

There is also a method of calculating the routing density according to Rent's Rule. This method uses a total number of routing channels available per square inch or centimeter and is driven by conductor width and spacing. Smaller geometries will produce greater routing densities. Table 3 and Table 4 list routing density in inches of wire per square inch of substrate.

Currently, the lower lead spacing threshold, or practical limit, is at approximately 0.5mm [.020"] pitch for most SMT packaged devices. A definite advantage of CMT is the ability to cross that threshold into smaller pitches in the range of 0.25mm [.010"] to 0.5mm [.020"] by removing the package and it's limitations.

Disadvantages: The smallest pitch that can be practically utilized is limited by the substrate choice. For example: PCB or ceramic substrates are limited to device pitches greater than 0.25mm [.010"] (0.13mm [.005"] bonding sites on 0.25mm [.010"] centers), while semiconductor substrates work well with pitches less than 0.5mm [.010"].

HIGHER HEAT GENERATION
Advantages: None.
Disadvantages: CMT is ushering in a whole new dimension of thermal management problems. Thermal requirements must now be thoroughly evaluated very early in the design process, prior to beginning any physical layout efforts.

SIZE
Advantages: The overall substrate level package size can be reduced by 50%, or more, over those using Fine Pitch Surface Mount devices.
Disadvantages: Design, fabrication, assembly, and test becomes significantly more challenging in every aspect with smaller, denser packaging.

CMT MOUNTING METHODS & SUBSTRATE TYPES
CMT MOUNTING METHODS
There are three basic mounting methods within CMT as shown in Figure 2: Tape Automated Bonding (TAR), Wire Bonding (WB), and Flip Chip. Within each of the mounting methods there are several methods which will be described later in the text.

SUBSTRATE TYPES
There are three basic types of substrates that could be used for the different CMT mounting methods. They are MCM-C, MCM-D, and MCM-L. As the different CMT methods are explored, the optimum substrate choices will be recommended. For purposes of this discussion, it is assumed that, by definition, a substrate is termed a Multichip Module whenever bare, or unpackaged, chips are directly attached and interconnected to it.

SUBSTRATE TYPES
MCM TECHNOLOGIES DEFINED
There are three types of Multichip Modules in use today according to
the Institute for Interconnecting and Packaging Electronic Circuits (IPC). They are identified by acronym-letter suffix as follows: MCM-C, MCM-D, and MCM-L. The letter designates the substrate material and its associated fabrication process.

**MCM-C: CERAMIC COFIRED SUBSTRATE**
The construction of this substrate is of ceramic or glass ceramic alternatives that have a relatively high dielectric constant greater than 5.0. Conductors with line widths of 0.13mm (.005") and larger are built up using layers of fired metals. The via interconnections between layers are built up at the same time as the conductors. Resistors may be cofired on the outer layer and laser trimmed to a precise value as the last step. All conductors and resistors are screened onto the substrate.

**MCM-D: DEPOSITED THIN FILM SUBSTRATE**
This process is similar to that of integrated circuit fabrication except the substrate is large enough to contain several bare dies. The base substrate is usually silicon with conductors between 1 micron and 1 mil wide, and vias built up with various suitable metals by vacuum deposition. The dielectric constant is generally less than 3.4.

**MCM-L: LAMINATED ORGANIC SUBSTRATE**
This is constructed using the common printed board materials and sequential lamination substrate fabrication processes. Line geometries of 0.08mm (.003") or greater are typically created with copper using the print and etch, or subtractive, method. Blind, buried, and through vias are drilled and plated, also with copper, making connections with various inner layers by design. This type of substrate will typically have higher layer counts of 10 – 50+ layers as needed to complete all of the interconnections. In addition, restraining layers may be incorporated in the layer stack-up to control X-Y expansion for Flip Chip applications.

Following substrate fabrication, the integrated circuits may be attached or mounted to the above MCM's by TAB, Wire Bonded, or Flip Chip assembly processes as described later in this paper.

**DESIGN FOR MANUFACTURABILITY**

**DFM VS YIELDS**
Design has a much greater influence on the manufacturability of a CMT assembly than on that of a surface mount assembly due to the significant reduction in geometries. All design efforts should take place in a Concurrent Engineering framework with yield optimization as a primary objective. The Concurrent Engineering team should be able to provide the designer with important information on process limitations specific to their fabrication or assembly operation, thus minimizing the risk associated with most emerging technologies. For example, the following design suggestions for MCM-L (printed circuit) substrates may help eliminate some common CMT manufacturing problems:

1. Define end product requirements prior to committing to any design efforts
2. Reassess overall corporate printed circuit board specifications in light of CMT
3. Determine which type of interconnection will be used as this will determine the substrate choice
4. Review all multilayer designs to see if the padcap architecture (pads only on outer layers) would make sense because fine lines can be produced with higher yields on inner layers
5. Make minimum sized features as large as possible
6. Employ grid based design rules to enhance testability
7. Utilize buried and blind vias to reduce high aspect ratio hole drilling and plating through the board
8. Utilize balanced construction from the center of a multilayer substrate out to the surface
layers to promote flatness.
9. Provide uniform copper density on the outer layers to promote feature size and thickness control.

There are also design rules for ceramic co-fired and thin film substrates.

Continuous process improvements must be implemented throughout the manufacturing process to maintain acceptable yields. This should be accomplished through the joint efforts of designers and manufacturers as they conduct frequent design reviews.

THE MANUFACTURING PROCESS

PROCESS OVERVIEW
The manufacturing processes for TAB, Wire Bonding, and Flip Chip begin after the substrate of choice has been fabricated. Fabrication process details have been intentionally omitted since they are not within the scope of the document. The basic manufacturing process steps are as follows:
- Substrate Fabrication
- Substrate Assembly
- Manufacturing Defects Analysis
- Burn-in & Functional test
- Device Encapsulation

The process details will be defined in the respective CMT categories later in this paper.

CHIP CONSIDERATIONS

INTEGRATED CIRCUITS
The layout of IC chips used for CMT are usually in the same relative form as those packaged in DIP or SMT packages. The chips are simply left unpackaged if they are destined for CMT. Either gold or aluminum chip metallization may be used, with gold or nickel or, in the case of TAB, even solder or conductive polymer on the substrate. The only requirement is that the metallization on the chip be compatible with the substrate for the type of interconnection to be used.

CHIP MOUNTING TECHNOLOGIES

TAP AUTOMATED BONDING (TAB)

There are basically two types of chips used for TAB or other TAB type lead bonding. Bumped chip bonding requires input/output (I/O) pads plated with gold bumps that will allow the inner lead bonding of TAB tapes, or circuitized TAB to the chip. Alternatively, bumped leads may be used, and the chip can then be identical to those used for wire bonding.

In the bumped chip method, bumps must be applied to the chip by evaporation/deposition. This must be accomplished prior to the dicing of the wafer. Bump application, therefore, is often done at the chip manufacturers location, although some vendors offer chip bumping service along with inner lead bonding. The structure of a typical chip bump is shown in Figure 3.

TAB ADVANTAGES
TAB has some advantages which will benefit users. An IC destined for TAB attach can be tested by the assembler after inner lead bonding, but prior to mounting on the substrate. Bare chips or chips intended for Wire Bonding currently cannot be tested by the assembler prior to assembly, however, much work is being done in this area and solutions should be forthcoming in the next year or two. The TAB package is likely to be the easiest to rework of the three methods which could be useful during prototyping or field service including repair and replacement.

TAB also eliminates the need for gold plating on the substrate since the outer lead bonding normally takes place through soldering. Two mass bonding or soldering methods available for TAB are hot bar or hot gas soldering. The hot bar forces the leads down into the solder and may not make a smooth fillet. Hot gas refloows the solder on the substrate then gently lowers the device leads into the molten solder forming a solder joint with smooth
fillets. There are also different methods for soldering TAB leads individually: laser, focused IR, and single point thermodcompression bonding.

When completed, the TAB assembly has advantages over wire bonding including low bond profiles and more compliant leads which enhance long term reliability.

**TAB CONSTRAINTS**

Historically, TAB lead frames have been costly to develop which made them prohibitively expensive for low volume applications. The lead frames for connection to the chips required specific designs which prevented them from being used in different applications. This has contributed to the high initial cost associated with TAB. The equipment used to assemble TAB components is less flexible than the equipment used in wire bonding due to the specific tooling requirements. Finally, from a high performance perspective, the TAB leads have higher resistance and lead inductance than wire bond leads.

**TAB DESIGN**

When designing for TAB CMT application, the method of outer lead bonding is critical to the substrate finish applied to the bonding pads. If the outer leads are to be attached with solder, then a solderable coating is required. If it is to be attached by thermodcompression, soft gold is required.

Finally, if it is to be outer-lead bonded using one of the newer anisotropic adhesives, a hard gold contact-type finish is desirable and should be readily available. However, if the board is a larger one, care should be taken to ensure that the printed circuit board manufacturer has the capability of selectively plating the entire board with gold, as some manufacturers equipment will not allow gold plating of large areas.

**TAB MANUFACTURING**

TAB is an assembly technology for connecting semiconductor devices to substrates. Basically, the process uses a specially plated tape etched in the desired conductor pattern. The tape may be single, two, or three layer construction. The conductors are etched into the pattern and are unsupported in the center area where the semiconductor chip is to be attached. TAB accomplishes this by means of a photo-imaged and etched pattern of conductors bonded to a dielectric tape. This carrier tape, which is usually stored on reels similar to movie film in widths from 8 to 70 mm, is commonly made from mylar or polyimide material. Windows are punched at specific locations in the tape and a thin, copper conductive foil is bonded to the tape. A conductor pattern of leads is etched in the foil, thus giving the desired interconnection circuitry with beam-type leads that extend over the window in the tape. Gold bumps are typically formed on either the tape or the chip itself. The IC is aligned on the tape and thermodcompression bonded to the inner leads of the tape. The outer leads bonding operation transfers the chip with its leads to the substrate.

**INNER LEAD BONDING**

Inner lead bonding can be used to simultaneously bond all the leads on a TAB tape to the chip. The leads are optically aligned to the chip. Positioning for this alignment is controlled by specially etched holes previously fabricated in the tape. The lead bonding process is usually a high speed solder or thermodcompression bonding technique. The solder process uses immersion tin plated leads and gold bumps on the chip to form a gold/tin eutectic. This method uses a relatively low bonding temperature (284 C) and low bonding pressure (75 grams per lead). Thermodcompression bonding uses gold plated leads to join to gold bumps. A typical thermodcompression cycle includes preheating the chip (200 C) prior to gang bonding the leads.
(approximately 375 C, 2.5 seconds, 200 ydmas per lead).

**BUMPED CHIPS**

Bumped chips are chips on which raised gold bumps have been fabricated on the pad areas. This operation seals the pads and provides some protection. The gold bumps are malleable enough to compensate for any non-planarity during inner lead bonding. Bumped chips are more reliable than regular chips, but require extra processing steps and, hence, are more expensive.

At this point, a chip slated for TAB can be processed in one of two ways. Early in the development of TAB, practitioners learned that reliable bonds could not be obtained unless "bumps" were added to the TAB leads or to the wafer pad area in order to obtain a planar surface. In the basic TAB approach, a barrier metal such as titanium-tungsten is deposited over the passivation on the pad as shown in Figure 3. This plus the addition of 0.025mm (.001") high gold bumps helps improve the reliability of the TAB connections to the tape during the inner-lead-bonding process.

The bumps on the chip are evaporated or electroplated onto the barrier metal at each pad position. Copper bumps can also be used, and both copper and gold can be tin plated. This completely seals the chip, and further enhances TAB's reliability as a CMT assembly process.

**BUMPED TAPE AUTOMATED BONDING (BTAB)**

Another processing approach, puts the bump on the tape rather than on the chip in Figure 4. This approach is known as BTAB. Bumped tape is TAB tape with a copper projection at the end of the lead. The bump is usually gold or immersion tin plated for inner lead bonding. The bump is formed by selective etching of a thick copper foil. This method of tape fabrication is limited to a single layer (copper foil) construction.

In both bumped chip and bumped tape, the bumps elevate the etched tape conductors above the chip to prevent shorting of the leads as well as to provide access to the bonding plane. The bumping process eliminates the need for forming the inner leads of the TAB tape prior to bonding.

**OUTER LEAD BONDING (OLB)**

The outer lead bonding process connects the chip with its leads to the substrate. OLB is a two step process usually performed sequentially on the component placement machine. The first step is to excise the chip with its leads from the TAB tape and form the leads. A vision system is required for precise alignment of the outer leads to the bonding pads. This is accomplished by referencing the lead pattern and then referencing a fiducial on the substrate. The outer lead bonding process may be completed by thermo-compression bonding, reflow solder, or conductive adhesive technology.

**WIRE BONDING**

The limited availability of bare integrated circuit chips has impeded the use of Wire Bonding Technology. Many potential Wire Bond designs have been done using the more expensive packaged device approach because only packaged devices were available. However, as Wire Bond technology gains acceptance as a less expensive and perhaps the only technology which will meet certain physical design requirements. Chip fabricators and assembly houses will form alliances to bring this technology to the market.

**WIRE BONDING ADVANTAGES**

Electrical interconnections from the device to the board are critical in Wire Bonding manufacturing and long term reliability. The traditional dominance of wire bonding is explained by its advantages over competing technologies:

- Adaptability to diverse metallizations
- Amenability to visual inspection
- Easily performed bond integrity tests
- History of satisfactory reliability
- Extensive base of expertise and equipment
- Relatively inexpensive for prototyping & low volumes

Another advantage of wire bonding is that it can be used in some cases to prototype a circuit designed for TAB prior to investing in a lead frame. Once a circuit is debugged and is operating satisfactorily, a TAB lead frame can be developed and implemented without changing the chip and substrate design.

WIRE BONDING CONSTRAINTS

Wire bonding has fewer constraints than the other CMT mounting methods because it has been established many years. There are, however, some constraints that should be listed:

- Substrate interconnections must be made one at a time
- Impedance control is not precise
- Encapsulation is mandatory
- Localized heating must be avoided on laminate substrates
- Selective deep gold plating required on substrates

WIRE BOND DESIGN

Chip areas for die and Wire Bonding substrates should follow guidelines for bond length and angles as shown in Figures 5 and 6. The suggested limits on these features appear in Table 5.

In order to obtain a design for a wire bonded structure that is manufacturable, the type of wire bonding process to be used must be considered a critical factor.

When thermocompression (TC) bonding must be used, the gold plating requirements are similar to those needed for thermosonic bonding. However, selection of the substrate is critical, because organic substrates cannot withstand the high bond temperatures required.

With thermosonic bonding (TS), some high Tg organics, such as 150°C BT epoxy and 260°C polyimide, may be processed. Substrate plating materials and thickness should be 40-50 microinches of soft gold plated over 50-200 microinches of nickel.

If ultrasonic bonding (usually with aluminum wire bonded at room temperature) is to be used, the substrate can be any accepted circuit material, with 5-15 microinches of soft gold plated over 50-200 microinches of nickel.

Whichever style of wire bonding is chosen for these designs, guidelines for the layout of the chip area on the substrate are process dependent and will require verification for each application.

WIRE BOND MANUFACTURING

When shipping bare, unprotected IC chips, one must choose the form in which the chips are transported from silicon fabricator to assembler. With TAB, this form is tape, but with the chip and wire technique, there is a choice of methods: Waffle packs, Wafer form, or chip-in-tape. Automatic pick-and-place systems for chip placement can usually accept dice either in waffle packs or in diced wafer form. In the case of the wafer, defective chips are indicated by the presence of an ink dot placed on each bad chip when tested at the manufacturer in wafer form, or they can have a "wafer map", a paper or software record of defective chip locations on the wafer.

At the assembly site, the chips are picked up by a pick-and-place machine and placed at a bond site on the substrate. The chips must be placed precisely in X-Y, rotational, and Z axes.

Thus, the technology used to make the IC chips for Wire Bonding is less of a concern than the method of shipment. When the chip manufacturer and the substrate assembler are the same, there is no problem. If they are different organizations, a close user-vendor relationship must exist.

Chip attach adhesives are various
bonding agents, listed in Table 6, that are used to bond bare chips to the substrate. Thermoset, one part, thermally and electrically conductive epoxies, are most popular. An alternative to one-part systems is a two-part system which is cured at room or slightly elevated temperature. Once mixed, the two-part epoxy has limited life and must be used quickly. As with other mounting processes, epoxy bonding involves trade-offs. Certain precautions must be taken:

- There are many types of conductive epoxies. Epoxies used for wire bonding must be low in ionic contaminants, low in outgassing and formulated for this purpose.
- When thermocompression wire bonding a chip, use a bonder with a heated probe tip since the heat associated with some other types of thermocompression wire bonding will soften the epoxy.
- Some semiconductor chips have gold backing in order to alloy the gold with the silicon. If the gold is vapor deposited, epoxy can pull it away from the chip and form a high resistance contact.

In summary the advantages for using epoxy adhesives include:

- Low temperature cure
- Ease of processing
- Ease of handling
- Ease of repair
- High yield ruggedness
- Bond compliance

Bonding wire for microelectronics assembly is a precision metallurgical product developed for the semiconductor industry. In order for a device packaging line to operate effectively, the yield of acceptable wire bonds must approach 6 Sigma quality levels. This places stringent quality standards on the wire. In addition, semiconductor manufacturers seek to maximize yields by optimizing wire to their particular chip metallizations, package constructions, and bonding machine configurations; therefore, there is no "standard" bonding wire. Some available bonding wire diameters are shown in Table 7. Furthermore, the wire from one wire manufacturer is not necessarily interchangeable with that from another. Bonding wire is a highly specialized product made by relatively few producers, each of whom employs guarded proprietary processes.

Despite the maturity of the wire bonding process, it is by no means static. Improvements are continuously being made in all of the variables including the wire, the bonding surfaces, the equipment, and especially the bonding processes themselves. Figure 7 shows a number of bonding variables.

There are three well developed methods for making wire connections: Ultrasonic bonding, thermocompression bonding, and thermosonic bonding as shown in Table 8. THERMOCOMPRESSION (TC) bonding is accomplished by pressing gold wire against the bond site metallization at an elevated temperature. Because of the high temperatures, organic based substrates are not used with this process. ULTRASONIC bonding uses ultrasonic energy to weld wire to the chip pad and circuit pad. The process takes place at room temperature. Aluminum wire is used almost exclusively for ultrasonic bonding, though gold and copper wires have been used successfully. THERMOSONIC (TS) bonding combines the principle features found in ultrasonic and thermocompression bonding. Thermosonic bonding temperatures are lower than in thermocompression bonding. Thermosonic bonding has been particularly successful in attaching wires to hard-to-bond thick film hybrid substrates.

**FLIP CHIP**

Flip-chip technology avoids conventional chip bonding. No adhesive is used, because the semiconductor chip is "flipped-over" such that its conductive pattern contacts the conductive circuitry of
the substrate. Therefore, the equivalent of chip attach and wire bonding are accomplished in one operation.

FLIP CHIP ADVANTAGES
Flip chip interconnection technique requires a specialized body of knowledge related to solders, their deposition, and the reflow process. However, the use of this technology will be driven by the many advantages of this chip mounting technique which include:

- Efficient use of substrate area
- Shortest interconnect path between devices
- All connections are made simultaneously
- Most dense interconnect method available
- Area array interconnection possible
- Very low device profile
- Fast manufacturing throughput times
- Reworkability is simplified
- Has been in use for over 10 years

The primary advantage of the Flip Chip option is that it provides the highest density of all CMT methods because it requires no additional interconnection scheme.

FLIP CHIP CONSTRAINTS
This method of CMT is the least understood of all the CMT mounting methods. As a result, there are many constraints which must researched and optimized before Flip Chip can be utilized effectively. Among the constraints are:

- Limited availability of bumped chips
- Requires precise alignment
- Requires matched TCE or SLC encapsulation
- Difficult or impossible to inspect
- Requires precise solder volume
- Cleaning under chip difficult
- Area array design rules must be employed

One solution to the availability problem is to produce the bump as a part of the interconnecting substrate, rather than as a part of the chip. The CMT assembler can then use any device available in bare chip form without bumps.

A major constraint of the flip chip technique is its limited heat transfer and dissipation. Since the chip is joined to the substrate only by the solder joint interconnection, rather than the entire back side of the chip, there is limited area for heat conduction into the substrate. One remedy is to incorporate non-functional thermal pads onto the silicon chip in presently unused connection areas. These pads would mate with heat sinking pads on the substrate, which could then connect to thermal vias in the substrate.

FLIP CHIP DESIGN
Flip chip or face bonding interconnection technique requires an interconnection substrate capable of very small geometries.

In this technique, multiple plating operations deposit a specific thickness of a given tin-lead composition onto the semiconductor device's interconnection pads, which are typically 0.1mm - 0.25mm (.004" - .010") square. Matching pads are imaged onto the substrate and are also plated with a solderable surface, i.e. copper (coated with an anti-oxidant), tin-lead, tin or gold. It must be pointed out that the fine pitch of the I/O pads on an IC chip is very difficult to fabricate on the surface layers of a printed circuit (lamine) board substrate. The chip is subsequently "flipped" to mate with the respective pads or "bumps", which are joined during a solder reflow process, thereby completing the connections simultaneously. If gold is used as the metallization on the substrate, keep it very thin (3-10 microinches) in order to provide as much solder volume as possible, and limit the formation of brittle gold-tin intermetallic alloy. If bare copper is the substrate metallization, it may be desirable to coat the pads with molten solder by a solder leveling process in order to improve solderability and increase the volume of solder for a more ductile and forgiving joint;
however, if such a process is used, take care to insure uniformity of
deposited solder height and volume
among all the pads for a given chip,
since deviations greater than .0002" ([U.UUmmm] may lead to open circuit
conditions after the reflow solder
assembly process step. It is
important to note that in advanced
technology packaging such as this,
the product and the manufacturing
process must be designed
simultaneously.

The design requirements for
adequately matching the coefficients
of expansion between silicon and the
substrate is becoming less critical
in the flip chip interconnection
technique. An SLC encapsulation
technology is currently under
development where an epoxy
encapsulant is applied to the flip
chip bonding site that restricts the
CTE mismatch between chip and
substrate. This new SLC technology
should provide a better CTE match in
order to prevent fracture of the
solder joints during thermal
cycling.

FLIP CHIP MANUFACTURING

Flip chip technology is based on a
use of controlled-collapse circuit
connection also known as C4. The
original flip chip concept employed
small, solder-coated copper balls
sandwiched between the chip
termination lands and the
appropriate pads on the
interconnecting substrate. The
resultant solder joints are made
when the unit is heated. However,
handling and placement of the small
diameter balls was extremely
difficult and costly.

In a more advanced technique, a
raised metallic bump or lump,
usually solder, is provided on the
chip termination pad. This is
normally done on all pads of all
chips while they are still in the
large wafer form. The individual
chip is then aligned to
the appropriate circuitry on the
substrate and bonded in place using
reflow soldering techniques. In this
way, the interconnection bonds
between the chip and the substrate
are made simultaneously, reducing
fabrication costs.

Flip chips with controlled-collapse
bonding have potential for very high
assembly rates. For example, with
only the use of simple
optomechanical assists, manual chip
placement rates as high as 200 per
hour have been achieved. This is a
very high assembly/bonding rate,
especially for chips with many
input/output terminations which
would require much more assembly
time using other techniques. To
data, flip chip devices have been
limited to very special packaging
applications. Whether or not these
can be considered to be CMT
applications depends on the
operative definition of the
substrate (board or other), since
most of the applications currently
use ceramic. Flip chip has
historically been used on ceramic
substrates instead of printed
circuit board substrates because of
the large difference in coefficient
of thermal expansion (CTE) between a
silicon chip and an organic-based
board.

Some methods of flip chip attachment
which use conductive polymer
attachment instead of solder require
only that the I/O pads of the chip
allow good adhesion and electrical
connection to the conductive polymer
used. For instance, aluminum pads on
a CMOS chip may require gold
metallization. No further
restrictions on size or technology
of the die apply. However, like most
Wire Bonding applications, heat
transfer could limit the types of
chips that could be attached this
way.

In recent years, the printed circuit
board (lamine) has progressed to
the point of equaling up ceramic in
many ways. Developments in aramid
and graphite reinforced organic
materials now make a laminate
substrate possible. Normal printed
circuit board materials such as E-
glass reinforced epoxy, triazine or
polyimide, as well as the newer
thermoplastic resins, e.g.,
polysulfone, polyetherimide, and polyphenylene sulfide, have expansion coefficients too large for the reliable attachment of chips with the flip chip technique. However, recent efforts directed towards achieving reliable attachment of leadless ceramic chip carriers (TCE of 6-8 ppm/C) to printed circuit boards can be adapted to flip chip technology. Specifically, by substituting an aramid fiber, such as Kevlar-TM, for the E-glass fiber in conventional laminates and by limiting the resin content to the range of 40-50%, an organic substrate with a thermal expansion coefficient of 4-8 ppm/C can be achieved. Alternatively, low thermal expansion coefficient metals such as Invar, Alloy 42, copper-Invar-copper or copper-molybdenum-copper, can be incorporated into the organic substrate, either as a thick .020"-.060" (0.5-1.5mm) or as thin .004"-.010" (0.1-0.25mm) planes within a multilayer printed circuit board. This technique yields similar expansion coefficients as the aramid reinforcement, but may be cheaper.

In summary, a substrate for flip chip interconnections must have a controlled and highly solderable surface, a thermal coefficient of expansion rate that closely matches that of silicon (or SLC encapsulation technology used), and thermal enhancements to handle the limited heat transfer capabilities of this interconnection technique.

CHIP ENCAPSULATION

CHIP PROTECTION FOR CMT

After the chip has been mounted to the substrate, there is a requirement for mechanical, chemical and electrical protection of the chip. This requirement is addressed in the following text:

CHIP PASSIVATION

The two most common passivation films available in integrated circuit chips are either silicon dioxide or silicon nitride. Of these, silicon dioxide, a clear, glass-like material is applied most commonly to chips by the manufacturer to be the "first line" of moisture protection. Silicon nitride, a gold colored compound, is used sometimes for this purpose. Either of these films is applied during chip manufacture in an extremely thin layer over the active surface of the chip, except that it is imaged so as to leave the I/O pads of the chip open for wire bonding or for access for TAB inner lead bonding. Organic materials, notably polyimides, have also been used for this purpose.

ENCAPSULATION

The "second line of defense" against the moisture and ionic contaminates that could cause corrosion of the thin aluminum conductors on the chip is the encapsulation material applied to the assembly after the chip has been interconnected. This can be one of many organic materials, and its method of application could vary for each material. But the purpose of each of them is to provide environmental protection (physical, mechanical, chemical, and electrical) to the chip and its exposed interconnection pad areas.

No matter how perfectly any CMT assembly is encapsulated with an organic material, it will never be hermetic. A hermetic seal is one that has a very low moisture leakage rate. Unfortunately, all organic materials have a higher degree of permeability to water. High hermeticity can only be achieved by a glass and/or metal barrier continuously and completely around the chip.

However, just as plastic DIP packages have proven reliable in many applications, and have replaced hermetic packages, CMT is a good candidate for some of those applications as well.

There are two classes of encapsulants currently in use today, silicones and epoxies. Silicones are soft materials that exhibit a high resistance to water vapor
permeation, although all organic materials are permeable to water and water vapor to some extent. Silicone materials, when used as an encapsulant in certain applications, have shown reliability in long term testing that rivals true hermetic packages. Soft encapsulants, such as silicones, typically exhibit poor resistance to aggressive solvents. Epoxies are hard materials which provide good mechanical protection and resistance to a variety of aggressive chemicals, when used as a CMT encapsulant. A new generation of epoxies has been developed that provide a good balance of electrical, mechanical, and chemical protection. These new epoxies may be used for high reliability applications.

In the future, conformal coating may be used to encapsulate substrates containing CMT devices. There are new generations of clear conformal coatings that can be put on the substrate in thin applications rendering them practically invisible.

**IMPACT ON TESTABILITY**

Surface Mount Technology moved the test industry from a .100" test grid to .050" grid for testing. CMT is likely to reduce that further down to .025" grid. Any test grid below this makes it practically impossible to do any fixed probe testing of the bare substrate. If the component land pattern for the CMT attach method cannot bring all signals to at least a .025" grid, then another method of test or combination of tests will have to be developed. Automatic Optical Inspection could be improved and provide verification, but this approach could not test the vias. If the pitch is too small to test with probes, then we may consider the electron beam capacitance test to verify the nets on the bare substrate prior to releasing it for assembly. Following assembly, the loaded substrate could be functionally tested through the connector or through the emerging built in self test strategies.

**SUBSTRATE TESTABILITY**

An optimum test philosophy that facilitates 100% substrate level testability would contain the following points:

- Strategic placement of all component vias
- Provide access to every node of every net
- Access every node from either side of the board
- Grid based via and component placement
- Correct test pad geometries and clearances
- Do not probe directly to SMT component lands
- Support Boundary Scan techniques

**ASSEMBLY TESTABILITY**

There are three categories of test for the completed CMT assembly:

- Electrical characteristics
- Mechanical integrity
- Functional reliability

The electrical test is performed to verify the electrical parameters of the device. Functional testing is done to assure that the assembly being qualified meets the electrical functional characteristics and basic function at minimum and maximum temperatures and power supply voltages. Functional testing can be geared toward a single specific application, and all parameters and functions not used in that application need not be tested. The mechanical tests are performed to assure the mechanical and physical qualifications of an assembly.

The following list of mechanical characteristics, which could be generally ignored in surface mount or fine pitch assemblies, now need to be tested in CMT assemblies:

- Conformance to design rules
- Die bonding integrity
- Substrate bonding integrity
- Solvent resistance
- Solderability
- Plating type and thickness
- Flammability
- Construction analysis
CONCLUSION

There are three component mounting methods within CMT: Tape Automated Bonding (TAB), Wire Bonding, and Flip Chip. CMT for IC Chips and MCM for substrates will be developed concurrently. In general, TAB devices may be attached to MCM-L or C, Wire Bonded devices to MCM-C, D or L, and Flip Chip devices to MCM-D. As geometries and materials advance, it will be possible to mount TAB, Wire Bonding, and then Flip Chip devices on MCM-L substrates. From a cost and time perspective, the MCM-L substrate is the most advantageous and will likely emerge as the packaging method of choice over the next few years.

REFERENCES

JMC TR 001 Tape Automated Bonding and Fine Pitch Technology.

ANSI/IPC-SM-784 Guidelines for Chip-on-Board Technology Implementation.

IPC-MC-790 Guidelines for Multichip Module Technology Utilization.


FIGURES
Figure 1 IBM Case Study of Wiring Delays
Figure 2 Three Component Mounting methods
Figure 3 Interconnection geometry of bumped chip TAB
Figure 4 Interconnection geometry of bumped-tape TAB (BTAB)
Figure 5 Wire bonding guidelines
Figure 6 Wire bonding layout features
Figure 7 Bonding variables

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Table 1 Package Geometry Trends
Table 2 Component Density Calculation
Table 3 Connectivity of Various Interconnects
Table 4 Connection Density
Table 5 Wire bonding features
Table 6 Various bonding adhesive types
Table 7 Aluminum and gold wire sizes and ratings
Table 8 Wire bonding comparisons

APPENDIX
Appendix A Terms & Definitions See IPC-SM-784 Page 2 - 5
IBM Case Study: Wiring Delays as a Fraction of Total Delays

source: IBM

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Figure 1
THREE CHIP ATTACHMENT METHODS

TAB LEAD FRAME

MCM-L SUBSTRATE

WIRE BONDING

MCM-L SUBSTRATE

FLIP CHIP

MCM-L SUBSTRATE

Figure 2
Figure 3  Interconnection geometry of bumped-chip TAB
Figure 4  Interconnection geometry of bumped-tape TAB (BTAB)
There are a number of variables that occur in either wedge or ball bonding. These are assembled for easy reference (24).

50 Bonding variables. There are a number of variables that occur in either wedge or ball bonding. These are assembled for easy reference. (Taken from a document titled "A Guide to Improved Bonding Wire" written by John Kleis, and published by Cooper Wire, Stern Metals Inc., 23 Frank Mossberg Dr., Attleboro, MA 02703, 617/222-6773).

Figure 7
## PACKAGE GEOMETRY TRENDS

<table>
<thead>
<tr>
<th>GEOMETRY</th>
<th>SMT'87</th>
<th>FPT'90</th>
<th>UFT'93</th>
<th>MCM'95</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEVICE PITCH</td>
<td>.050&quot;</td>
<td>.025&quot;</td>
<td>.015&quot;</td>
<td>.010&quot;</td>
</tr>
<tr>
<td>VIA GRID</td>
<td>.050&quot;</td>
<td>.050&quot;</td>
<td>.025&quot;</td>
<td>.010&quot;</td>
</tr>
<tr>
<td>DRILL SIZE</td>
<td>.018&quot;</td>
<td>.013&quot;</td>
<td>.010&quot;</td>
<td>.008&quot;</td>
</tr>
<tr>
<td>ROUTING GRID</td>
<td>.012&quot;</td>
<td>.010&quot;</td>
<td>.006&quot;</td>
<td>.005&quot;</td>
</tr>
<tr>
<td>LINES / SPACES</td>
<td>.006&quot;</td>
<td>.005&quot;</td>
<td>.003&quot;</td>
<td>.002&quot;</td>
</tr>
<tr>
<td>Cu THICKNESS</td>
<td>.0014&quot;</td>
<td>.0007&quot;</td>
<td>.0004&quot;</td>
<td>.0002&quot;</td>
</tr>
<tr>
<td>CKT DENSITY</td>
<td>50 CSI</td>
<td>100 CSI</td>
<td>200 CSI</td>
<td>400 CSI</td>
</tr>
<tr>
<td>LAYER COUNTS</td>
<td>8-10</td>
<td>10-12</td>
<td>12-18</td>
<td>18-24</td>
</tr>
</tbody>
</table>

PADCAP ARCHITECTURE WILL DOMINATE MCM-L

*Table 1*
SMT COMPONENT DENSITY CALCULATION

0 - 40 LSI = THROUGH HOLE COMPONENTS
40 - 60 LSI = SURFACE MOUNT SINGLE SIDE
60 - 80 LSI = SURFACE MOUNT DOUBLE SIDED
80 - 160 LSI = SURFACE MOUNT DENSE MEMORY
160 - 400 LSI = MULTICHIP MODULES

LSI - LEADS PER SQUARE INCH
USE 10 LSI / ROUTING LAYER TO BUDGET LAYER COUNTS
RANGE IS FROM SIMPLE PCB'S TO MULTICHIP MODULES
50 CSI EQUALS 8 CONNECTIONS PER SQUARE CENTIMETER
# Connectivity of Various Interconnects

(No. of Conductors/Inch/Level)

<table>
<thead>
<tr>
<th>Cond. Width</th>
<th>Connectivity/Level</th>
<th>Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>mills</td>
<td>microns</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>250</td>
<td>50</td>
</tr>
<tr>
<td>5</td>
<td>125</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>50-70</td>
</tr>
<tr>
<td>4 (dia.)</td>
<td></td>
<td>60-80</td>
</tr>
<tr>
<td>3</td>
<td>75</td>
<td>165</td>
</tr>
<tr>
<td>2.5 (dia)</td>
<td></td>
<td>160</td>
</tr>
<tr>
<td>2</td>
<td>50</td>
<td>250</td>
</tr>
</tbody>
</table>

Table 3
### CONNECTION DENSITY

<table>
<thead>
<tr>
<th>#/comp.</th>
<th>DIP inch wire/ in² of substr.</th>
<th>CHIP CARRIERS inch wire/ in² of substr.</th>
<th>TAB inch wire/ in² of substr.</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>40</td>
<td>80</td>
<td>200</td>
</tr>
<tr>
<td>44</td>
<td>43</td>
<td>123</td>
<td>309</td>
</tr>
<tr>
<td>68</td>
<td>44</td>
<td>139</td>
<td>347</td>
</tr>
<tr>
<td>156</td>
<td>—</td>
<td>160</td>
<td>399</td>
</tr>
</tbody>
</table>

Table 4
<table>
<thead>
<tr>
<th>Wire Bonding Process</th>
<th>0 Degrees</th>
<th>A (min.)</th>
<th>B (min.)</th>
<th>C (min.)</th>
<th>D (min.-max.)</th>
<th>E (min.)</th>
<th>F (min.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gold Thermocompression/Thermosonic</td>
<td>60-120</td>
<td>0.1 mm [0.004]</td>
<td>0.1 mm [0.004]</td>
<td>0.15 mm [0.006]</td>
<td>1.0-2.5 mm [0.040-0.100]</td>
<td>0.5 mm [0.006]</td>
<td>0.1 mm [0.004]</td>
</tr>
<tr>
<td>Aluminum Ultrasonic</td>
<td>60-120</td>
<td>0.08 mm [0.003]</td>
<td>0.125 mm [0.005]</td>
<td>0.15 mm [0.005]</td>
<td>1.0-2.5 mm [0.040-0.100]</td>
<td>0.125 mm [0.005]</td>
<td>0.08 mm [0.003]</td>
</tr>
</tbody>
</table>

* For 0.025 mm [0.001 inch] diameter wire

Table 5
### Various Bonding Adhesive Types

<table>
<thead>
<tr>
<th>Type</th>
<th>Advantages</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phenolics</td>
<td>Very high bond strength</td>
<td>Used mostly for structural applications, possibly corrosive, difficult to process at low temperatures.</td>
</tr>
<tr>
<td>Pdyurethanes</td>
<td>Easy to rework</td>
<td>Not suitable for temperatures above 120°C, relatively high outgassing, some decomposition.</td>
</tr>
<tr>
<td>Polyamides</td>
<td>Easy to rework</td>
<td>High moisture absorption, high outgassing, varations in electrical insulation properties, especially when exposed to high humidity.</td>
</tr>
<tr>
<td>Polymides</td>
<td>Very high temperature stability</td>
<td>High cure temperatures, require solvents as vehicles, voiding.</td>
</tr>
<tr>
<td>Silicones</td>
<td>High temperature stability, easy to rework, high purity, low outgassing.</td>
<td>Moderate to poor bond strength, high coefficient of thermal expansion, corrosivity, voiding.</td>
</tr>
<tr>
<td>Epoxyes</td>
<td>Some are easy to rework by thermomechanical means, some are low outgassers, easy to process, can be filled to 60-70 percent with a variety of conductive or nonconductive fillers.</td>
<td>Depending on type of curing agent used and degrees of cure: outgassing, catalyst leaching, corrosivity.</td>
</tr>
<tr>
<td>Cyanoacrylates</td>
<td>Very rapid setting (10 sec.), give very high initial bond strengths</td>
<td>Bond strengths often degrade under moist or elevated temperature (150°C) conditions, corrosivity.</td>
</tr>
</tbody>
</table>

*Table 6*
### Aluminum and Gold Wire Sizes and Ratings:

<table>
<thead>
<tr>
<th>Wire Minimum diameter (mm/inch)</th>
<th>Standard Wires</th>
<th>Resistance (Ωft.)</th>
<th>Resistance (Ωft.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Aluminum 1% Si (Hard)</td>
<td>Aluminum 1% Si (Annealed)</td>
<td>Gold</td>
</tr>
<tr>
<td>0.0018</td>
<td>X</td>
<td>36.06-39.86</td>
<td>34.62-38.273</td>
</tr>
<tr>
<td>0.0025</td>
<td>X</td>
<td>17.67-19.53</td>
<td>16.0-18.75</td>
</tr>
<tr>
<td>0.050/C.002</td>
<td>X</td>
<td>4.41-4.88</td>
<td>4.23-4.68</td>
</tr>
</tbody>
</table>

1. ASTM F487
2. ASTM F72

Table 7
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Thermo compression (Gold Wire)</th>
<th>Automatic Thermosonic (Gold Wire)</th>
<th>Ultrasonic (Gold &amp; Aluminum Wire)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Develop &amp; control</td>
<td>Excessive capillary heat may cause annealing (softening) of the wire and affect ball formation.</td>
<td>Easiest to control</td>
<td>Must control acoustic energy &amp; force</td>
</tr>
<tr>
<td>Speed**</td>
<td>~20 wires/minute (manual rate)</td>
<td>~600 wires per minute***</td>
<td>~240 wires per minute***</td>
</tr>
<tr>
<td>Current carry (0.001 inch*))</td>
<td>~0.55 amps</td>
<td>~0.15 amps</td>
<td>&lt;0.40 amps</td>
</tr>
<tr>
<td>Heat required</td>
<td>Heated work stage 300-400°C (pulsar capillary heat optional)</td>
<td>150°C work stage</td>
<td>No heat required (typical for aluminum wire)</td>
</tr>
<tr>
<td>Acoustic energy required</td>
<td>None</td>
<td>Controllable</td>
<td>Controllable</td>
</tr>
<tr>
<td>Force required</td>
<td>Most force required</td>
<td>Less than ultrasonic &amp; thermo-compression</td>
<td>Less than thermocompression</td>
</tr>
<tr>
<td>Direction</td>
<td>Omnidirectional (360°)</td>
<td>Omnidirectional (360°)</td>
<td>Straight line bond ± 7.5° off true line</td>
</tr>
<tr>
<td>Looping</td>
<td>Some control — operator dependent</td>
<td>Bes control (machine controllable)</td>
<td>Good control / machine controllable</td>
</tr>
<tr>
<td>Pad size (0.001 inch Dia.)</td>
<td>Ball size dependent wedge size = 1.5X to 5X wire diameter in length and 1.5X to 3X wire diameter in width</td>
<td>Ball size dependent wedge size = 1.5X to 5X wire diameter in length and 1.5X to 3X wire diameter in width</td>
<td>Wedge size dependent width = 1.2X to 2.5X wire diameter length = 1.5X to 5X wire diameter</td>
</tr>
<tr>
<td>Bond head clearance</td>
<td>Largest head size max clear required</td>
<td>Smallest head size min clear required</td>
<td>Large head sue — deep access available</td>
</tr>
<tr>
<td>Sensitivity to contamination</td>
<td>Most sensitive</td>
<td>Less sensitive</td>
<td>Least sensitive</td>
</tr>
<tr>
<td>Purple plague</td>
<td>Most prominent</td>
<td>Increases with reduced hermeticity and increased temperature</td>
<td>Increases with reduced hermeticity and increased temperature</td>
</tr>
</tbody>
</table>

* The information in this table is for general application. Some parameters, i.e., heat, force, may be adjusted for specific applications.
** Each wire requires 2 bonds.
*** Automatic Bonding
APPENDIX A

2.8 Terms and Definitions  The definitions of terms shall be in accordance with IPC-T50 and the following:

Angled Bond  Bond impression of first and second bond are not in a straight line.

Back Bonding  Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of back bonding is face down bonding.

Ball Bond  A bond formed when a ball shaped end of an interconnecting wire is deformed by thermal compression against a metallized pad. The bond may also be designated a nail head bond from the appearance of the flattened ball.

Beam Lead  A long structural member not supported everywhere along its length and subject to the forces of flexure, one end of which is permanently attached to a chip device and the other end intended to be bonded to another material, providing an electrical interconnection or mechanical support or both.
Beam Lead Device  An active or passive chip component possessing beam leads as its primary interconnection and mechanical attachment means to a substrate.

Bond  An interconnection which performs a permanent electrical and/or mechanical function.

Bond Deformation  The change in the form of the bond produced by the bonding tool, causing plastic flow, in making the bond.

Bond Envelope  The range of bonding parameters over which acceptable bonds may be formed.

Bond Interface  The interface between the lead and the material to which it was bonded on the substrate.

Bond Lift-Off  The failure mode whereby the bonded lead separates from the surface to which it was bonded.

Bond Off  See Bond lift off.

Bond Pad  See Bonding area.

Bond Schedule  The values of the bonding machine parameters used when adjusting for bonding. For example, in ultrasonic bonding, the values of the bonding force, time, and ultrasonic power.

Bond Site  The portion of the bonding areas where the actual bonding took place (see Bonding area).

Bond Strength  A measure of force or pressure required to separate a layer of material from its base. This may be measured as peel strength, in pounds per inch of width, or as pull strength, in pounds per square inch, when a perpendicular pull is applied to the surface of the material. In wire bonding, it is the pull force required to rupture the bond interface or wire. Typically measured in gram-force.

Bond-to-Bond Distance  The distance between successive bonds of a given interconnect wire or lead.

Bond Tool  The instrument used to position the lead(s) over the desired bonding area and impart sufficient energy to the lead(s) to form a bond.

Bondability  Those surface characteristics and conditions of cleanliness of a bonding area which must exist in order to provide a capability for successfully bonding an interconnection material by one of several methods, such as ultrasonic, thermosonic, or thermocompression wire bonding.

Bonding, Die  Attaching the semiconductor chip to the substrate, either with an epoxy, eutectic or solder alloy.

Bonding Area  The area, defined by the extent of a metallization land or the top surface of the terminal, to which a lead is or is to be bonded.

Bonding Pad  A metallized area in which a connection is to be made.

Bonding Wire  Find gold or aluminum wire for making electrical connections in hybrid circuits between various bonding pads on the semiconductor device, substrate, or package terminals.

Bulk Conductance  Conductance between two points of a homogeneous material.

Burn-In  The process of electrically stressing a device (usually at an elevated temperature environment) for an adequate period of time to cause failure of marginal devices.

Camber  A term that describes the amount of overall warpage present in a substrate.

Capillary  A hollow bonding tool used to guide the bonding wire during the bonding cycle. Also applies a combination of heat, pressure, mechanical energy, or ultrasonic energy during the bonding cycle (depending upon the bonding process chosen).

Capillary Tool  A tool used in bonding where the wire is fed to the bonding surface of the tool through a bore located along the long axis of the tool.

Ceramic Package  (Sometimes referred to as a "co-fired ceramic package")—a package body made up of tape-cast or pressed aluminum, beryllia, or aluminum nitride "preforms". Conductive patterns are defined on multiple layers in the "green" state. Then layers are stacked and laminated and fired at high temperature to yield a monolithic multilayered structure.

Centerwire Break  The failure mode in a wire pull test where the wire fractures at approximately midspan.

Chip  The uncased and normally leadless form of an electronic component part, either passive or active, discrete or integrated.

Chip-and-Wire  A technology employing face-up-bonded chip devices exclusively, interconnected to the substrate conventionally (i.e., by flying wires). More properly designated as "die and wire".

Chisel  A specially shaped bonding tool in the shape of a chisel used for wedge bonding and ultrasonic bonding of aluminum or gold wires to elements or package leads.

Chopped Bond  Those bonds with excessive deformation such that the strength of the bond is greatly reduced.

Circuit  The interconnection of a number of electrical elements and/or devices, performing a desired electrical function.

Coefficient of Thermal Expansion  The ratio of the change in length per unit length to the change in temperature.

Compliant Bond  A bond which uses an elastically and/or plastically deformable member to impart the required energy to the lead. This member is usually a thin metal foil that is expendable in the process.

Compliant Member  The elastically and/or plastically deformable medium which is used to impart the required energy to the lead(s) when forming a compliant bond.

Conductive Adhesive  An adhesive material that has metal power added to increase electrical conductivity.

Conductive Epoxy  An epoxy material (polymer resin) that has been made conductive by the addition of a metal powder, usually gold or silver.
Conductivity  The ability of a material to conduct electricity; the reciprocal of resistivity.

Controlled Collapse  Controlling the reduction in height of the solder balls in a flip-chip processing operation.

Cratering  Defect in which a portion of an IC chip pad, under a bond, is torn loose by excessive ultrasonic energy or insufficient force.

Creep  The dimensional change with time of a material under load.

Cure Time  The total elapsed time between the addition of a catalyst and the complete hardening of a material; also the time for hardening of premixed, frozen, or refrigerated epoxy adhesives.

Current Carrying Capacity  The maximum current which can be continuously carried by a circuit without causing objectionable degradation of the electrical or mechanical properties.

Cut off  The operation following the final bonding step that separates the bond from the wire magazine.

Die (Plural Dice)  Bare, unprotected Integrated Circuit (IC) chip(s).

Die Bond  Attachment of a die or chip to the substrate.

Dielectric Constant  The term used to describe a material's ability to store charge when used as a capacitor dielectric. It is the ratio for the charge that would be stored with free space as the dielectric to that stored with the material in question as the dielectric.

Dielectric Loss  The power dissipated by a dielectric as the friction of its molecules opposes the molecular motion produced by an alternating electric field.

Direct Contact  A contact made to the semiconductor die when the wire is bonded directly over the part to be electrically connected, as opposed to the expanded contact.

Electroless Plating  Deposit of a metallic material on a surface by chemical deposition as opposed to the use of an electric current.

Electron Beam Bonding  Bonding two conductors by means of heating with a stream of electrons in a vacuum.

Encapsulate  Sealing up or covering an element or circuit for mechanical and environmental protection.

Eutectic  The specific proportions of the constituents of an alloy having the lowest melting point. The system from totally molten to totally solid without going through a slushy range at the eutectic composition.

Eutectic Alloy  An alloy having the same liquidus (melting temperature) as solidus (solidification temperature).

Hermetic Seal  A seal that is gas tight—there is no exchange of internal gases with those outside of the package. By definition, a plastic encapsulated package is not hermetic (measured in atm-cm²/sec.)

Intermetallic Bond  The ohmic contact made when two metal conductors are welded or fused together.

Intermetallic Compound  A compound of two or more metals that has a characteristic crystal structure that may have a certain composition corresponding to a solid solution, often refractory.

Lid  Abbreviation for “leadless inverted device.” A shaped, metalized ceramic form used as an intermediate carrier for semiconductor chip devices, especially adapted for attachment to conductor lands of a thick-or-thin film network by reflow solder bonding.

Metallization  A film pattern (single or multilayer) of conductive material deposited on a substrate to interconnect electronic components, or the metal film on the bonding area of a substrate which becomes a part of the bond and performs both an electrical and a mechanical function.

Microbond  A bond of a small wire, such as 0.025 mm [0.001 inch] diameter gold wire, to a conductor or to a chip device.

MOS Device  Abbreviation for a metal oxide semiconductor device.

MTBF  Abbreviation for mean time between failures. A term used to express the reliability level. The reciprocal of the failure rate.

Nonconductive Epoxy  An epoxy material (polymer resin) either without a filler or with a ceramic or mineral powder filler added for increasing thermal conductivity and improving thixotropic properties. Nonconductive epoxy adhesives are used in chip to substrate bonds where electrical conductivity to the bottom of the chip is unnecessary or in substrate-to-package bonding.

Nuqueat  The region of recrystallized material at a bond interface which usually accompanies the melting of the materials at the interface.

Off Bond  Bond that has some portion of the bond area extending off the bonding pad.

Parallel Gap Soldering  Passing a high current through a high-resistance gap between two electrodes to remelt solder thereby forming an electrical connection.

Parallel Gap Welding  Passing a high current through a high-resistance gap between two electrodes that are applying force to two conductors, thereby heating the two workpieces to the welding temperature and effecting a welded connection.

Passivation  The formation of an insulating layer directly over a circuit or circuit element to protect the surface from contaminants, moisture, or particles.

Peel Strength (Peel Test)  A measure of adhesion between a conductor and the substrate. The test is performed by pulling or peeling the conductor off the substrate and observing the force required. Units are oz/ml or lb/lin. of conductor width.

Pull Strength  The values of the pressure achieved in a test where a pulling stress is applied to determine breaking strength of a lead or bond.
Pulse Soldering  Soldering a connection by melting the solder in the joint area by pulsing current through a high-resistance point applied to the joint area and the solder.

Purple Plague  One of several gold-aluminum compounds formed when bonding gold to aluminum and activated by re-exposure to moisture and high temperature (340°C). Purple plague is purplish in color and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

Push-Off Strength  The amount of force required to dislodge a chip device from its mounting pad by application of force to one side of the device, parallel to the mounting surface.

Reducing Atmosphere  An atmosphere containing a gas such as hydrogen that will reduce the oxidative state of the subject compound.

Reflow Soldering  A method of soldering involving application of solder prior to the actual joining. To solder, the parts are joined and heated, causing the solder to remelt or reflow.

Resistance Welding  The joining of two conductors by heat and pressure with the heat generated by passing a high current through the two mechanically joined materials.

Sagging or Wire Sag  The failure of bonding wire to form the loop defined by the path of the bonding tool (dross) between bonds.

Scrubbing Action  Rubbing a chip device around on a bonding pad during the device attachment operation to break up any oxide layers and improve wetability. Typically part of the solder or eutectic attachment operation.

Search Height  The height of the bonding tool above the bonding area at which final targeting adjustments are made (prior to lowering the tool for bonding).

Second Bond  The second bond of a bond pair made to form a conductive connection.

Second Search  That portion of machine cycle at which final targeting adjustments in the location of the second bond under the tool are made prior to lowering the tool for making the second wire bond. This is analogous to “first search” during the first bond.

Shear Rate  The relative rate of flow or movement (of viscous fluids).

Sputtering  The removal of atoms from a source by energetic ion bombardment, the ions supplied by plasma. Process is used to deposit films for various thin-film applications.

Squashout  The deformed area of a lead which extends beyond the dimensions of the lead prior to bonding.

Stitch Bond  A bond made with a capillary-type bonding tool when the wire is not formed into a ball prior to bonding.

Tail (of the Bond)  The free end of wire extending beyond the bond impression.

Thermal Mismatch  Differences of thermal coefficients of expansion of materials which are bonded together.

Thermocompression Bonding  A process involving the use of pressure and temperature (substrate temperature 450°C, terminal 1300°C) to join two materials by interdiffusion across the boundary.

Thermosonic Bonding (TS Bonding)  A wire bonding process using both thermocompression and ultrasonic energy to join two materials by interdiffusion across the interface boundary (substrate temperature 150°C).

Ultrasonic Bonding  A process involving the use of ultrasonic energy and pressure to join two materials.

Ultrasonic Cleaning  A method of cleaning that uses cavitation in fluids caused by applying ultrasonic vibrations to the fluid.

Vacuum Deposition  Deposition of a metal film onto a substrate in a vacuum by metal evaporation techniques.

Vacuum Pickup  A handling instrument with a small vacuum cup on one end used to pick up chip devices.

Viscosity  A term used to describe the fluidity of material, or the rate of flow versus pressure. A unit of viscosity is Poise (P) (centipoise = 1/100 poise, cp = 1000 centipoise). Other units of viscosity are Pascal-second (Pa·s) and Stokes (St).

Wafer  A slice of semiconductor crystal ingot used as a substrate for transistors, diodes, and monolithic integrated circuits.

Warpage  The distortion of a substrate from a flat plane.

Wedge Bond  The second bond of a thermocompression or thermosonic bonding process. This can also be the first or second bond of the ultrasonic bonding process.

Wire Bonding  The method used to attach very fine wire to semiconductor components to interconnect these components with each other or with package leads.

3.0 Design of COB Structures  The design of COB structures starts with the decision to use direct chip attachment and interconnection to the packaging and interconnecting (P&I) structure. That decision is based on the advantages and disadvantages of the COB assembly technique as outlined in section 1.2 of this document.

The advantages include:
- Lower cost (in high volume),
- Lighter weight,
- Smaller packages,
- Lower "Z" dimension profile (thinner packages),
- Shorter circuit paths (faster switching speed),
- Improved impedance control,
- Reduced number of interconnection levels in the overall system (fewer solder joints), and
- Shorter turn-around time for prototypes and production.