ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

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Number	
2.6.25	
Subject	
Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis	
Date	Revision
11/03	
Originating Task Group	
Electrochemical Migration Task Group (5-32e)	

IPC-TM-650
TEST METHODS MANUAL

1 Scope

This test method provides a means to assess the propensity for conductive anodic filament (CAF) growth, a form of electrochemical migration within a printed wiring board (PWB). Conductive anodic filaments may be composed of conductive salts, rather than cationic metal ions, however inadequate dielectric for the applied voltage, component failures, and part use exceeding the maximum operating temperature (MOT) of the laminate can contribute to product failures as well. This test method can be used to assess PWB laminate materials, PWB design and application parameters, PWB manufacturing process changes and press-fit connector applications.

2 Applicable Documents

2.1 IPC

IPC-A-47 Composite Test Pattern Ten-Layer Phototool

IPC-2221 Generic Standard On Printed Board Design

IPC-9253 CAF Test Board (Available in the 'Drafts' section of the 5-32e Committee Home Page)

IPC-9254 CAF Test Board (Available in the 'Drafts' section of the 5-32e Committee Home Page)

IPC/EIA J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-004 Requirements for Soldering Fluxes

IPC/EIA J-STD-006, Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.2 American Society for Testing and Materials (ASTM)

ASTM D-257 Standard Test Methods for DC Resistance or Conductance of Insulating Materials

3 Test Specimens

(Recommended that the latest version of the CAF test board be used)

3.1 IPC-9253 and IPC-9254 The IPC-9253 and IPC-9254 have 10 layers and dimensions are approximately 125x175 mm [nominally 5x7 in]. Test board designs for evaluating CAF resistance shall have varying drilled hole wall to drilled hole wall distances for plated holes. These distances can range from as low as 0.15 mm [0.00591 in] separation for alternate laminate materials expected to have very high CAF resistance and minimal copper wicking out from the plated-through hole (PTH), to as high as 0.89 mm [0.0350 in] separation for evaluating press-fit connector applications. The drilled hole size, rather than the finished hole size, is specified in the chart on the bare board fabrication drawing to ensure consistent spacing. Internal layer thieving may be added to plane layers around the perimeter. Test boards should be manufactured so that the machine/grain direction of the woven fiber reinforcement is perpendicular to the rows of same-net daisy chain vias for A1-A4 (machine/grain direction tends to fail first). Test board designs shall have sufficient minimum spacings on outer layers to ensure that surface insulation resistance failures do not occur. Layouts of the IPC-9253 and IPC-9254 test board structures (CAF Test Boards) are shown below (Figure 1).

IPC-9253 and IPC-9254 Test Structures A1 through A4

The four structures A1-A4 each have five rows of connected vias. Within each structure each row has 42 vias with alternating rows being tied to positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 1 mm [0.040 in] pitch between rows of daisy chain vias. The resulting via edge to via edge spacings are: 0.27 mm, 0.38 mm, 0.51 mm, 0.65 mm [0.0106 in, 0.0150 in, 0.0201in, 0.0256 in]. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in these four test structures A1-A4 are aligned with the glass fibers. Since A1-A4 evaluate susceptibility to CAF in just one direction, test coupons should be manufactured so that the machine direction of the woven fiber laminate reinforcement is perpendicular to the rows of same-net daisy chain vias (machine direction tends to fail first).

For both A and B test structures the inner and outer layer pads are the same, i.e., the same pad size is consistently used within a given test structure, although it does change from structure to structure. All via to electrode connections are made on layer 2 and are repeated on layer 9 so that a single etch-out will not affect results. Traces from via to electrode are routed on internal layers rather than external layers to minimize potential for surface insulation resistance failure.

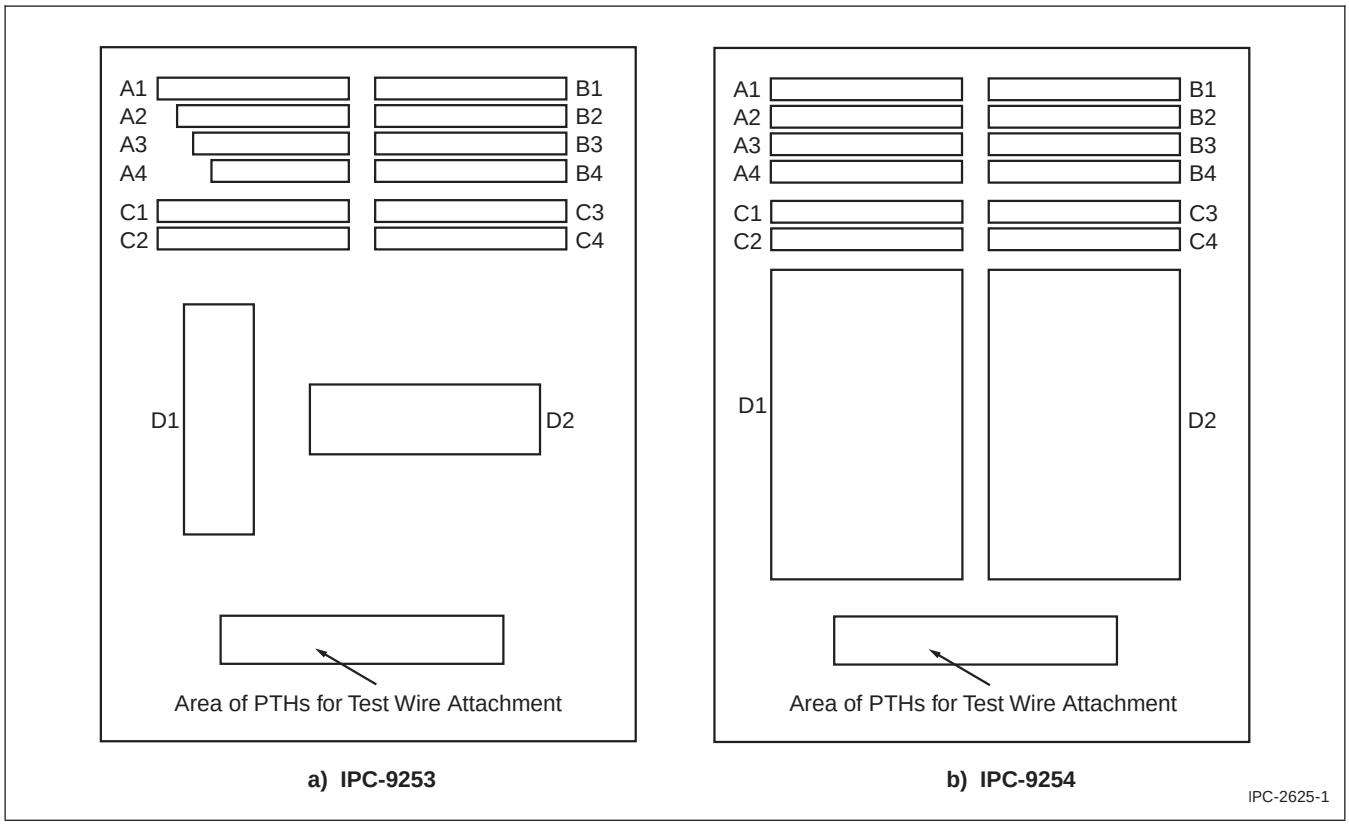

Figure 1 Layouts of the Two Versions of the CAF Test Boards

Design details for each test structure A1-A4 follows in Table 1. Note: ''Manhattan Distance'' is the shortest orthogonal distance along the X- and/or Y- axes lines between adjacent drilled hole features (corresponds to the orthogonal nature of the laminate material's woven glass fiber reinforcement (Figure 2).

IPC-9253 and IPC-9254 Test Structures B1 through B4

The four ''B'' test structures have seven alternating rows of vias. Within each structure, alternating rows have either 27 or 26 vias with the alternating rows being tied to either positive or negative electrodes. The via edge to via edge spacing is

Table 1 Test Structures A1 through A4 Design Rules

	A1	A2	A3	A4
Outer layer pad size	0.86 mm [0.0339 in]	0.81 mm [0.0319 in]	0.75 mm [0.0295 in]	0.69 mm [0.0272 in]
Inner layer pad size	0.86 mm [0.0339 in]	0.81 mm [0.0319 in]	0.75 mm [0.0295 in]	0.69 mm [0.0272 in]
Drilled hole size	0.74 mm [0.0291 in]	0.63 mm [0.0248 in]	0.51 mm [0.0201 in]	0.37 mm [0.0146 in]
Via edge to via edge (shortest distance)	0.27 mm [0.0106 in]	0.38 mm [0.0150 in]	0.51 mm [0.0201 in]	0.65 mm [0.0256 in]
Via edge to via edge (Manhattan Distance)	0.27 mm [0.0106 in]	0.38 mm [0.0150 in]	0.51 mm [0.0201 in]	0.65 mm [0.0256 in]
On IPC-9254 **only**, bias applied between:	J1, J5	J2, J5	J3, J5	J4, J5

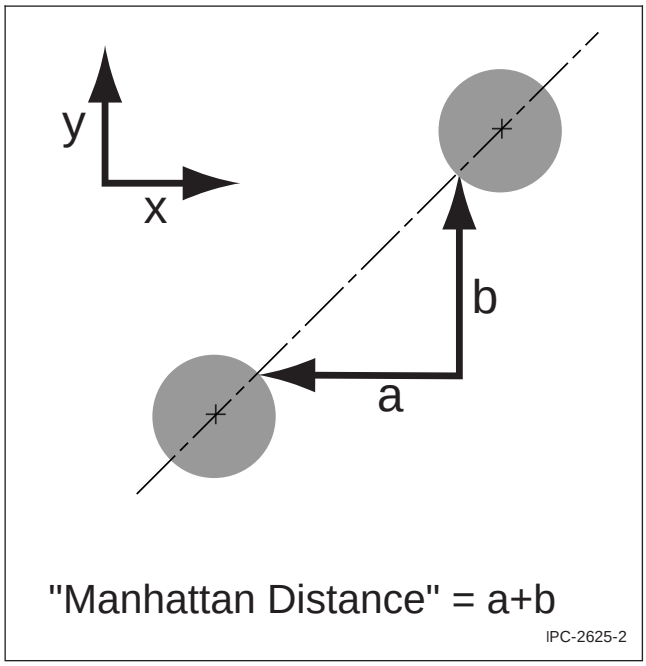

Figure 2 Manhattan Distance (Shortest Orthogonal)

varied from one structure to the next by using a different drilled hole size on the same 1.52 mm x 1.52 mm [0.05984 in x 0.05984 in] via grid. The 1.52 mm x 1.52 mm [0.05984 in x 0.05984 in] grid has an interstitial via therefore, tipping at a 45° angle results in a square 1.08 mm x 1.08 mm [0.04252 in x 0.04252 in] grid. Note: the sketches do not look square when tipped 45° but, the CAF Test Boards do. The resulting via edge to via edge spacings are: 0.26 mm, 0.37 mm, 0.51 mm, 0.62 mm [0.0102 in, 0.0146 in, 0.0201 in, 0.0244 in]. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the ''B'' test structure are not aligned with the glass fibers. If the failure mode is along glass bundles it is reasonable to expect the ''B'' test structure to perform better than the ''A'' structure for equivalent via edge to via edge spacings. Within a given test structure, the inner and outer layer pads for all 10 layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change from structure to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etch-out will not affect results.

A conceptual representation of the ''B'' test structure is shown to the upper right (Figure 3). Design details on each of the four ''B'' test structures follows in Table 2.

3.2 Other Structures Section C is designed to evaluate plated-through hole (PTH)-to-plane layer spacings. It is recommended to use the registration coupon F from either test artwork IPC-A-47 or IPC-2221 when CAF testing includes this region. Section D in the IPC-9254 design is for layer-to-layer Z-axis CAF testing. Section D in the IPC-9253 is for evaluating CAF resistance in a press-fit compliant pin connector application. The feature in the D region is an optional feature that is present automatically with the design. However, the A, B and C regions shall remain as designed in order to provide a standard basis of comparison.

The CAF test board with 10 layers is designated to evaluate thin single-ply constructions typically used on high performance boards. This board construction stackup can be reduced down to: (a) four layers by eliminating layers 3 through 8 and (b) only test structures A and B, when just evaluating differences between laminate materials.

3.3 CAF Test Board Design This 10-layer CAF test board for evaluating the insulation resistance between internal conductors within a printed wiring board has the following key features for evaluating hole-hole CAF resistance (Figure 3).

Table 2 Test Structures B1 through B4 Design Rules

	B1	B2	B3	B4
Outer layer pad size	0.94 mm [0.0370 in]	0.89 mm [0.0350 in]	0.84 mm [0.0330 in]	0.75 mm [0.0300 in]
Inner layer pad size	0.94 mm [0.0370 in]	0.89 mm [0.0350 in]	0.84 mm [0.0331 in]	0.75 mm [0.0295 in]
Drilled hole size	0.81 mm [0.0319 in]	0.71 mm [0.0280 in]	0.57 mm [0.0224 in]	0.46 mm [0.0181 in]
Via edge to via edge (shortest distance)	0.26 mm [0.0102 in]	0.37 mm [0.0146 in]	0.51 mm [0.0201 in]	0.62 mm [0.0244 in]
Via edge to via edge (Manhattan Distance)	0.37 mm [0.0146 in]	0.52 mm [0.0205 in]	0.72 mm [0.0283 in]	0.88 mm [0.0346 in]
On IPC-9254 **only**, bias applied between:	J7, J11	J8, J11	J9, J11	J10, J11

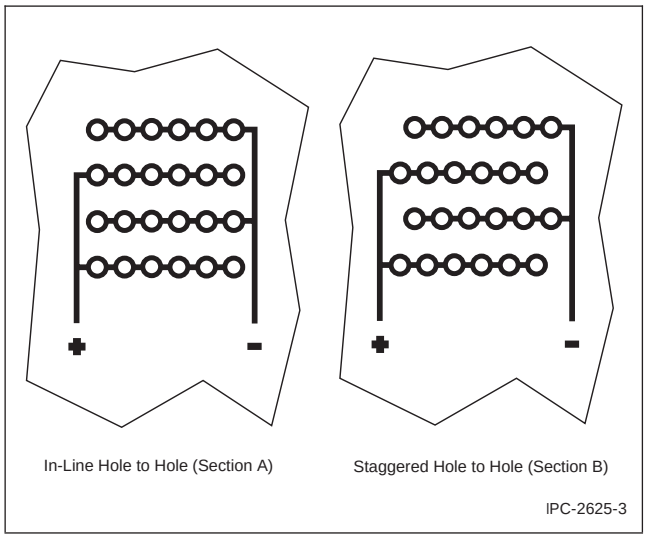

Figure 3 CAF Test Board PTH-PTH Spacing Design

Holes In-Line (in-line with glass fiber direction): There are two rows of 42 signal-1 vias intermeshed with three rows of 42 signal-2 vias; for a total of 168 potential in-line PTH-PTH failures for each spacing distance.

Holes Staggered (closest PTH-PTH spacing in diagonal direction): There are three rows of 26 signal-1 vias intermeshed with four rows of 27 signal-2 vias; for a total of 312 potential diagonal PTH-PTH failures for each spacing distance.

3.4 CAF Test Coupon/Board Quantity The CAF testing data analysis technique recommended for either of these CAF test coupon/board designs requires a minimum 25 CAF test boards to be run per sample lot per bias level for statistical significance. This provides a total of 4,200 potential in-line hole-hole CAF failure sites and 7,800 potential diagonal hole-hole CAF failure sites for each unique sample/condition set.

For comparison, on a 1,428 I/O BGA device (Figure 4) there are about 500 power/ground pins. So with an average of slightly less than two adjacent power/ground pin spacings per pin there are about 1,000 potential in-line hole-hole CAF failure sites per BGA device. For a production board with the equivalent of three of these BGA devices and about 1200 passives or other components with close power/ground pin spacings, the total number of opportunities for in-line CAF failure would then be about 4,200 (about the same as the entire CAF test board sample lot of 25 pieces).

As a general rule, there should be enough CAF test boards run within each sample test lot to have at least the equivalent

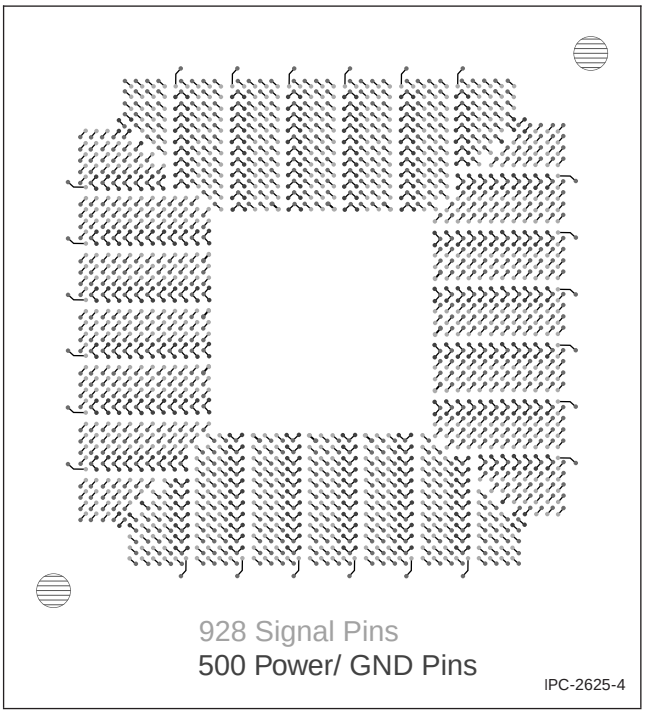

Figure 4 BGA Device I/O Pin Assignment

number of potential CAF failure sites as on a single targeted specific application PWB.

4 Equipment/Apparatus or Material

4.1 Environmental Test Chamber A clean test chamber capable of producing and recording an environment of 65 ± 2 °C [149 ± 3.6 °F] or 85 ± 2 °C [185 ± 3.6 °F] and 87 +3/-2% relative humidity, and that is equipped with cable access to facilitate measurement cables to be attached to the specimens under test.

4.2 Measuring Equipment A high resistance meter equivalent to that described in ASTM D-257, with a range up to 10^{12} ohms and capable of yielding an accuracy of ± 5% at 10^{10} ohms with an applied voltage of 100 ± 2 VDC, or an ammeter capable of reading 10^{-10} amps and capable of yielding an accuracy of ± 5% in combination with 100 ± 2 VDC power supply. The values of resistors used shall be verified by reference resistors traceable to known industry or national standards such as NIST.

4.3 Power Supply A power supply capable of producing a standing bias potential of 10 VDC up to 100 VDC with a

tolerance of ± 2 VDC, and current supply capacity of at least 1 Ampere (Amp).

4.4 Current Limiting Resistors Tight control of the total current limiting resistance value is critical for this test method. One 10^6 ohm resistor in series shall be used for each current path. Insert the current limiting resistors in series with the terminating leads going to each test pattern. Note that some test equipment has current limiting resistors built into the testing systems. For the purposes of this standard test, excluding the current limiting resistor and for each CAF test circuit, the total series resistance of the measuring equipment and wires shall not be more than 200 ohms. A lower total resistance value will increase potential for damage to the test board when a CAF failure occurs. A higher total current limiting resistance value for each test net removes test conditions further from actual field conditions and is not recommended.

4.5 Connecting Wire Use PTFE- or PFE-insulated copper wires and solder the copper wire directly to the board to connect test points for each test board to the measurement apparatus.

4.6 Other Dedicated Fixtures Hard-wiring is the default connection method. Other dedicated fixtures may be used, provided that the fixture does not change the resistance by more than 0.1 decade compared to a comparable hard-wired system when measured at the test conditions. These fixtures should be checked for their resistance values frequently.

5 Procedure

5.1 Test Specimen Preparation

5.1.1 Sample Identification Use a method for identifying each test board that does not cause contamination, such as a scribe, making marks away from the biased area(s) of the specimen. Test boards shall be handled by the edges of the board only, and the use of noncontaminating gloves is recommended.

5.1.2 Prescreen for Opens and Shorts Perform as-received insulation resistance measurements using a multimeter to make connection to each net, and check for gross defects. Check for shorts at a 1.0 megohm setting. No opens are allowed in connected nets.

5.1.3 Cleaning Entirely clean each sample (CAF test board) per IPC Test Method 2.3.25 (Resistivity of Solvent Extract) by immersion washing until the level of ionic contamination is reduced to less than 1.0 microgram NaCl equivalent per square centimeter and for a maximum of 20 minutes. Boards not achieving this level of cleanliness within 20 minutes shall be scrapped for the purposes of this test.

5.1.4 Connecting Wire Plated-through holes near one edge of the board may be used for connecting wire to each test circuit. Cover the test board with noncontaminating film to prevent flux spattering during the wire attach process. After stripping back the wire insulation, use water white rosin (per J-STD-004, Type B) and best soldering technique (per J-STD-001, Class 1 or 2) to solder (per J-STD-006, Type Sn63) PTFE- or PFE-insulated wires to the connection points on each test board. Ensure against damaging PWB laminate material adjacent to the plated holes during soldering by using appropriate time/temperature parameters for the soldering iron.

5.1.5 Cleaning After Attachment Perform appropriate local cleaning and rinsing after the attachment of the connecting wires. Isolation resistance between connecting wire attachment sites should remain excellent through 96 hours conditioning. Note: Each CAF test failure that does occur during subsequent testing should be checked to determine whether the connecting wire attach area is the low resistance site. If the connecting wire attach area rather than the daisy chain area is the low insulation resistance site, then that test sample is no longer valid for data analysis.

5.1.6 Dry Bake sample boards for six hours in a clean oven at 105 ± 2 °C [221.0 ± 3.6 °F].

5.1.7 Precondition Precondition test board samples in a bias-free state (no electrical potential applied to any test pattern) for 24 hours minimum at 23 ± 2 °C [73.4 ± 3.6 °F] and 50 ± 5% relative humidity prior to any initial insulation resistance measurements [measuring insulation resistance of each daisy-chain net on each test board before starting the first 96 hours (± 30 minutes) of bias-free temperature and humidity conditioning].

5.1.8 Temperature/Humidity/Bias (T/H/B) Chamber Place the specimens in the environmental test chamber in a vertical position such that the air flow is parallel to the direction of all test boards in the chamber. Allow at least approximately 2.5 cm [nominally 1.0 in] between each test board. Place the test boards, as much as possible, toward the center of the chamber to help ensure against nonoptimum air flow and/or drops

of condensation falling onto the test boards. Dress all wiring away from the test patterns, keeping the wires away from the test patterns as they are routed to the outside of the chamber. Also, wire should not impede airflow around the samples. Set the chamber temperature and humidity with a ramp rate of one hour.

5.2 Test Procedures

5.2.1 Environmental Test Chamber Controls Tight control of the test humidity is critical for this test method. A difference of 5% relative humidity can result in a 0.5 to 1.0 decade difference in measured resistance. If condensation occurs on the test specimens within the environmental chamber while the samples are under voltage, other dendritic growth can occur. Water spotting may also be observed in some ovens where the air flow in the chamber is from back to front, when water condensation on a cooler oven window can be blown around the oven as very small droplets that deposit on test specimens. This contributes to dendritic growth. These conditions should be eliminated to ensure meaningful test results. Although the environmental test chamber should be capable of producing and recording an environment of 65 ± 2 °C [149 ± 3.6 °F] or 85 ± 2 °C [185 ± 3.6 °F] with 87 +3/-2% relative humidity. A range of ± 5% relative humidity may be permitted for short periods, not to exceed five minutes.

5.2.2 Resistance Measurements Measure the insulation resistance of each test board daisy-chain net using 50 VDC per second rate of rise and minimum hold time of 60 seconds at 100 VDC test voltage. The polarity of the bias (conditioning) voltage and the polarity of the test (measurement) voltage must always be the same. 100 VDC applied voltage is used as the test voltage for insulation resistance measurements.

5.2.3 After initial insulation resistance measurements are taken, close the environmental test chamber and allow the test boards to stabilize for 96 hours (± 30 minutes) at the specified 65 ± 2 °C [149 ± 3.6 °F] or 85 ± 2 °C [185 ± 3.6 °F] with 87 +3/-2% relative humidity and no bias applied. After the 96 hour (± 30 minutes) stabilization period, insulation resistance measurements shall be made between each daisy-chain net and ground.

5.2.4 Ensure that all test board samples are connected and that the appropriate current limiting resistor is in series with each corresponding test circuit. Then, connect the test boards to the power supply to begin the T/H/B portion of the CAF testing.

5.2.5 Verify that the appropriate voltage bias is being applied for the duration of the test. For comparing the CAF resistance of different laminate materials and processes, use the CAF test standard of 100 VDC bias condition. For correlating test results to expected life in the field, the second bias voltage condition selected should be two times the maximum operating voltage differential for a given application. While a lower voltage may not discriminate between more CAF-resistant materials and processes, a higher voltage, which almost linearly affects time to failure, should also be avoided. This is because a higher voltage may offset the impact of humidity, a key part of the failure mechanism, due to localized heating.

5.2.6 The bias polarity should always be the same as the polarity used when measuring the insulation resistance after the 96-hour stabilization period.

5.2.7 It is recommended that additional resistance monitoring measurements be taken every 24 to 100 hours of bias (conditioning) voltage during the duration of the test, ensuring that the polarity of the insulation measurement voltage and the bias voltage are always the same. Decade drops in resistance, observed when these intermediate measurements are taken, also count as failures and improve the accuracy of the test since CAF filaments are very thin and are easily destroyed. Also when over 50% of the parts have failed, the test can be stopped. As CAF forms, the voltage delivered across the CAF failure site will drop as the resistance decreases. This becomes significant as the resistance of the net approaches the resistance of the current-limiting resistor, so adjustments to the voltage during the test are not required.

5.2.8 After 500 hours of applied bias (596 hours total), perform the insulation resistance measurements, as before.

5.2.9 Additional temperature/humidity/bias conditioning may be performed after 500 hours of bias, sometimes up to 1000 hours or more. However, the 500 hours bias testing results shall provide a minimum standard for reporting CAF testing results when using this procedure.

5.2.10 Suspect CAF test failures may be checked to determine whether the connecting wire attach area is the low resistance site rather than the daisy-chain area. This requires cutting the trace near the daisy chain (destructive). After all testing is completed, if the connecting wire attach area rather

than the daisy chain area is then found to be the low insulation resistance site, then that test sample is no longer valid for data analysis.

5.3 Data Handling and Analysis

5.3.1 Lognormal plots are recommended for plotting percent of samples above an insulation resistance value, versus insulation resistance. Use the log value of the insulation resistance.

5.3.2 If lognormal plots are not used, a test circuit failure shall be determined by more than a decade drop in insulation resistance as a result of the applied bias. The baseline for the decade drop shall be the average insulation resistance at 96 hours for each coupon (A-1, A-2, etc.).

5.3.3 Test board nets with less than 10 megohms insulation resistance (high resistance short) after the 96-hour stabilization shall be excluded, since these failures are due to poor PTH hole quality or laminate capability.

5.3.4 The insulation resistance baseline (before bias conditioning) value for a given daisy-chain net (same design spacing) shall be the average resistance of those un-shorted daisy-chain nets on all test boards in the valid sample group as measured after the 96-hours stabilization period.

5.3.5 The percent failure rate for a given sample group and subsequent test condition is the percent of test boards that show more than a decade drop in resistance compared with the baseline value for daisy-chain nets with the same design spacing.

5.3.6 For a given sample lot, there may be binomial failure distributions where assignable causes exist along with different levels of capability.

5.4 Visual Examination After completion of the test, the test boards shall be removed from the environmental chamber and examined at 10X magnification for evidence of surface insulation resistance failure (i.e., discoloration, corrosion), handling or processing defects other than CAF.

5.4.1 Assignable Cause Where an assignable cause of low insulation resistance can be properly attributed to a handling or processing defect other than CAF (i.e., contamination on the insulating surface of the board, scratches, cracks, or other obvious damage affecting the insulation resistance between the conductors), then such a value should be excluded.

5.4.2 CAF Microsections Since CAF filaments form along the interface between resin and the woven reinforcement, these filaments can be very small and easily disrupted by a relatively low current flow or other causes. Microsectioning to observe CAF filaments can be a tedious process with a low success rate.

5.5 Reporting Results

5.5.1 The percent failure rate at 500 hours for each spacing in sections A and B are the results of interest. Generally PWB processing has the greatest impact on reduced CAF resistance at smaller plated-through hole-to-plated-through hole (PTH-PTH) spacings, while the laminate material has the greatest impact at larger PTH-PTH spacings. However, the laminate material used can also affect the extent of fracturing and copper wicking near a PTH.

5.5.2 There are several additional factors that can affect CAF resistance. See APPENDIX A for the list of PCB manufacturing parameters that may affect CAF resistance and that should be documented.

6 Notes

6.1 Definitions [Only those terms not already included in IPC-T-50.]

a) ***Conductive Anodic Filament (CAF) Formation:***

The growth of metallic conductive salt filaments by means of an electrochemical migration process involving the transport of conductive chemistries across a nonmetallic substrate under the influence of an applied electric field, thus producing Conductive Anodic Filaments.

b) ***Electrochemical Migration (ECM):***

The growth of conductive metal filaments across or through a dielectric material in the presence of moisture and under the influence of voltage bias.

c) ***Electroless Nickel / Immersion Gold (ENIG):***

This is a multi-functional surface finish wherein the electroless nickel layer is capped with a thin layer of immersion gold. It is applicable to soldering, aluminum wire bonding, press fit connections and as a contact surface. The immersion gold protects the underlying nickel from oxidation/ passivation over its intended life.

d) ***Maximum Operating Temperature (MOT):***

An underwriters Laboratories Inc. (UL) requirement value of laminate materials as determined by the results of tests performed by UL.

e) ***Organic Solderability Preservative (OSP):***

A surface finish for fine pitch featured PCBs that are often assembled using surface mount components (SMCs). The OSP surface finish provides very flat/co-planar land areas for the placement and attachment of SMC devices.

f) ***Printed Circuit Board Fabrication (PCB Fab):***

This phrase alludes to the manufacturing of a bare printed circuit board that is not populated (assembled) with any discrete components.

6.2 Reference Documents

IPC-TR-476 Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies

IPC-TM-650, Method 2.6.14.1 Electrochemical Migration Resistance Test (note: covers only surface electrochemical migration)

IPC-9201 Surface Insulation Resistance Handbook

APPENDIX A

Additional CAF Resistance Factors Checklist

Document for every CAF resistance test the several additional factors that can affect CAF resistance. These critical factors include:

Needed Parameters	Comments
Test board revision level used.	
Drilled Hole Size for each Hole-Hole and Hole-Plane spacing tested (also recommend drilling feed rate, speed of rotation, chip loading data, backup material type, etc.).	
Type of desmear (permanganate, plasma, or ?).	
Whether glass microetch was used (and if so, the controlling process parameters).	
Board finish type (HASL or specific OSP, immersion silver, immersion tin, ENIG, etc.).	
Laminate material type that was used (manufacturer and material name or number).	
Type of soldermask (if used).	
PCB Fab manufacturer and facility.	
Method of separating test board from working panel.	
Number of circuit layers in test board.	
Copper thickness in plated through holes in test board.	