SURFACE MOUNT COUNCIL WHITE PAPER

Design for Success
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DESIGN FOR SUCCESS WHITE PAPER

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The Surface Mount Council (SMC) is made up of key industry representatives from EIA, IPC and SMTA. The SMC is dedicated to promoting the use of surface mount and advanced electronic packaging technology in the design and production of electronic hardware.

Council Members represent user, supplier and equipment manufacturing companies engaged in surface mount implementation for automotive, telecommunication, computer, instrument, government, consumer and medical electronics.

The mission of this Council is to facilitate, coordinate and promote the orderly implementation of surface mount technology through standardization, the development of technical documents and other means.

This Technical Report is a compilation of six papers. The focus is to establish the design for excellence parameters for designing and fabricating electronic assemblies. The presentations were commissioned by the SMC and prepared by the industry experts indicated under the title of each presentation.

The papers were presented as a part of the Surface Mount International proceedings. They have been extracted to provide the reader with a compendium of the major conclusions that should be observed in order to follow Design for Excellence Principles.

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Arlington, VA 22201-3834

IPC
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These papers were originally presented at Surface Mount International 1996 in San Jose.
ABSTRACT
This paper addresses the complete process of reengineering New Product Development Processes to incorporate DFX methodologies. The companion papers address specific aspects of DFX such as Fabrication, Assembly, Test, Reliability and the Environment. Issues like Serviceability, Repairability, ESD protection, etc. are not discussed but are equally important. The paper presents the case for a comprehensive analysis of the key business issues and definition of requirements before initiating work to refine or restructure processes. The specific tools, methodologies, and practices of DFX are often the easier elements to address and implement. Short and long term success requires a base of robust business and management processes. The paper addresses the importance of assessing the global competitive situation and defining the specific requirements for success of the individual organization. Comprehensive corporate and functional strategies, roles of individuals and functions, specific criteria of success, and other requirements are discussed. The need for effective and stable leadership, business focus and management is presented. Tools and methodologies required to meet the "Design for" criteria are presented as elements to consider in refining or redesigning new product development processes.

INTRODUCTION
The fundamental measures of success for any business are economic. The Electronics Industry has provided rapid improvements in technologies and capabilities that have provided enormous benefits. Global markets have responded with major increases in demand for all types of products. The demand provides the profits and capital required to support the tremendous growth. The future also contains major growth potential in many new areas. The computer, communications, consumer electronics, and information markets are currently creating major demand. There are other markets, such as autos, that may have even more growth opportunities.

Successful electronics companies will benefit with increased orders for products and services. Those companies that can rapidly define and develop excellent products will enjoy "premium" margins. They will enhance their profits until the competition responds with competitive products that force the market prices down into cost based pricing. Companies must continually innovate and create exciting new products to be successful.

A key element for success is the ability for a company to quickly respond with very competitive, high quality, and low cost products. Although the electronics industry is one of the most flexible and responsive industries, consumer demand will probably increase the pressure for even faster responsiveness for new products during the next decade.

THE CHALLENGE AND OPPORTUNITY
This enormous opportunity presents some staggering numbers described by the projected volumes of chips. The American Electronics Association projects the World Total Electronics Market to grow at ten to eleven percent annually [1]. This was projected to be $940 Billion for 1996. VLSI Research was quoted by the Associated Press to estimate that forty to fifty of the nine hundred IC fabs in the world should be replaced each year. Currently fewer than twenty are being replaced each year. Major capital investments are being made in fabs to meet the demand. There was an estimated $18 billion spent for 1994.

This discussion of the macro market is presented to illustrate the market for electronic products is very, very large and growing at a rapid rate. It is to emphasize that increased
competition will increase pressure and profit margin demands upon all manufacturers. It is a market that will have major opportunities for companies that have effective new product development processes. It will strongly favor companies that have well-designed processes to apply Concurrent Engineering, DFX tools, Concurrent Manufacturing, Predictive Engineering, robust data bases and effective processes to rapidly introduce innovative high quality products.

The trend for the world electronics market could well be similar to leaders of the fashion garment industry. In this marketplace, ideas for a new product can be created on Monday. On Tuesday, the garment is designed, documented in a computer file and transmitted to multiple manufacturing sites around the world. It can be manufactured and distributed to multiple international locations by Saturday. This characterizes a mature industry that has developed a very responsive approach to consumer demands.

The computer, consumer electronic and telecommunications industry have many similarities to the fashion clothing industry. For example, there are many styles or configurations in the personal computer market for monitors, keyboards, disk drives, monitors, power supplies, main boards, etc. A quick glance at the advertisements in your Sunday newspaper illustrates the quickly changing configurations of computers, telephones, etc. These quickly and ever changing customer wants further support the need for flexibility and short time-to-market for new product development and manufacturing in the electronics marketplace.

EVERYONE WILL BE REQUIRED TO CHANGE

Competition in all markets is significantly increasing. The reductions in international barriers and free flow of business will create even more competition from sources that have definite advantages in their cost structures. Companies that are having difficulties with cost, time-to-market or other issues of their new product development process must change the processes that are developing those products.

This corporate issue quickly becomes a personal issue for people in organizations that refuse to change and improve. Consistently producing noncompetitive products, lost market share and low profits have affected too many people in our industry. The reality is that it only requires one person to have the motivation and take the leadership for creating positive change. One person or a few people can lead the change the behavior and capabilities of even the largest company. It can be done before the situation becomes terminal.

An old saying can be paraphrased to, "You will continue to get what you are now getting unless you change the processes you are using." It is very simple. Some gains and improvements can be gained by working harder but the only real answer is to change the processes or ways the work is executed. Development processes, like all natural processes, have a certain defect rate and the process must be addressed, analyzed, and designed to minimize defects, insure positive results, and produce world class products without special attention, screening, or rework.

Change requires someone to lead the change. Managers and other key individuals in the product development process must take responsibility for creating the most effective product development processes for their particular organization. Managers own the responsibility to provide the leadership, direction and commitment to change the processes. There are some examples where individual engineers and other professionals have successfully changed the processes without management support but that should be the last resort. The actual process requires very few days of dedicated work. It is probably the most important and rewarding work that can be done within a company.

Successful products generate the revenue that fuels the company engines. Marketing, Sales, R&D, Manufacturing and all other functions require parts of this revenue to operate and develop even more products. Developing products that generate this revenue is the most important task within a company. All other activities support this process or provide direct customer support.

Change is required of everyone. The companies leading in product development must change and incorporate improvements because today’s processes cannot insure future success. There are ways to smoothly incorporate new ideas, improvements, and best practices into the existing processes to remain leaders.

Companies that are in the middle of the pack need to change to prevent falling further behind. The companies that are truly behind must address changing their processes today for survival. It is not difficult to do but requires leadership, commitment, and the will to make things happen. Again, a very small group of people can cause tremendous improvements to occur.

COMPETITION DRIVES THE NEEDS FOR BETTER PROCESSES

The concepts of Design for Manufacturability, Assembly, Test or DFX have been available for many years. These concepts have always been important but not everyone has given them the same attention. Why is this any different now than in past years? It is because traditional techniques and "throw it over the wall" organizations will simply not survive in the competitiveness of the future marketplace. The competition in the market will force every company or operating unit to become competitive or they will simply cease to exist. People that don’t get the message or refuse to
take action will experience tough competition in the marketplace from those people that take the initiative to act now. Reorganizations, consolidations, and down sizing are largely the result of weak and ineffective new product development processes. Many companies suffer from long periods of flat revenue and struggle for survival because of ineffective product development processes.

An open and competitive market can be very rewarding or it can be very cruel. There are many companies that seem to consistently develop winning products. However, everyone has seen companies that could not or refused to develop the capabilities to develop the processes to quickly and effectively develop new products and be competitive. Unfortunately, good intentions, management rhetoric or wishing success are of no value in the marketplace. It is also true that size is no guarantee of success. Some of the most incredible examples of organizational ineptitude exist in the largest of companies. Sometimes, the larger companies are easy targets for aggressive companies. Larger companies often have created the markets but cannot compete in the execution of competitive new products to maintain their lead.

Rapidly developing the most competitive new products is truly where small companies can take business from large companies. Many examples exist in the electronics industry where larger companies have been removed from the marketplace by smaller, well focused, well managed, and well coordinated teams of people. This is particularly possible in the electronics industry because of the abundance of excellent subcontractors, standard components and materials, good suppliers, and adequate capital.

THE ROBUST IC DEVELOPMENT PROCES S
The message is that "every" company must focus on the processes to develop very competitive new products in the shortest possible time. One element of the electronics industry that addresses the total integrated development and manufacturing processes required for success and survival is the IC industry. The processes to design, manufacture, package and test integrated circuits have all the needed elements required to develop competitive products. A critical aspect is the capability to accurately characterize the processes and predict results before the actual detailed design begins. The Integrated Circuit DFX rules are general enough to apply to nearly every product development project. They are well documented, easily understood and available to everyone to apply to new product design and development projects. These rules are easily applied and insure that substantially more competitive products are developed.

Predictive models exist to provide complete performance, yield and cost data for alternative product specifications. This completely integrated capability is available to the designers of a new chip as they are considering alternatives of design architecture. A very key element is that the models available to the product managers, management, designers and other members of the development team can very accurately predict all the critical performance and cost parameters before the product is designed. These capabilities are not options for the IC industry. They have been developed because of the economic parameters required to make a profit, survive and be successful. The IC industry has incredible capital requirements, enormous volumes, tremendous leverage based upon process yields, and very highly refined technologies and processes. Very slight inefficiencies can quickly become life threatening and must be recognized and designed out of the processes at the very beginning.

This is the ultimate "Design for Every Important Consideration" or DFX process. Every issue that is important for IC design, development, manufacturing, packaging, and test is embedded into the models. The model accurately represents the process capabilities and the resulting costs for every step in the process. The financial models both require and reward investments to achieve this capabilities. It is a highly evolved process and a necessary element of any successful IC business.

The driving factors that require the "up-front total capability" for the IC industry do not generally exist in the electronics industry. Fortunately, or unfortunately, depending upon the perspective, companies can exist and produce products without such comprehensive and robust systems, processes, and methodologies. Electronic product manufacturing companies can and do get products out the back door by changing the product, reworking, tweaking, inspecting in quality, and otherwise brute force manufacturing products. Costs and time to make engineering changes are not so obviously prohibitive as in the IC process. The negative consequences of making changes to the competitiveness may be as serious but probably will not be noticed. This is especially true because most accounting systems do not capture and report the total impacts of these types of activities.

DFX MUST BE CONSIDERED AT THE START OF A PROJECT
The importance of making the correct decisions before actual design begins was documented by the Ford Motor Company many years ago. The results illustrated in Figure 1 illustrate that more than eighty five percent of the Manufacturing cost of a product is fixed within the first five to ten percent of the development time. The percentage is even higher for electronics and is still higher for IC's. This shows the need for a comprehensive and complete analysis of the alternatives and consideration of DFX guidelines before beginning the actual design of an electronic assembly or product.
Percent of Total Manufacturing Cost Fixed vs Development Stage of Products

Phases of Product Development

Figure 1. Percent of Total Manufacturing Cost vs. the Development Stage of the Product

Figure 2: Flexibility to Change Costs vs the Board Design Stage

The flexibility to control costs quickly diminishes as the product is developed. This is illustrated in Figure 2.

COMPANY SIZE: ADVANTAGE OR DISADVANTAGE?

Few product development and manufacturing organizations have the integrated and predictive processes characterized by the Integrated Circuit industry. Business research documented by Bennett Harrison in his book, Lean and Mean, describes the gains made by larger US, UK, and EEC companies compared to smaller companies [2]. While smaller US companies have done better at product innovations, larger companies have an advantage in process innovation. A key element in the core competence for the IC industry is the integrated, robust development and manufacturing process methodologies and technologies. Product manufacturing companies that have integrated, robust and comprehensive new product development processes are likely to have definite advantages as the electronics industry matures. The dominant positions of the large Japanese and Korean VCR manufacturers is a good
example. No new VCR competitor is likely to enter into this market.

Companies that have robust development processes are likely to dominate organizations that do not develop comprehensive development processes and capitalize upon the strengths of all functions and resources. All companies must rethink their development processes and optimize them around their specific needs, resources, and market requirements. Reengineering the product development processes to incorporate the appropriate DFX methodologies will provide the smaller companies with powerful weapons in the fight to be successful.

Success requires first being competitive, consistently profitable and then the possibility of surviving. Bennett Harrison's data from three studies of all types of businesses for the US, UK and the EEC is startling. The US press and the electronics industry generally have lauded the value of small entrepreneurial start up companies for creating large numbers of new jobs. One probably would interpret this as a measure of success. Bennett Harrison's "real" data from extensive research and studies over a base of all businesses in the US shows that a great deal of the growth in the smaller companies has resulted in the "lean and mean" down sizing of larger companies.

INTERNAL AND EXTERNAL MANUFACTURING
Harrison suggests that the work is shifting from the larger product focused companies to external process focused companies, the subcontractors. This is particularly true in the computer and electronics industries where very large subcontractors have emerged for fabrication, assembly, test and distribution of products.

The economic models for these mega-subcontractors begins to resemble those of the IC manufacturers. Their process controls, predictive models, DFX rules, cost models, volumes, procurement strengths, asset utilization, process technologies, internal focus, commitment and discipline are very effective. The resulting manufacturing costs for the subcontractor plus their "reasonable profit" is still less than the "manufacturing cost" of the final Product Manufacturing Company. At least that is what the Product Manufacturer's accounting system reports. The decision makers within the Final Product Manufacturing companies agree and believe it or they would manufacture the products themselves.

Why is this discussion presented? Because the reality is that the central theme of Design for Success or DFX is rapidly changing. It is quickly becoming Design for Survival. This is because the larger focused fabrication and assembly companies have the economics and management capabilities to carve core competencies from the innards of their customers and make a handsome profit doing it. Now that they have the subassembly and assembly manufacturing responsibility, they will and are often completing the final Product Manufacturing role. They have the competencies to compete in the Manufacturing Arena and are winning bigger and bigger pieces of the total profit pie. Their next logical step is to move down the product chain and vertically integrate forward, toward the final product. This will cause them to start competing for the actual design of the products in addition to the pure assembly and test roles.

The subcontractors now control the central data bases, DFX knowledge, and process capabilities required to effectively compete in the toughest part of the process, namely manufacturing the products. They are in a commanding position to become bigger players in the market. There are few examples in any industry where companies successfully vertically integrate towards the consumer. This is an excellent example and we can all watch it happening today.

The other reason to address this phenomenon is because the larger subcontractors must develop and commitment to provide very comprehensive DFX rules to their customers. They must have consistency, commonality, and proven designs to meet their business objectives. They have in fact become very similar to the IC manufacturers and for the same fundamental reasons. It must be even more important for the internal manufacturer because they typically do not have the resources to invest in the process technologies. There is little room for inefficiencies when competing with the large refined processes of the subcontractors.

Companies competing with these major players must quickly and effectively decide how they are going to respond. The previous discussions illustrate that the market is enormous and growing. However, small and large companies are at risk if they do not respond with a competitive product development and manufacturing strategies and capabilities.

The reality is that if a company loses its internal competency to develop and manufacture products better than the competitors, it loses some of its advantage in the market place. It must share some potential profits with its subcontracting partners. It is true that the company can still maintain a competitive advantage through Marketing, Sales, and Distribution. However, it is exposed to companies that do not have the overhead burden of a larger company and that can contract out Marketing, Sales, Design, and Distribution to provide much more competitive products into the marketplace.

THE PROCESS FOR SUCCESS
The need for paying attention to the details of New Product Development is obvious. It is sometimes easier to set up some DFX tools than to address the broader issues that may have more impact upon the business. Success requires excellent management and coordination, sound Business, Marketing, Sales, and Manufacturing plans and a sound and
effective product development process. The best DFX plan
will not overcome fundamental weaknesses in key strategies
or product plans. This is emphasized because often the
engineers and managers in the product development
processes sometimes are so heavily involved in DFX
programs and they ignore weaknesses in more fundamental
business issues. DFX is only one of the important issues to
increase the total quality of new product development.
Individuals should become aware of other fundamentals that
are necessary for success and act to address the issues.
Development engineers are very innovative, adaptive and
react to the situation to get the job done. However, the focus
must be to develop a process that works every time without
this extra effort.

Products developed by multifunctional teams that have
created or reengineered their own optimized product
development process consistently introduce products that:
  - Meet Specifications
  - Are Low Cost
  - Have Consistent Quality
  - Have a Short Development Time
  - Are Produced to Plan
  - Can Provide Rapid Volume Changes
  - Have a Minimum of Design Changes
  - Meet Profitability Objectives

A robust new product development process is required to
have the most effective DFX processes. Solid Business,
Marketing, Sales and Distribution, Product Development,
Quality, Technology, Financial, Cost Accounting and
Manufacturing strategies are essential. The strategies should
support each other. They should be clearly and openly
communicated and understood throughout the organization.
Strategies can vary from those of a being a technology
leader, cost leader, follower, or somewhere in between. It is
essential that all key managers have the same vision and
objectives for operating and making decisions.

The Product Development organization needs clear and
consistent direction to most effectively use DFX rules and
guidelines. Understanding the customers' real needs is very
important. A complete understanding of the marketplace and
competitors is essential to determine and define the product
features and specifications. There are many proven
methodologies to define customers' needs. The results are
essential to determine the market requirements, features and
specifications of the products to be developed. This is
particularly important to prevent false starts and reverts of
the development team. Development teams generally can
develop products much more quickly and effectively when
stable product plans are available.

**EMULATING THE IC DEVELOPMENT PROCESS**

The proposal was made that the processes and methodologies
available to IC designers are desirable and should be sought
for electronic assembly and final product manufacturing. A
comprehensive model for the process has been described in
the literature [3]. This model is based upon four separate
domains. They are Concurrent Design, Concurrent
Manufacturing, a Product Data Manager database, and a
Predictive model. The IC model previously described has
element a refined software to provide sophisticated modeling and predictive capabilities for all
input scenarios.

IC product development models incorporate all the elements
of DFX. The IC rules have been continually developed and
improved. Best practices and lessons learned have been
incorporated into the processes. The appropriate metrics have
been defined and the capability to facilitate what-if scenarios
is available. IC design rules and procedure summarize all the
DFX rules and criteria. The model described in [3] describes
the data base requirements for electronic products and
assemblies.

![Organizational Architecture of a Desired Database](image-url)
Examples of the information each function is responsible for are shown below:

- Product Data Manager: Concurrent Manufacturing
- Bills of Material: CAM Databases
- Product Structure: Internal & External suppliers
- Engr Change Requests: Manufacturing Models
- Engr Change Orders: Produceability metrics & data
- Purchase Orders: Process capabilities
- Approval forms: PPM data by process & process
- Electronic Approvals: Mfg. rules and best practices
- Drawings: Process documentation
- Text Files: Preferred components
- Process Sheets: Preferred technologies
- Part Data: Preferred suppliers
- History Files
- Expert System Database
- Group Technology

Concurrent Design

- PWB Design Rules
- CAE Tools
- CAD Tools
- Performance Models
- Simulation Models
- Cost vs. Complexity
- PCB Test Rules
- Fab Test Rules
- ICT Test Rules
- Technology Profiles
- Rework Rules

Predictive Engineering

- Design for models:
- Minimum Complexity
- Fabrication
- Assembly
- Fabrication Test
- ICT
- Final Test
- Environmental
- Packaging
- ESD
- True Costs
- Auto Router Rules and Metrics
- Technology Characterizations
- Materials Characteristics
- Optimum Design Density
- Relative Cost Indexes
- SMT Assembly & Test
- MCM Application Rules
- Chip on Board Application Rules
- IC's Applications and Rules

This approach often is very effective because the individual engineers representing all the functions have the opportunity to be innovative and create better solutions when addressing the issues. The manufacturing engineers also know of the new processes and technologies that must be considered when introducing new products. Only the individuals responsible for the specific processes within the company or the key suppliers know all the metrics, the limitations, and the characteristics to expect when the product is to be manufactured. The multifunctional team that uses the DFX tools, resources, and technologies available can be very effective.

Many examples exist where new product development teams have reengineered their development processes to incorporate the right organization, processes and apply DFX criteria. The results demonstrate developing products in thirty to fifty percent of the time previously required. Substantial improvements are gained in the cost, performance, quality, responsiveness, and flexibility of the resulting manufacturing process. The results provide more revenue, profit, and market share. These benefits are essential to short and long term success.

**REENGINEERING, MORE THAN A FAD**

Pay Attention to This Buzzword. Reengineering is like many other concepts. Many, many people were doing it before they knew what "It" was. The process could be called "doing the right things" or "that is how we operate." Like so many things today, unfortunately buzzwords and acronyms rather than internal proposals capture the attention of so many executives. It often fits into the "silver bullet" or "add water and stir" approach to solving America's management problems. However, this is one technique to pay attention to and not ignore. This is one methodology that will facilitate major change is a very short time. It provides a very effective way to develop and optimize the most effective product development process for a company. Fortunately it is quite easy to implement and use.

Reengineering can be very easily applied by the smallest of organizations. Typical product development Core Teams have less than ten members. Often, that is the size of the entire engineering department or company in a smaller company. The potential benefit is especially important for smaller companies that do not have processes documented or well thought out. The process forces people to completely think about the total process rather than optimizing each separate function. It develops the most effective alternatives to develop products in much less time. This is accomplished while people representing the entire development, manufacturing, and distribution process are present to insure that all objectives are met.
This also applies to the largest of companies. Few companies have taken the time to optimize their development processes. If they have documented them, it is doubtful that the documentation is current and will not likely represent the processes that will be in existence when the new products are introduced. This is because many companies are actively pursuing a continuous improvement approach to manufacturing and are continually improving the manufacturing processes.

The only people that really know what is currently happening in a manufacturing operation are the people working there. The people that know the processes are the Process Engineers, Manufacturing, Tooling, Test, Quality, and other engineers; the managers, the suppliers and the people working in the processes. They know what and when process improvements should be made. This is the real knowledge database that exists in most companies and it is essential that these people be the ones that are involved in the reengineering process. They know the exact details of every desirable DFX issue and know how and when they can and should be used. The entire process can be developed and analyzed at the same time and optimized for maximum effectiveness.

There are equivalent resource pools in the other functional areas. Key people from Engineering, Sales, Marketing, Quality, Materials, Management, Cost Accounting, Suppliers, Regulatory and others are ready and willing to participate in finding ways to develop competitive advantages and compelling products. They have the ball and the game cannot be played without their direct involvement. These people must be directly involved. They have the knowledge and abilities to make the best decisions. This means that some outside person can develop better plans than they can do themselves. It simply does not make sense.

The resulting reengineered process is the composite of all the good ideas, DFX tools, innovative ideas, best practices and best judgements of the people involved in the product development and the process owners. It also provides a format to include the best ideas of key Suppliers and key Customers. It provides a mechanism to achieve agreement between the Development Team and Management regarding the objectives, the processes, the investments, and time frame to achieve the objectives.

**REQUIREMENTS FOR EFFECTIVE DEVELOPMENT TEAMS**

The importance of multifunctional development teams is accentuated because the process relies upon the internal knowledge, expertise, judgment, innovation and other capabilities of the specific individuals involved in the reengineering project. The Framework for information described in Figure 3 is typically not available and must be provided by direct interaction between the individual team members. The functional departments must be represented either on the Core Team or Extended Team. Co-location of the Core Team is also very important for all the reasons described in articles regarding effective product development organizations.

**DEVELOPMENT TEAM MEMBERS**

The multifunctional team should be chosen and the Team Leader selected. This would include the Core and Extended team members. Each person would represent one key function required to successfully develop the product. The Team Leader is typically from R&D or Product Management but any qualified person could be the team leader. This person is the key contact point with Senior Management and provides the leadership, coordination, and control of the project for the team. It is better to have this person monitor and manage performance to the resulting schedule. It is strongly recommended to not have a "project coordinator" specifically for the purpose of managing the project and schedule as will be explained later.

The functions represented on the teams depend upon the specific product to be developed. The following functions would be represented for a typical product with electronics, firmware or software and some mechanical features other than packaging of the product. This is not a rigid recommendation and individual teams may suggest more or fewer functions represented on the Core Team. Some teams may only have three or four total members.

<table>
<thead>
<tr>
<th>Core Team</th>
<th>Extended Team</th>
</tr>
</thead>
<tbody>
<tr>
<td>Team Leader</td>
<td>Sales</td>
</tr>
<tr>
<td>Circuit Design</td>
<td>Human Resources</td>
</tr>
<tr>
<td>Mechanical Design</td>
<td>Management</td>
</tr>
<tr>
<td>Test Engineering</td>
<td>Key Suppliers</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>Service</td>
</tr>
<tr>
<td>Quality</td>
<td>Key Customers</td>
</tr>
<tr>
<td>Software/Firmware</td>
<td>Reliability</td>
</tr>
<tr>
<td>Procurement</td>
<td>Cost Accounting</td>
</tr>
</tbody>
</table>

The team members are expected to represent their function on the team and can speak and commit for their function without always going back to the "boss" for a decision. The tasks and times to accomplish each task must be agreed to by each of the individuals on the team. This requires that the representatives be well-qualified members of the departments they represent and able to make decisions without undue checking with their manager. It requires that the team members be qualified to make decisions that their managers agree to and will support. Their managers will be aware of the decisions that must be made and when the decisions are due. The comprehensive schedule that will result from this process requires that the functional management review, agree or modify, support and commit to the resulting reengineered process and schedule. The team members and their direct managers will be aware of the nature of decisions and commitments that must be made well in
advance of the date required. They will have adequate time
to plan, decide, and commit to the decisions.

PREPARATION TO REENGINEER THE
DEVELOPMENT PROCESS
Specific objectives for the product or product must me clear,
understood and agreed upon by all Functional Managers, key
individuals and the team members. This considers the
Business, Marketing, R&D, Manufacturing, Sales, Financial
and other key objectives. Reengineering the product
development process should focus on a specific product or
product family. Reengineered processes for a specific
product can be easily expanded to a family of products or a
product line. It is very important that the specifications of
the product be agreed upon by all parties before starting the
design of the particular hardware and software. This does not
prohibit the use of reengineering a process to determine and
define the specifications. However, it is very important that
the specifications be firm and agreed to by all parties;
especially Sales, Marketing, and R&D, before detailed
hardware design is begun.

It is particularly important that the departments have
agreement upon which specific DFA criteria they want
incorporated into the reengineered process. It is also
important that each set of criteria be documented and
understood so that all team members can help modify or
support to result in a better product. For example, if Design
for Serviceability is considered, there should be objectives
and an appropriate set of actions, results, and metrics to
support the requirement. The Design for In Circuit Test has
a specific set of criteria that is dependent upon the devices
used, the placement equipment, the test equipment, and the
techniques to test and analyze the circuits, electronic
assemblies, and final products. These techniques and
requirements are usually well understood and documented.

REENGINEERING THE DEVELOPMENT PROCESS
The team members develop complete lists of the tasks and
expectations required to design, develop, manufacture, test,
and package the product. This list should be developed by
the team member and the other key people in the functional
department they represent. Considerable thought should be
invested to develop the products expecting that there will be
no engineering changes required. It should also be expected
to arrive at a product that has the lowest cost, highest
performance and quality. This may sound unreasonable but
these conflicting requirements can be usually met with the
ingenuity and creativity of the individuals and still introduce
the products in much less time.

The full team will develop a Process Map of the processes
and procedures to develop the product that meets all the
objectives and incorporates all the DFA and other tools and
best practices. This resulting process represents the integrated
model of the most effective process to develop the product.
It will include all the milestones, tests, reviews, and
requirements defined to develop products. The resulting logic
of the individual tasks in the Process Map is reviewed,
modified, improved and worked with until all parties agree
upon the results.

The resulting map is typically a very complex item. The
team needs a tool to work with this map to optimize,
manage, and complete. Project Management software for
PC's is ideal. The map is entered as a PERT Chart and then
all the power of project management software can be applied
to the map. The process map incorporates all the
development objectives, milestones, reviews, tasks, activities
and DFA tools. It insures the best possible product is
developed in the least time without abusing people or short
cutting the standards, specifications, or objectives.

Project Management software, such as Microsoft Project,
provides a powerful tool set to optimize the result. Special
reports for the Team Leader, each individual team member
and management status reports are readily available. This
software has almost too much capability. The
recommendation is to only use the basic capabilities. Avoid
trying extra fancy or complex features until people are
experienced in managing projects with the basics. After the
plan is complete, it is suggested the team work with and
record progress and status on hard copy paper reports and
avoid working in the computer. Experience suggests that as
much time can be spent keeping the computer updated as is
required to develop the project.

APPROVAL OF THE FINAL PROCESS AND
SCHEDULE
The final development schedule should be reviewed and
approved by the total team. The result should be tested
against all the project objectives. Project Management
software provides immediate projected dates for completion.
In-depth critical path analysis should be conducted to
thoroughly review the logic, reality, and robustness of the
final schedule. The final result is then reviewed by Senior
Managers and approved. Special attention should be focused
to insure that all the elements of the DFA criteria are
effectively and efficiently satisfied. The final approval of the
schedule is essential before beginning development.
Beginning major design and development before the
Development Team and managers agree is a poor practice
and often causes problems later in the project because of
misunderstandings at the beginning.

The management approval to begin starts the actual and
formal development process. Regular weekly status meetings,
held on Monday or Tuesday of each week are essential.
Special care should be taken to avoid long, inefficient, and
boring meetings. Conduct quick status meeting and let
everyone get back to work. Anyone experiencing problems
meeting their commitment should advise the Team Leader
and work out the details before they become late. Every
effort is to meet the dates on or before the task is due and micromanaging is absolutely to be avoided. Team members are responsible for their own independent professional work and the Team Leader is not expected to provide regular encouragement to meet dates or performance criteria. That is the responsibility of the individuals.

MANAGING TO SUCCESSFUL COMPLETION
The Development Team is involved until the project is managed to successful completion. This means meeting or exceeding all the expectations. It also involves learning from the process about refining estimates, avoiding weak components, choosing stronger suppliers, focusing on critical issues, etc. These new lessons learned and best practices should be incorporated into the basic development process and considered for inclusion into the next project.

Regular management reviews are typically included in all development processes. They are also included in the reengineered process. The frequency and timing is negotiated with the appropriate managers. This can also sometimes includes key customers. Care must be taken to remember that Senior Managers are a very important group of Customers. Key managers, like key customers, are very important and need to have good communications. This does not mean that specifications should be allowed to change but managers do have a great deal of accountability and responsibility to the company. They must be informed and aware of the status of the company’s investments in new products.

TYPICAL RESULTS
The typical results from a large number of reengineering projects are truly impressive. These are some common results achieved for reengineered product development processes:

- 40-70% Reduction in Product Development Times
- 15-40% Reduction in Product Costs
- 40-80% Reduction in Number of Parts
- 40-90% Reduction in Product Assembly Times
- 30-90% Reduction in Manufacturing Lead Times
- 50-80% Reduction in Manufacturing Space
- 25-65% Reduction in Number of Suppliers
- 15-70% Reduction in Tooling Costs
- 25-90% Reduction in Engineering Change Orders

CONCLUSIONS
The Product Development Processes are the most important processes within any company. Very strong growth in the global electronics market and tremendous competitive pressures will significantly increase the demand to develop more competitive products in significantly less time. The processes are affected by nearly every functional department from Sales through Distribution and Field Support and every function has a meaningful input into how to best design and develop the product. The total process should be reengineered by the people on the development team. The Product Development Process includes tasks, reviews, milestones and DFX issues that satisfy the requirement from each function to produce the most competitive product possible. Each person on the team has the opportunity to define their tasks and time required to complete the tasks. It typically requires a Development Team about ten days to reengineer and develop a comprehensive plan and schedule. The resulting plan produces specific tools for each individual that defines what and when their tasks need to be completed. Design for X rules, principles and guidelines must be considered at the very beginning of the development process to most effectively impact the final result. Major improvements in competitiveness are gained by effectively addressing the development process and using DFX principles.

ACKNOWLEDGMENTS
The author would like to thank Mr. Happy Holden of the Hewlett-Packard Company for his ever present challenges and motivation to find more effective product development processes.

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(1) American Electronics Association, "AEA World Electronics Outlook" March 1994
(3) Holden, Happy, "Optimizing PWB Designs: The Focus on Metrics", Hewlett-Packard
INTRODUCTION
The focus of this paper is on Design for Manufacturability (DFM) from the bare board fabricators' perspective. In the mid 1980's the PWB (Printed Wiring Board) industry began to feel the impact of the increasing complexity of integrated circuit packaging. Since then we have seen the transition from 16 pin dual in-line packages with leads on 0.100 inch centers to 340 pin ultra fine 0.012 inch pitch components. To compound matters, the density of the components increased as the number of functions required per board increased. Initially, the term "manufacturability" referred to the capabilities of insertion and placement equipment i.e. component orientations, spacing, heights, etc. In an effort to improve yields, bare board manufacturers began to follow the lead of the assemblers who had already initiated Design for Assembly (DFA) programs. By 1987 several large captive manufacturers had developed formal approaches to DFM and were actively working with their PWB designers to improve manufacturing yields. Some of the obvious benefits of designing manufacturability into bare boards include:

- Higher quality
- Reduced lead times
- Lower labor and material costs
- Higher first pass yields

Because of the success of these early DFM programs, they have become an integral part of the preproduction engineering departments of many North American fabricators.

The evolution of these DFM programs during the last decade can be broken into three distinct phases:

- Establishing the DFM discipline
- Automating the DFM analysis
- Expanding the DFM scope

The first phase of these programs was the domain of the fabricators. Using traditional methods and technology preproduction engineering departments developed screening methods to manage the increasingly complex designs that resulted from surface mount technology. As the discipline matured and the benefits of DFM were established, third party tooling software suppliers recognized the need for greater analytical speed and accuracy thus initiating the second phase.

Today we have entered a new phase with the advent of automated repair software. This software allows for rapid, reliable "repair" of design problems that are detected in the analysis.

ESTABLISHING THE DFM DISCIPLINE
The DFM programs developed by fabricators have rating methods for assessing manufacturability or producability of a given design. These scoring schemes, whether manual or highly automated, take into consideration three critical factors:

1) Component packaging technology and associated design attributes i.e. hole sizes, annular rings, traces and spaces, etc.
2) Complexity factors which characterize the complexity of the design attributes
3) Manufacturing cost drivers

1) Component Packaging Classes and Associated Design Attributes
The choice of component packaging technology determines the requirements for hole sizes and tolerances, traces and spaces and many other critical design factors which impact the manufacturing yields. Therefore, the first step in setting up a DFM rating scheme is to categorize designs from least complex to most complex based on component packaging technology. A design with 16 pin DIP packages would represent the least complex while a design incorporating 340 pin ultra fine 0.012 inch pitch components would represent the most complex.

<table>
<thead>
<tr>
<th>Class</th>
<th>COMPONENT PACKAGING</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Low density: Through hole designs (one or two traces between integrated circuit pins placed on 0.100 inch grid).</td>
</tr>
<tr>
<td>II</td>
<td>Medium density: Typically mixed through hole and surface mount technology designs (one trace between vias placed on 0.050 inch grid).</td>
</tr>
<tr>
<td>III</td>
<td>High density: Surface mount designs, two and three tracks between feed through noles placed on 0.050 inch grid.</td>
</tr>
</tbody>
</table>

Table 1: Component Packaging Classes
The second step in developing a rating system is to determine what are the typical physical characteristics associated with the design classes. This is relatively simple as the CAD (Computer Aided Design) systems require pad geometries in order to set up the component libraries. The pad geometries in turn determine the largest size trace which can be used to provide connectivity when the design is routed. The size of any required component or feed through holes is also fixed by the pad geometries.

Figure 1 is an example of pad construction for a 16 pin DIP package. This design has two traces routed through 0.100 inch centered through holes (in the illustration above, this design would be a Class 1, low density design):

- Pad diameter 0.055 inch
- Hole callout 0.035 + 0.005/-0.005 inch; preferred drill diameter 0.041 inch
- Trace width 0.009 inch/Space width 0.009 inch

**Figure 1**

The following is an example of preferred pad constructions for a surface mount design which has one trace through 0.050 inch centered via (feed through) holes (in the illustration above, this design would be a Class 2, medium density design):

- Pad diameter 0.031 inch
- Hole callout 0.021 + 0.000/-0.021 inch; preferred drill diameter 0.021 inch
- Trace width 0.006 inch/Space width 0.006 inch

**Figure 2**

Understanding the design attributes required by the selected component packaging technology allows one to set up subcategories for each design attribute. From a bare board perspective, the component packaging technology is commonly referred to as "6 and 6", "5 and 5", "4 and 4", etc. referring to the traces and spaces required in the routing of the different design densities.

The third step is establishing a scoring methodology which results in a numerical rating. Appendix I shows an example of a matrix of attributes which have been associated with given component technologies. A Complexity Index or Matrix characterizing the complexity of physical characteristics (size, layers, holes, traces, etc.) allows one to easily calculate the first pass yield which is essential to both costing and pricing. Metrics establish a common language that links manufacturing to design. The equations or tables allow for analysis of various factors and result in a numerical score. If the score meets producibility requirements, then the design may be approved for tool and build. The following chart is an example of how the Hewlett-Packard Loveland facility has characterized first pass yield as it relates to increasing complexity.

The fabricator's success depends on being able to characterize his processes and keep them in statistical control. The fabricator must understand processing variables or the ratings are meaningless. Process Engineering must design experiments (DOE) which characterize process capability with respect to the end product parameters. Several approaches have been taken to come up with manufacturing capabilities. DOE's may be run looking at a single attribute such as minimum drill capability, smallest trace and space on a given copper weight, etc. Another approach which has been taken is to select a representative design and systematically vary the design attributes to determine tradeoffs. Statistical process control must be in place in order for the stated capabilities to have any validity.

Understanding the design attributes required by the component packaging technologies combined with stated manufacturing capabilities allows the fabricator to develop "preferred pad constructions" as well as design rules and guidelines for optimum yields. For example, with reference to the pad construction shown in Figure 2 above, it would not be unusual to see an 0.008 inch trace, 0.008 inch spaces and correspondingly smaller drill diameters and pad sizes. However, depending on the thickness of the board, the resulting aspect ratio could present problems for the fabricator. The goal is to simplify the product and make it easier and less costly to manufacture.

2) Complexity Factors

The following are typical design attributes which can be physically measured, associated with one or more component technologies and represent varying degrees of difficulty in the manufacturing process:

- Inner and outer layer trace and space width
- Drill diameters/Final plated hole tolerance
Complexity Index

- Annular ring
- Clearance pad diameters
- Nominal finished board thickness
- Board thickness/hole size/aspect ratio
- Copper clad weight of the laminates/foils
- Overall finished profile tolerance

It should be noted that although the attributes are common to PWB's, manufacturing capabilities are vendor specific. The IPC (The Institute for Interconnect and Packaging Electronic Circuits) has recognized the need for vendor qualification, and has introduced a document aimed at assisting OEMs in evaluating and assessing the capabilities of PWB fabricators, IPC-1710, "Manufacturer's Qualification Profile."

The following is a brief discussion of the key design attributes and how they impact bare board manufacturer:

1) Minimum Trace and Space Width (typically measured on the master plotted artwork).

The smaller the line width, the more challenging the image reproduction as it relates to imaging and etching. The designer must understand the fabricator's line width capabilities and the expected yields. The thickness of the copper is a key factor for achieving minimum line width within required tolerances on outer layers because of the additional pattern plate. The minimum line width improves significantly with 0.5 oz. copper clad in the 0.006 to 0.007 inch range and becomes a requirement in the 0.006 to 0.005 inch trace width range. This is especially critical to the designer who is working with impedance lines on the outer layers. It can be an unpleasant surprise to learn that in order to manufacture the design to specified impedance values the line widths must be reduced to 0.005 inch, but the outer layers were designed with 1 ounce material compromising the manufacturing yields and associated costs.

2) Minimum Drill Diameter

Fabricators' drilling capabilities are typically stated as the smallest drill size that can be used in a production mode. Stack heights (how many panels may be drilled at a given time) are determined in large part by the smallest drill size and can therefore, have a significant impact on the cost associated with drilling. The designer must be aware of their vendor's minimum drill size capability and what the associated cost is when selecting a technology set to ensure there is a good match. Minimum drill size is not only a driver for drilling cost, it may also have a significant impact on the reliability of the board as it impacts annular rings and aspect ratio (see below).

3) Inner and Outer Layer Annular Ring (The difference between the drill diameter and the corresponding circuitry pad diameter as measured on the master artwork.)
It is important that the designer not only understand the finished board specification with respect to annular ring, but additionally what the capability of the vendor is to meet this requirement. The pad constructions that the design has dictated must allow enough registration tolerance in order to fabricate the boards to customer specification. The fabricator may or may not include the plating in the hole wall (typically 0.001 inch of copper) when stating their capability. Issues with annular ring can often be resolved by increasing the pad size or decreasing the drill size.

4) Ground Plane Clearance
Ground Plane Clearance refers to the removed portions of a ground plane that isolate it from a drilled hole in the base material to which the plane is attached. Clearance is determined by measuring from metal to metal on the master artwork. To ensure the minimum required clearance can be maintained on the finished board, the minimum required electrical clearance plus the image and drilling tolerances must be added together to determine the appropriate clearance pad diameter. (Refer to IPC-D-275 Design Standard for Rigid Multilayer Printed Boards and Rigid Printed Board Assemblies for specifics).

If the plane layer design leaves strips of copper between clearance pads, a minimum spacing must be maintained between clearance pads to avoid causing shorts due to resist lifting and redepositing. (Again measurements are taken on the master plotted artwork.)

5) Aspect Ratio
The maximum board thickness divided by the smallest selected drill diameter. The maximum board thickness is the calculated thickness over copper before plating. Additional thickness caused by plating, hot air solder leveling, or soldermask has no impact on aspect ratio.

Aspect ratio is critical to reliable copper plating thickness in the hole wall. The greater the aspect ratio the more difficult the board is to plate and at some point the fabricator’s ability to produce reliable product is compromised.

3) Cost Drivers
In addition to understanding how the design drives costs, the designer must understand the key cost drivers relative to bare board manufacture. The cost drivers are:
- Raw laminate - both panel utilization and material selection, i.e. mixed dielectrics, non-standard materials, etc
- Number of layers
- Number of different drill sizes and total number of holes
- Gold requirements
- Mechanical tolerances, i.e. plate thickness, hole-to-hole, edge-to-edge dimensions, etc
- Solder mask requirements
- Electrical test parameters
- Yield

When all factors are considered, complexity factors as well as the additional cost drivers, a "score card" can be developed to quickly and accurately predict first pass yields as well as price. The Table 1 below is an example of a score card approach.

In the late 1980's the first step in the DFM analysis was manually filling out a check sheet. The single image plots were measured and trace and space widths as well as pad sizes were recorded. Drill sizes were selected and manual calculations were made to determine the annular rings and aspect ratio for the design. This inspection step took several hours and was prone to errors. Design Rule Checks (DRC's) are generally a standard Computer Aided Design (CAD) system feature. However, they do not provide an adequate tool for assessing whether or not the design can be fabricated efficiently and at a reasonable cost. They do not take into account drill information that impacts two very critical variables in PWB manufacture, annular ring and aspect ratio.

The original intent of the Merix Complexity Factor Matrix and accompanying documentation was to aid the preproduction engineering department in screening jobs for producability before loading new designs to the manufacturing floor thereby improving yields. It soon became evident that it would be beneficial to develop a
<table>
<thead>
<tr>
<th>FABRICATION FACTORS</th>
<th>pts.</th>
<th>Highest</th>
<th>pts.</th>
<th>High Middle</th>
<th>pts.</th>
<th>Low/Middle</th>
<th>pts.</th>
<th>Lowest</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material of Construction</td>
<td>147</td>
<td>Polyimide</td>
<td>88</td>
<td>Cyanate Ester</td>
<td>49</td>
<td>FR-4</td>
<td>40</td>
<td>CEM III</td>
</tr>
<tr>
<td>Number of Layers</td>
<td>196</td>
<td>8 layers</td>
<td>137</td>
<td>6 layers</td>
<td>89</td>
<td>4 layers</td>
<td>36</td>
<td>2 sided</td>
</tr>
<tr>
<td>Number of Holes / Panel</td>
<td>270</td>
<td>&lt;20,000</td>
<td>100</td>
<td>10,000 - 20,000</td>
<td>90</td>
<td>3001 - 10,000</td>
<td>27</td>
<td>1 - 1000</td>
</tr>
<tr>
<td>Lithography (traces &amp; spaces)</td>
<td>25</td>
<td>&gt; 4 mils</td>
<td>10</td>
<td>4 - 5 mils</td>
<td>6</td>
<td>6 - 8 mils</td>
<td>1</td>
<td>&lt; 8 mils</td>
</tr>
<tr>
<td>Gold Tabs</td>
<td>48</td>
<td>1 Side, &lt;3 sq.inch or 2 Side, &lt; 3.5 sq.inch</td>
<td>32</td>
<td>2 Side, &lt;3 sq.inch or 1 Side, &lt; 2.5 sq.inch</td>
<td>16</td>
<td>1 Side &amp; &lt; 1.5 sq.inch</td>
<td>0</td>
<td>None</td>
</tr>
<tr>
<td>Annular Ring</td>
<td>30</td>
<td>&gt; 2 mils</td>
<td>21</td>
<td>2 - 4 mils</td>
<td>7</td>
<td>4 - 6 mils</td>
<td>1</td>
<td>&lt; 6 mils</td>
</tr>
<tr>
<td>Solder Mask</td>
<td>25</td>
<td>2 Sided Dry Film</td>
<td>17</td>
<td>2 Sided LPI</td>
<td>10</td>
<td>1 Sided LPI</td>
<td>5</td>
<td>Screened - 1 side</td>
</tr>
<tr>
<td>Metalization</td>
<td>75</td>
<td>Electroplated / Reflowed Tin-Lead</td>
<td>69</td>
<td>SMOBC / SSC</td>
<td>46</td>
<td>SMOBC / Electroless Ni/Au</td>
<td>29</td>
<td>SM0BC / Organic Coated</td>
</tr>
<tr>
<td>Minimum hole Size</td>
<td>166</td>
<td>&gt; 8 mils</td>
<td>64</td>
<td>8 - 12 mils</td>
<td>60</td>
<td>10 - 20 mils</td>
<td>5</td>
<td>&lt; 20 mils</td>
</tr>
<tr>
<td>Controlled Impedance</td>
<td>105</td>
<td>+/- 5%</td>
<td>62</td>
<td>+/- 10%</td>
<td>30</td>
<td>+/- 20%</td>
<td>0</td>
<td>None</td>
</tr>
</tbody>
</table>

**Points are PER PANEL**

| For board, divide by # per panel |

DFM manual with rules and guidelines that could be used to train PWB designers. Some of the pitfalls could then be avoided at the design stage or worst case, soften the blow when manufacturability issues were encountered. The first edition of the Merix DFM manual went to press in June 1988 and has seen many revisions over the years.

Phase I of the DFM program evolution drew to a close with a solid foundation in place. However, the procedures for analysis were manual and cumbersome. Because artwork was required, problem detection was not quick enough to avoid wasted time and energy.

**AUTOMATING THE DFM ANALYSIS**

Fortunately, Infinite Graphics Inc. (IGI), a tooling software supplier, recognized the need for an automated design analysis. IGI software developers used the Merix Complexity Factor Matrix as a backbone and developed the ScriCAM PAR® (Producability Analysis Report) program. This pioneering program automatically reads the customer's design data and provides a complete design analysis. If there are potential tooling or manufacturing issues, communication can occur within hours rather than days.

Integrating an automated DFM program on the front end of the tooling stream significantly increases the output of a tooling department Merix, as well as many other PCB manufacturers, integrated PAR® on all incoming designs. This necessitated restructuring computer aided tooling (CAT) departments as well as converting preproduction engineering personnel from personal computers to X terminals. Tooling technicians were "transferred" to sales support teams.

Immediately upon receiving the customer data over modem or the Internet, the data is read into the tooling system. The drawings are plotted first so that the preproduction engineering activities as well as the DFM analysis can be run in parallel. Any custom apertures are set up and customer specifications are reviewed for any nonstandard requirements. The DFM analysis requires input of the design's hole size callouts including specified tolerances and plating type from the fab drawing. Merix tooling software support engineers developed an automated drill selection program that consistently and rapidly selects the correct drill sizes. After the drill sizes are assigned, the DFM analysis is run. Within an hour or two, this analysis can be reviewed by preproduction engineering. Any conditions that do not meet DFM requirements are resolved with the customer before loading the job to tooling. If single image artwork plots are required by the customer, they can be plotted in parallel with the analysis.
The software produces detailed reports, in both graphic and
text formats, that list typical spacing values and deviations
from desired specifications, soldermask values, surface
mount pad geometries and drill summaries. The following
detailed checks are performed:

**Signal layer checks:**
- Pad to trace spacing
- Trace to trace spacing
- Hole to circuit spacing
- Circuit to non-circuit spacing
- Trace Width
- Annular ring
- Geometry to board edge.

**Plane layer checks:**
- Clearance to clearance spacing
- Clearance annular ring
- Thermal annular ring

**Soldermask Layer checks:**
- Minimum trace overhand
- Minimum sliver
- Annular ring with signal layer

**Solderpaste Layer checks:**
- Minimum sliver
- Annular ring with signal layer

**Silkscreen layer checks:**
- Minimum line width

Ideally, the data generated by the DFM analysis is integrated
with a traveler (manufacturing routing) generation system to
ensure the appropriate manufacturing processes are selected.
Merix has a sophisticated Computer On-line Tracking
(COLT) system that drives traveler generation and the shop
floor control system from a central database. The data
generated by the DFM analysis is input into a part specific
database.

An example of design characteristics that can be directly
associated with manufacturing constraints are trace width and
copper weight at the outer layer etch operation. If a design
has 6-mil traces and spaces on the outer layers, a program
can be written to ensure that the appropriate clad weight is
selected (less than one ounce). A heavier clad weight may
compromise the trace width at outer layer etch after plating.
It is also more cost effective as well as environmentally
friendly to use the lighter clad weight. A second example of
how a design characteristic drives manufacturing processes
is with respect to parts with high aspect ratios. The diameter
of the minimum drill as well as the calculated thickness of
the board after lamination can be used by the system to
determine aspect ratio. An algorithm can be run to determine
what type of copper plating the hole wall will receive based
upon the calculated aspect ratio. If high aspect ratio plating
programs are called for, preproduction engineering can be
flagged on-line and any necessary adjustments to trace
widths in order to meet specified impedance requirements
can be made. Because of these types of sophisticated
algorithms, Merix first pass yields on impedance boards is
very predictable.

Manufacturability issues not so easily quantified and for
which manufacturing capabilities have not been characterized
remain problematic. These "gray areas" are more difficult to
automate and thereby simplify. Without metrics, establishing
rules and guidelines are difficult. Internal low pressure areas
and plating imbalance result from designs that do not have
"good" circuitry distribution. Product Engineers are routinely
relied upon to troubleshoot these types of manufacturability
issues. Guidelines and suggestions rather than rules are
typically the norm.

For example, the Merix DFM manual states, "Circuit area
and distribution between front and back of the board should
be balanced within 10%. Plating thieving of low pattern
density and cross hatching of external plane areas should be
considered." Process characterization studies need to be
performed to determine where yields are impacted before our
tooling software partners can supply the solutions for
automated DFM checks as well as repair.

The overall benefit of an automated design check is a
significant reduction in cycle time for customers as well as
improved accuracy. Some side benefits have resulted as well.
Single image plots are no longer needed in order to "view"
the board design. The data can be viewed in the X-terminal
graphical window environment. Critical line width
measurements can be made on-line more quickly and
accurately than waiting for single image plots to measure
with a microscope with a measuring reticule. Automated
Optical Inspection (AOI) of the photo plots as a means of
checking for spacing violations becomes unnecessary.

Due to the difficulty of maintaining controlled hard copy
issues of DFM manuals converting to an on-line system may
prove beneficial. The hard copy manual can be replaced with
computer disks so that customers can also put the
information on-line for use on their systems. In the past
large design centers received as many as twenty hard copies
that quickly became outdated. Today an updated disk can be
delivered periodically to a customer focal point and the
information updated on-line. The plan for the future is to put
the Merix DFM information on the World Wide Web
allowing Product Engineering to provide real time updates.

**Documentation and CAD Data Check List**
These are the minimum requirements necessary to perform
a manufacturability assessment:
- CAD Image data (Gerber Data or IPC-D-350)
— Aperture lists
— Drill files (X,Y coordinates)
— Fab (mechanical) drawings (HPGL files)
— Net List

Preferably this data is transferred via a modem or the Internet.

PHASE III: EXPANDING THE DFM SCOPE

An area that still presents opportunities for both tooling and manufacturing is related to problems with the dimension on fab drawings. Often dimensions are missing or incorrect. The tolerances may leave no latitude for drilling or profiling. If the customer provides a board outline with the CAD data that is to scale, this outline can be checked to the fab drawing. It may also be used later in the panelization process as well as in developing the NC profile program. If a usable board outline is unavailable, a board outline must be created much earlier in the tooling process. This step will again move resources from the traditional CAT role back up into the processes, eliminating redundant steps and catching errors closer to the source before value is added.

The next major step in the development of DFM software is "DFM based automatic editing". Editing on tooling workstations is inefficient, time consuming and subject to errors at best. When the DFM analysis identifies a "design error" the question becomes who edits the CAD data and who updates the customer CAD files? This is particularly difficult when the problem has no impact on the performance characteristics of the design, but is a problem for fabrication. Merix is currently evaluating software that will increase the manual editing speed and quality. On-line design rule and netlist checks that are tied to materials and stackup information via a unified open database will prevent introducing new violations during the manual edit sessions. This will maintain both design integrity and manufacturing optimization. Chuck Feingold, Valor Computerized Systems, describes this next step forward as making the DFM programs "three dimensional" by adding the board construction as well as the functionality to the analysis. Knowing the design will not be compromised by manual edits, allows fabricators much more flexibility in "modifying" the CAD data to improve manufacturing yields.

A second new technology that will revolutionize DFM programs is Product Data Management (PDM). Today, it is the fastest growing technology within the scope of "CIM (Computer Integrated Manufacturing) related investments. According to CIM data’s Product Data Management Technology Guide, "PDM provides a means to manage all product related information as well as the processes utilized throughout the product’s entire life cycle. PDM integrates and manages processes, applications, and information that define products across multiple systems and media." PDM systems and methods provide a structure in which all types of information used to define, manufacture, and support products are stored, managed, and controlled. Typically, PDM will be used to work with digital files and database records. These may include:

— Specifications
— CAD drawings
— Geometric models
— Images (scanned drawings, photographs, etc.)
— Engineering analysis models and results
— Manufacturing process plans and routings
— NC part programs
— Electronically stored documents, notes, and correspondence
— Hardcopy (paper-based) documents (by reference)

In short, any information needed throughout an interconnect product’s life can be managed by a system, that makes correct data accessible to all people and systems that have a need to use them. This will allow both product and process engineers to view the customer data and all appropriate tooling files. Annotations can be made by a product engineer for reference by anyone needing to view the data. One of the successful PDM installations specific to our industry has been the Star 1000 Engineering Information and Archiving system. Companies using this technology report much reduced interruptions of their tooling resources.

CONCLUSION

The same benefits that were achieved when DFM programs were first implemented in the late ’80’s can be achieved more quickly and reliably today with automated DFM checks and repairs. Design for Manufacturability programs are evolving from manual design rule checks (enhanced by the addition of the fabricators drill information and material stackups) to on-line design rule and net list checks. Next generation preproduction, engineering systems are becoming available, that are based on open file formats and object oriented programming.

In reviewing the literature, the common theme for both Design for Assembly and Design for Fabrication is that the analysis is "too often postponed until after the design has been completed and the product is released to the fabricator and/or assembler" resulting in unnecessary delays and expenses. The analysis is too late in the design process to have maximum impact. The New Product Introduction (NPI) process is all one direction, from Design to Manufacturing. Because of this "one way" flow of information, fabricators and assemblers have developed DFX (Design for Assembly/Manufacturing) programs to protect their manufacturing operations from designs which negatively impact yields or disrupt the manufacturing process flow. Fabricators have developed DFM manuals and training
programs for their customers in an effort to minimize the number of designs which must be redesigned in order to be manufactured in a competitive manner. The current state of the manufacturability assessment may best be described as "Redesign for Manufacturability."

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REFERENCES:

APPENDIX

COMPLEXITY FACTORS MATRIX (June 1995)

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Key:
INN ------ Inner Layer  PLA ------ Plating  GE ------ Greater than or Equal to
DRI ------ Drilling SM ------ Solder Mask LT ------ Less Than
LAM ------ ML Lamination FIN ------ Finishing (Profiling) LE ------ Less than or Equal to
OUT ------ Outer Layer GT ------ Greater Than EQ ------ Equal to

Note: All dimensions are in inches
INTRODUCTION
Evaluating assembly efficiency of the surface mount product is too often postponed until after the design has been completed and the product is released to production. Design for Assembly efficiency is a process that should start during the products conception. With the cooperation of designers, manufacturing and test engineers, materials specialists and development engineers, most issues related to manufacturing efficiency can be resolved without impacting program schedules. The benefit of this concurrent activity during the products development phase ensures a smoother transition of the product into manufacturing. The term "Design for Manufacturing" (DFM) means more than efficient assembly... a product that is designed well should also be competitive in cost while providing a long and reliable service life.

Surface Mount assemblies, especially those with ball grid array, fine pitch and micro ball grid array devices, require continuous process monitoring and methodical inspection. For example, solder joint quality in the U.S. is generally measured against a criteria defined in both IPC-A-620 for overall workmanship and the National Solder Standard, ANSI/J-STD-001 which defines the requirements for a reliable solder connection. Understanding these guidelines and standards, the PC board designer can develop the land pattern geometry's that will provide the opportunity for process engineers to meet the industry established requirements.

MANUFACTURING EVALUATION
Design for Assembly (DFA) includes all aspects of the manufacturing process:
- Design for Assembly
- Design for Testability
- Design for (PCB) Fabrication

Before releasing a new design to manufacturing for volume assembly, a DFA evaluation of the finished surface mount product should be performed. The evaluation will include a thorough review of documentation, CAD generated data, materials and finished hardware (and when available, a prototype assembly).

ASSEMBLY DOCUMENTATION REQUIREMENTS
The preparation of clear and complete assembly documentation is vital to the successful transition of the product from the design/engineering environment into a production environment. Individuals developing the documentation and other necessary data for manufacturing should be aware of the expectations and requirements.

DOCUMENTATION AND CAD DATA CHECK LIST
- Bill of Material (BOM)
- Approved Vendor List (AVL)
- Assembly Detail
- Special Assembly Instructions
- PCB Fabrication Detail
- Gerber Data or IPC-D-350 File on Disk

CAD data is especially useful for developing machine tooling, programming of automated assembly systems as well as process and test fixture preparation.

DATA REQUIRED FOR ASSEMBLY PROCESSING
- X-Y Device Coordinate Data
- Testing Requirements
- Schematic Diagram
- Net List
- X-Y Test Proce Locations

Although hard copy data is acceptable for X-Y coordinate and net list, CAD information supplied on disk media is preferred.

EVALUATING THE SMT PC BOARD QUALITY
A solder sample is selected from each board lot or specific date code. The circuit substrate is compared to the fabrication detail and specified IPC quality level established. Following physical inspection, solder paste is applied to the SMD land patterns of the sample. The non-populated substrate is processed to reflow the solder paste and if organic flux is used, aqueous cleaning typically removes residue. The reflow solder quality will be evaluated as well as the substrates physical reaction to the temperature cycles of the reflow systems. A similar test is performed using the wave solder process.

FINE PITCH AND uBGA TECHNOLOGY ISSUES
Fine Pitch and uBGA assembly represents an understandably advanced packaging and manufacturing concept. Component density and complexity is far greater than many commercial products and if assembled in high volume, several issues must be addressed before an automated process can be developed. For example, the Fine Pitch components having
a lead spacing of 0.65mm (0.25") or less are adapted to both standard and custom application specific integrated circuits (ASIC). Industry standards for the Fine Pitch family of devices have extremely broad mechanical tolerance that must be considered when developing the land pattern geometry and spacing typical of that defined in Figure 1.

![Diagram of land pattern geometry on Fine Pitch devices showing least material condition and maximum material condition.

Figure 1. Land pattern geometry on Fine Pitch devices should allow for both Least Material Condition and Maximum Material Condition.

Because the tolerances will vary a great deal between suppliers and although one may mathematically develop a geometry suitable for attachment of the Fine Pitch device, land patterns must often be tailored or refined before efficient assembly process yields are achieved.

Ball Grid Array devices in comparison, are dimensioned without MMC/LMC factors associated with formed lead configurations.

The Ball Grid Array (BGA) and Micro Ball Grid Array (uBGA) family of products on the other hand have proved to be far more efficient as far as assembly process yield. Although the array devices are not as widely used as the fine pitch configuration at the time of this writing, the BGA and uBGA packages have closely defined physical attributes and uniform land pattern conventions.

USE PROVEN SMT LAND PATTERN GEOMETRY

Land pattern sizes and spacing generally follow recommendations furnished in IPC-SM-782A. Geometry of specific land patterns may deviate from those shown in the IPC document however, to meet specific process requirements. Land pattern length for wave solder processing for example, may be extended by an additional 2.5mm (.01") from the lead or contact end to provide exposure to flux and solder. Devices that are consistently supplied at either extreme of the established tolerance limits (LMC or MMC) may also need an adjustment to recommended land pattern geometry.

CONSISTENT ORIENTATION OF DEVICES

Although consistent orientation of devices on the PC Board is not mandatory, uniform direction of similar device types can improve assembly and inspection efficiency. For assemblies having mixed technology, leaded devices attached in a common orientation reduces assembly time because the placement head is generally in a fixed position and the board must be rotated. (surface mount assembly systems on the other hand, can rotate the devices before placement). Consistent SMT device orientation, although preferred, is not a factor for reflow solder processing but if the devices are attached using a wave solder process, device placement should be consistent and the direction of the device adjusted to maximize exposure to the wave.

POLARIZED DEVICES IN ONE DIRECTION

The direction of the polarized device, diodes, tantalum capacitors and even ICs, may be dictated by the function of the circuit. Process engineers recognize that performance of the circuit takes priority over assembly efficiency but, common polarity of device types or families adds to the overall producability of the SMT assembly. When a common polarity or direction of device families can be achieved, machine programming is simplified and fewer errors will occur during assembly. In addition, visual or automated inspection is more efficient and overall process yield is generally better.

UNIFORM AND ADEQUATE DEVICE CLEARANCE

Automated surface mount device placement is very accurate but designers attempting to maximize component density may not be aware of all manufacturing complexities. In order to maximize process yield and assembly efficiency, recognize the requirements of specific soldering processes, inspection criteria and repair techniques. Tall components that are too close to a fine pitch device will restrict the angle of view needed to inspect the solder joint and access by rework or repair tools will also be hampered. Wave soldering is common for the lower profile chip devices, diodes and transistor packages and small outline IC (SO IC) devices can be wave soldered as well but some packages may not withstand direct exposure to the molten solder. To ensure consistent attachment quality, space between devices must allow for uniform exposure to the solder. To ensure that solder contacts all termination points on devices during wave soldering for example, taller components must be spaced away from the low profile device to prevent shadowing.

SMT DEVICES USE STANDARD CONFIGURATIONS

Standards have been developed by the national and international electronics industry associations for most
surface mount devices. When possible, select device packaging controlled by these standards. This will help the designer in maintaining a uniform land pattern library in the CAD system and process engineers will have more control over the assembly processes. The designer may find that standards for components have been developed in other countries and although similar in appearance, differ to a degree from devices developed domestically.

As an example, small outline devices supplied from European and North American companies meet EIA/JEDEC standards while Japanese manufacturers may adhere to EIAJ furnished specification. In selecting the device package from multinational suppliers use a degree of caution. Because of the somewhat liberal tolerances of the EIAJ standards, the designer cannot assume that the physical dimensions of the devices are consistent between one manufacturer and another.

Products submitted for standardization by the JEDEC members today must meet internationally recognized dimensioning guidelines. All components must be dimensioned using the metric system. Any device submitted for consideration in "inches" will be rejected. Because standards are developed using only metric factors, device packaging standards developed for fine pitch and ball grid array are far more uniform.

COMPONENT PARTS HAVE MULTIPLE SOURCES
Discrete passive and generic active devices are available from several sources. Although single source devices may be necessary for specialized functions, two or more suppliers should be qualified for other devices when possible. It is not uncommon for a company to select three alternative sources for devices and typically one or two are considered primary sources and a third as a backup. Having multiple sources will avoid the inconvenience of shortages due to the industry's difficulty in forecasting supply and demand. Of equal significance to those attempting to control manufacturing costs, single sourcing does not allow any leverage for the buyer when negotiating price.

DESIGNED FOR EFFICIENT SMT PROCESSING
Assembly processing of the board can be relatively simple or, depending on the component types and density, more complex. The complex design however, can be efficient to manufacture and the less complex made difficult if the designer does not understand the requirements of each assembly process step. Assembly planning should take place during the preliminary phase of the design layout. Often, by adjustment of a components location or orientation and polarity direction on the PC board, manufacturability can be enhanced.

When the PC Board is small, irregular in shape or devices are very close to the board edge, panel array recommendations can be considered for a uniform panel array format.

DESIGN FOR TEST AND REPAIR
The detection of assembly process or device defects with bench top analyzing equipment is time consuming and may add significant costs to the product. Whether manual or automated, a test strategy should be defined before the PC Board design is started. If the test method selected uses automated In-circuit Test (ICT) for example, probe access must be available at specific common connecting circuit points. Though most component malfunctions may be detected through in-circuit and diagnostic capability built into a functional test system, there is considerable concern that specific solder process defects will be difficult to identify.

Test systems can be programmed to automatically measure the function of each device on the completed assembly. The automated system can also detect and locate improperly placed or damaged components and identify solder process defects. Process defects include both bridging of solder between the leads of devices and open connections between the device lead and the board's land pattern.

The in-circuit test systems are fixtureed and programmed specifically for each assembly type and when the board has been designed for testability the system will efficiently detect both component failure and assembly process (solder) defects. Figure 2 illustrates a solder bridge defect that may be identified with visual inspection however, insufficient solder or a very small alloy bridge on the fine pitch devices may escape detection unless electrical testing methods are employed.

![Figure 2](image)

Figure 2. Solder defects may be detected visually however, in-circuit electrical tests is a more reliable method of monitoring assembly process defects.

TESTING HIGH DENSITY PC BOARD ASSEMBLIES
Because the component density may be equal on both primary and secondary sides of the assembly, conventional electrical testing for process monitoring may not seem practical or possible. The small via pads typical on the high density fine pitch or uBGA PC board can be utilized for test probe access however, test specialist generally request enlargement of specific pads (see Figure 3) needed for probe contact.
products adds a unique level of difficulty to the assembly process (as well as test and inspection).

Recognizing that Fine Pitch/μBGA design is a more complex assembly than the average surface mount product, assembly process refinement may be considered to ensure manufacturing efficiency and yield.

As complexity of assembly processing increases the cost of assembly increases. For example, before locating fine pitch, ball grid array or die size Micro BGA devices on both primary and secondary sides of the board, the designer should understand the associated difficulty factor for both design layout and assembly processing. Other issues to be considered are the unique attachment process methods required for other device technologies. PC board assemblies are not always exclusively surface mount and often, a mix of leaded pin-in-hole (PIH) components are included in the design. In an automated in-line assembly operation, surface mount devices are generally (but not exclusively) attached with a reflow solder process.

The most efficient method of processing an assembly with both SMT and PIH device technologies may include reflow and wave solder. When both reflow and wave processes are employed, leaded PIH devices are installed during the final assembly operations. That is, termination of leaded devices is most often fulfilled following the reflow soldering of surface mount devices using a wave or other solder process.

SOLDER ATTACHMENT
Although other attachment materials are available for assembly of electronic products, solder alloy attachment of devices is most common method in use. Reflow soldering is a process that uses a tin/lead alloy supplied in a paste like form. The paste material converts to a liquid when exposed to temperatures exceeding 190°C. The reflow solder process uses a non contact heat transfer technology, typically infrared, forced convection (hot air or gas) or vapor phase. As noted, wave solder can be used to attach both leaded and selected surface mount devices but surface mount devices exposed to the molten solder must be attached to the boards surface with an epoxy before soldering.

After reviewing the device types selected, their location and the general complexity of the assembly, process engineers will develop a detailed manufacturing plan. The plan will identify the most cost effective methods for assembly and include the solder attachment processes to be employed. One of the following in-line solder process options may be considered:

SOLDER PROCESS OPTIONS
○ Reflow Solder
○ Double Reflow Solder
o Reflow/Wave Solder
o Double Reflow/Wave Solder
o Double Reflow/Selective Wave
o Reflow Solder w/ Ruppert Process

The reflow/wave and double reflow/wave solder process requires epoxy attachment of all surface mount devices on the secondary side of the board (devices exposed to the molten solder). The designer should use caution when considering wave solder for active device attachment because many surface mount component types (lead, Pin Pitch and Ball Grid Array or uBGA devices for example) are not suitable for wave solder.

CONSIDERATIONS FOR SELECTIVE WAVE SOLDER
Selective wave solder process uses a pallet fixture that masks the previously reflow soldered devices from exposure to the molten material. The selective wave solder fixture is designed to secure the assembly and allow solder contact at specific locations.

When selective wave solder follows a double reflow solder process, specific clearances are defined between surface attached devices and the leads exposed to the wave solder. If devices previously attached during the reflow process can not be shielded from a secondary exposure to the wave solder sequence, epoxy must be dispensed under the exposed part before the reflow solder operation. In this way, the surface mount parts will stay in position although the attachment solder is returned to liquid when exposed to the wave.

To avoid the use of adhesive, physical clearance restrictions between the surface attached device and PIH device lead must be considered, allowing unrestricted exposure to the wave solder. Also, to avoid excessive fixture thickness, higher profile surface mount components, those with an overall height greater than 3.0mm (.125"), should be moved to the primary surface of the board.

REFLOW SOLDER OF PIH DEVICES
The Ruppert Process allows the manufacturing engineer a method for simultaneously reflow soldering surface mount and leaded PIH devices. In this process, a calculated volume of solder paste is deposited in a pattern around each lead hole and pad feature. As the solder converts to liquid, the alloy flows to the lead, filling the hole and furnishing a very consistent solder joint. When adapting this process, components must be selected that can physically withstand the temperature of reflow soldering.

MANUFACTURING PROCESS INSTRUCTIONS (MPI)
Because detail drawings are often large and awkward to handle on the production floor, process engineering will typically prepare unique instructions for each phase of the assembly operation. The preparation of a detailed Manufacturing Process Instruction (MPI) document and the use of specific fixture technology, both production yield and cost objectives can be met. The MPI can be developed for production floor use as hard copy instructions or distributed electronically. Because copy machines are so common in business environments, timely implementation of changes and retrieving or replacing all obsolete (or down rev) hard copy from a large production operation can be difficult. Adding an expiration date or time to all documents on the production floor is recommended. Electronic distribution of documentation has proven to be an advantage over hard copy when rapid response to engineering change (EC) is critical.

PANELIZATION FOR MACHINE TRANSFER
PC Board shape and size will impact both fabrication cost and assembly efficiency. In order to automate the transfer of a board from one assembly station to another, provisions can be made to accommodate conveyer systems. Small or odd shaped boards for example, are more efficiently processed in a panel array. These individual assemblies can be retained in an efficient panel array format and after all the assembly process steps are concluded, excised by hand or machine (see Figure 4).

Figure 4. Small and/or irregular shaped PC Boards are furnished in a uniform panel format for efficient handling during assembly automation processes. The individual assembly units are separated following soldering and cleaning operations.

Panelization can apply to larger boards as well. Even though the board outline specified for the finished assembly is an
irregular shape, additional board material can be retained to furnish at least two uniform parallel sides.

**PCB MATERIAL PLANNING**
Panel size limits must also be considered. To control the cost of the bare board the designer must attempt to maximize material usage yield the highest possible quantity of finished boards from a standard panel blank. As an example, 18" x 24" panel blanks typical of that shown in Figure 5 are common for domestic multilayer PCB suppliers.

![Panel Diagram](image)

**Figure 5.** When developing the panel array, maximum utilization of the fabrication process panel will avoid or reduce excessive waste of PC board material.

Other panel sizes are available but the 18" x 24" panel size is most common due to the laminating press design. The actual usable area for the 18" x 24" size noted may be only 16" x 22" depending on boarder areas reserved for alignment pins and test coupons. Assembly machines have panel size restrictions as well. Some models of Panasonic and Fuji assembly systems, for example, can only accommodate a panel size of 14" x 18" while other systems may accept a panel measuring 18" x 20" or more.

**ASSEMBLY EQUIPMENT (PCB SIZE) LIMITATIONS**
When the SMT product requires large finished board sizes, the designer will need to know the assembly equipment limitations before starting CAD design. In addition to panel size limits and specific tooling hole requirements there are other physical restrictions or features that must be considered during the design phase of a program. The conveyer transfer mechanism on stencil machines, dispensing systems and placement equipment requires a minimum clearance from board edge to component body or land pattern of 3.1 mm (.125"). Tooling hole size and location will also vary somewhat between assembly systems. The Fuji and Panasonic systems, for example, specify two non-plated tooling notes on a line parallel to the long edge of the board.

The holes are positioned 5.0 mm (.200") from the board edge and an equal dimension from each end.

The more sophisticated assembly machines use automated vision systems for precise alignment adjustment for both solder paste application and device placement. To accommodate the vision features, the designer must provide fiducial targets on the board surface. The fiducial target is etched into the board to minimize dimensional tolerance accumulation to the land pattern geometry provided for device attachment. Three global fiducial targets are required for each board side having surface mount devices. Two addition fiducial targets for each fine pitch device is requested as well. The standard (minimum) size of the target is 1.0 mm (.040") diameter with a clearance of 0.25-0.50 mm, void of solder mask and other physical features (see Figure 6).

![Fiducial Targets](image)

**Figure 6.** To accommodate the vision alignment systems on surface mount assembly equipment, each board or panel must include three global fiducial targets (and two fiducial patterns for each fine pitch device).

The standard fiducial is a solid filled etched copper circle .040" (1.0 mm) in diameter. A clear zone must be provided around the fiducial diameter and devoid of any other circuit features as well as solder mask material.

**DOCUMENTATION FOR FIXTURE DEVELOPMENT**
Development of PCB assembly fixtures requires detailed instructions as well as CAD data. Before releasing the product to assembly, documentation must be complete and accurate. The Gerber or IPC-D-350 data generated to fabricate the PC Board can be used to assist in assembly machine programming, development of solder stencils and other assembly and test fixtures. Even though each assembly system may use incompatible software, equipment companies or system specialists have developed the conversion or translation software features to adapt the standard CAD data into a compatible format.
MANUFACTURING USE OF CAD DATA
- Assembly Machine Programming
- Solder Stencil Development
- Vacuum Fixture Preparation
- Wave Solder Fixtures
- Test Fixture Engineering

Process development for surface mount, fine pitch and ball grid array or Micro BGA assembly is not routine. That is, from experience, engineers may often adapt several process proven methods for soldering the various devices to the substrate.

USING CAD DATA FOR AUTOMATED ASSEMBLY
As the complexity of electronic products has increased it is apparent the industry must utilize the efficiency of assembly automation as effectively as possible, especially for the assembly of PC Boards. Driven by the competitive demands to meet higher performance or a reduced size requirement for electronic products, engineers and designers must often adapt several assembly methods.

Direct transfer of CAD data into automated assembly systems will dramatically accelerate production set-up and reduce overall assembly system programming time.

ESTABLISHING A COMPONENT DATABASE
With the increased usage of surface mount for PC board based products, the design and materials specified for the board must be matched to diverse component and assembly process technologies.

Prior to designing the PC Board in the CAD system, each component is constructed in digital form creating an electronic data base. The CAD data is most often used to prepare photo-tool artwork, PCB fabrication details and assembly instructions but when prepared in the correct format, it can used for assembly set-up.

When the CAD data base is formatted correctly, specific physical data for each device can be adapted to program the machine for component placement (X-Y coordinate position) and orientation. To facilitate the X-Y coordinate information, a datum position must be established on the board surface. The recommended datum "0" for X and Y coordinates is (ideally) one of the global fiducial targets at the lower left or upper right corner of the board or panel.

Component packaging can be dissimilar between device families because of differences in shape and size. Surface mount devices for example, are furnished in standard tape and reel formats as well as tube magazine feeders. To accommodate automated assembly of fine pitch devices, tray carriers are most often adapted.

Note: Each surface mount devices is located using the body center and a basic orientation for reference ("0" degree is the basic orientation of the device).

Orientation as well as polarity of a device must be defined in the CAD data base. When developing this format, the device location coordinates can be transferred to the assembly systems quickly. Resistors and capacitor devices as an example, have a common orientation but no defined polarity. As the designer develops the component data base, numbers are generally assigned to each end of the device to accommodate circuit routing and maintain orientation or polarity.

Tantalum capacitors, diodes, ICs and other polarized components have a unique orientation in relation to tape feed systems. In all cases, keep in mind the relationship of the device orientation within the tape cavity and its relationship to the perforation at the tape carrier material edge.

TAPE AND REEL PACKAGING
Each device family or package type has a standard orientation in relation to the perforated indexing pattern at the tape edge. Rotational data must be specified from the "0" position in a counterclockwise direction (typically 90 - 180 - 270). The "0" starting position of the component is significant (see Figure 7). Tape and reel packaged devices for example, have an established standard for orientation related to the perforated pattern of the tape. The standard orientation does vary however, between unique device families.

![Standard Device Packaging Orientation](image)

Figure 7. Passive and active devices are supplied in a tape and reel format, held and protected within an embossed pocket.

Devices supplied in tube magazine carriers and flat tray carriers will not always be consistent with the tape and reel packaging system. For device types supplied in either of these package configurations, machine programmers recommend that the designer maintain the orientation established for the tape and reel packaged component as illustrated in Figure 8.
Figure 8. The rotational origin of tape-and-reel as well as tray packaged devices is significant when developing the component data base file in the CAD system.

Surface mount devices packaged in flat pack tray carriers are usually not suited for tape and reel and except for the odd configurations (transformers, multichip modules, connectors) most devices furnished in the tray format are the more delicate fine pitch product. The partitioned tray is specifically designed to restrict movement of the devices in transit and to protect the delicate leads from deforming.

DOCUMENTATION REQUIREMENTS

As part of the manufacturing planning cycle a task group is assembled to evaluate the manufacturing efficiency for each surface mount product. The review committee may include representatives from design, test, manufacturing engineering, quality and materials, each having specific responsibilities.

The following documentation must be prepared and furnished to manufacturing in order to plan material requirements, plan assembly processes, develop fixtureing, program assembly systems and prepare for assembly test.

1) Assembly Documentation: Assembly details for circuit boards must define the location and orientation of all component parts. When practical, include the component outline with reference designation. The graphics must define the polarity for diodes and tantalum capacitors as well. The physical position for all devices must be referenced to the “0 datum” (fiducial) location. Assembly drawings must include detail for connectors, hardware as well as special instructions needed to complete the assembly. Also reference industry standards and quality level that would apply to the finished product. The assembly detail must furnish enough information for processing and inspection of the final configuration.

2) Material Requirements: Material for each assembly is defined in a formal Bill of Material (BOM). The BOM includes a part number, quantity required, device description, value, type or size and reference designer. If a manufacturer’s part number is not supplied on the BOM, then a second list must be prepared that defines the approved vendor list (AVL). The AVL defines all approved or alternate sources and unique manufacturers part number used to order the devices.

3) Bare Board Specifications: The PC Board fabrication detail must define all physical attributes including tooling hole locations and size. Information supplied generally includes base material description and thickness, layer sequence, solder mask type and plating, application industry (IPC) standards. If boards are supplied in a panel format (one or more units in a single panel), dimensional coordinates for each board unit is to be referenced.

4) Machine Program Data: To facilitate automated machine programming the position data for each surface mount device is furnished in hard copy format (see Figure 9) or disk file. The data defines the part number, reference designator and X-Y coordinate location and orientation for each device on the assembly. Data for machine programming can be developed by other methods but the manual programming process may require one or two additional days to complete and verify accuracy.

<table>
<thead>
<tr>
<th>Device Ref.Dess.</th>
<th>Part Number</th>
<th>Location</th>
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<th>Y</th>
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<td>2115</td>
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</table>

![Figure 9. Data output from the CAD system is a useful tool in the programming of surface mount assembly machines. The example shown defines each components part number, X-Y location on the PC Board, orientation and device type.](image)

5) CAD Data File: The preparation of solder paste stencils and other fixtures requires a disk copy of the IPC-D-350 or Gerber data and aperture list developed for fabricating the PC Board. Manufacturing engineers for example use the solder paste layer(s) of the file to prepare stencil fixtures. To regulate or control solder paste volume of specific device types, the assembly process engineer may modify the land pattern stencil opening geometry. When stencils systems are equipped with vision assisted alignment, the global fiducial target images furnished on the PC board for automated component placement may also be merged onto the stencil pattern (especially when fine pitch devices are in use).
Process development for surface mount assembly is not routine. That is, from experience, engineers may adapt several process proven methods for soldering the various devices to the substrate. Because each assembly will have its own character, process engineering will include the development of a detailed Manufacturing Process Instruction (MPI) document and unique fixture development.

**Documentation and CAD Data Check List**
- Bill of Material (BOM)
- Approved Vendor List (AVL)
- Assembly Detail
- Special Assembly Instructions
- PCB Fabrication Detail
- Gerber Data File (on disk)
- X-Y Device Coordinate Data (on disk)
- Testing Requirements
- Schematic Diagram
- Net List (on disk)

**ASSEMBLY PROCESS REFINEMENT**

Assembly process refinement for SMT includes extensive monitoring through both manual and automated visual inspection following each machine operation. As an example, a measurement of solder paste volume with a laser scanning microscope on each board is recommended followed by additional periodic sampling of the product during other stages of the assembly sequence. After attachment and reflow soldering of surface mount devices on a sample lot, quality and engineering specialists inspect the solder fillet on each component contact site. During this review process each team member studies the alignment of the passive components and the finished registration of multiple lead IC devices. Additional evaluations are made following wave solder processing to measure uniformity and identify bridging potential to adjacent leads or devices.

**GENERAL DESIGN CONSIDERATIONS**

The fundamental elements of good design practice assessed during the design review are noted in the following:
- Use proven SMT land pattern geometry.
- Consistent orientation of devices.
- Polarized devices in one direction.
- Uniform device clearance and distribution.
- SMT devices use standard configurations.
- Component parts have multiple sources.
- PCB designed for efficient SMT processing.
- The SMT assembly is testable from one side.

* Land pattern sizes and spacing recommended generally follows those illustrated in IPC-SM-782A.

**VERIFICATION FOR TESTABILITY**

The test strategy must be defined before the PCB Board design is started. If the test method selected uses automated in-circuit test, then probe access must be available at specific common connecting circuit points. If test probe contact patterns are not accessible at each common junction of the circuit network then measuring or exercising the components (individually) during the test is not possible. The detection of assembly process or device defects with bench top analyzing equipment is difficult and adds significant costs to the assembly. If the design does not furnish test sites at each "net", reliable and consistent electrical testing may be compromised.

The in-circuit test systems are fixtured and programmed specifically for each assembly type and when the board has been designed for testability the system will efficiently detect both process (solder) defects, workmanship quality problems and component failures. Even though most component malfunctions may be detected through in-circuit and diagnostic capability built into a functional test system, there is considerable concern that specific solder process defects will be difficult to identify. Test systems are programmed to automatically measure the function of each device on the completed assembly.

The automated system can detect and locate improperly placed or damaged components and identify solder process defects.

The process defects include both bridging of solder between the leads of devices and open connections between the device lead and the board's land pattern.

**CONCLUSION**

The component and circuit routing density factor on the high performance products adds a unique level of difficulty to the PC board fabrication assembly process, test as well as inspection. Recognizing that Fine Pitch, Ball Grid Array and Micro BGA design is a more complex assembly than the average surface mount product, alternative assembly process and test methods may be considered to ensure manufacturing efficiency and yield. Because the component density may be equal on both primary and secondary sides of the assembly, conventional electrical testing for process monitoring may not be capable of detecting all process defects. Surface Mount assemblies, especially those with higher device complexity, require continuous process monitoring and methodical inspection.

With thorough planning and a clear understanding of assembly process steps and machine requirements, the designer will have enhanced capability to prepare a process compatible product. Providing a good design with complete and legible documentation and CAD data in the format detailed will help to ensure that the assembly meets the expectations of high quality, performance, reliability and cost targets established.
INTRODUCTION
With the explosion of surface mount technology and the continuing strides in advanced packaging such as ball grid arrays, multi-chip modules, tape automated bonding, and chip on board, the electronics industry continues to push the limits of component and printed circuit assembly (PCA) densities (see Figure 1). Moore's Law [1] predicts that semiconductor densities will continue to double approximately every 2 years. This ramp up in densities adds complexity to new designs and usually imposes restrictions on testing.

Figure 1. Advances in surface mount packaging continue to push the limits of component and board densities.

Design for test [2] (DFT) is needed now more than it ever was. Test engineers are faced with optimizing fault coverage on the most dense and complex devices that have ever been manufactured while test access continues to be traded off. In addition, the demands of short times to market and the pressure of maintaining or achieving acceptable levels of testing costs create major challenges for test organizations. If a company is to remain or become effective at ensuring quality and controlling costs, a design for test process must be used and designs need to be made testable. Embracing DFT will reduce both the recurring and non-recurring cost of test, reduce the overall product development cycle, improve quality, and improve communication between various groups.

The purpose of this document is to: provide a high level understanding of a DFT process methodology; highlight some of the major issues that affect DFT, test strategy development, and the cost of test; and furnish a general set of guidelines that can be used in design-for-test practices.

THE DESIGN FOR TEST PROCESS
What Is "Design For Test"?
DFT is a process used by companies to achieve the goals of ensuring that new designs are testable and product test costs are minimized. For practical reasons this paper will mainly focus on DFT for printed circuit assemblies. However, DFT can be practiced at all product levels that require test, from the device level all the way up to the final system level.

A simplistic view of the DFT process has 4 major serial steps:

1) Collect Data/Identify Issues
2) Generate Possible Solutions
3) Examine the Tradeoffs
4) Choose a Solution

1) The collection of data becomes the foundation for this four-step DFT process. The data consists of schematics, bill of materials, performance requirements, test specifications, cost targets, electrical and physical constraints, and much more.

2) The test experts will process this myriad of information and begin to formulate an understanding of the impact on testability and test costs. As test issues are identified and understood, a number of possible solutions can be generated.

3) Each possible solution will present its own set of tradeoffs. The impact of test issues such as fault coverage, diagnostic ability, throughput, and test cost must certainly be considered, but one must also take a
360 degree view and consider the impact on things like time to market and overall product cost, not just test impact alone. Gains in one area can result in losses in another.

4) Once the tradeoffs are weighed, the best solution is chosen. The best solution will be the one that yields the greater benefit for the company rather than a particular group and minimize the overall cost of the product that will be incurred throughout the life of the product (more on this later).

Take this for example: A particular circuit in the design requires an electrical adjustment to be made on every individual assembly. Some possible solutions could include:
1) Re-design the circuit using tighter tolerance components to eliminate the need for adjustment.
2) Add more circuitry to the design so the adjustment can be done automatically in the system by software.
3) Add a test process step to perform the manual adjustment.

Solution number one will result in a higher material cost, but a lower production cost due to the elimination of the adjustment. Solution number two results in a higher cost for both material and additional software development, but also a lower production cost. Solution number three results in an even lower material cost but adds production test cost associated with an added process step to perform and test the adjustment. As you can see, each solution presents its own set of tradeoffs. The impact of these tradeoffs must be completely understood before a final solution is reached. Some issues identified during this process will require little effort to choose a solution and others will require an in depth analysis such as the previous example.

The 4-step DFT process may occur in iterations. During the course of design development, the initial data or information will get modified or new data will become available. As a result, new issues may arise or existing issues may present themselves with a different set of tradeoffs. The process can be used again and again until the data remains stable and all issues are resolved.

When Should DFT Occur?
The DFT process should take place as early in the process as possible, even prior to the design phase. It is estimated that as much as 60% of the total cost of a product is committed in the conceptual phase before the design phase actually starts [3]. Also, because of today’s critical time to market demands, design engineers are on extremely aggressive schedules. Making modifications to the design because of testability reasons can add design time and disrupt engineering schedules. The later in the process that DFT starts, the less likely a design change can be made and opportunity is lost.

As mentioned earlier, the foundation for performing DFT is collecting data. The DFT process can start as soon as useful information on the design becomes available. The design phase is only one step of an entire product development process. An example of the front end of a product development process is shown in figure 2.

Although the majority of detailed information such as schematics, bill of materials, drawings, etc. will become available in the design phase, higher level information will be available in the phases prior to the design phase. Information such as preliminary specifications, the

<table>
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<tr>
<th>Conception/ Project Definition</th>
<th>Design</th>
<th>Design Implementation</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start DFT Process</td>
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Figure 2. The DFT process can begin as soon as design information is available.

presence or absence of application-specific integrated circuits (ASIC) DFT (i.e. 1149.1 boundary scan [4] or built in self test), or general design descriptions are extremely useful to know about in advance. This high level information can be used in framing test strategies early or identifying potential capital equipment needs.

How Should DFT Be Implemented?
As mentioned earlier, one of the more important aspects of DFT is acquiring current information relative to the design. The design phase itself is extremely dynamic. As designs evolve, especially during the early stages of the design phase, they are constantly subject to modifications. Specifications can change, new functions can be added, circuitry can be added or removed. If the development of the design is left unchecked, testability can be compromised. It is necessary to establish continuous communication with the design groups.

Concurrent engineering [5] and concurrent engineering teams are the best way to open and maintain lines of communication and keep information flowing. Concurrent engineering teams are made up of representatives from various groups in the company who provide input to the design. Team membership can include representatives from design, manufacturing, test, marketing, artwork, purchasing, operations and service groups. The team will meet on a regular basis and the frequency of the team meetings will be determined as needed by the team. In addition to the regular meetings there should be periodic major checkpoints or reviews.
that occur. A test engineer with good technical and communication skills should be designated as the test representative who will provide input toward making the design testable.

The process of DFT also needs to be complemented by a set of design for test guidelines that are updated on a regular basis. The guidelines serve as a primary vehicle for communicating test capabilities and constraints while also containing recommended design for test methods.

**TEST STRATEGY**

**Test Strategy Overview**

Test strategy is the choice of one or more available test methods to provide the highest amount of fault coverage. The ideal test strategy will detect all possible faults as early as possible in the test process, use the smallest possible number of discrete test steps, and use the least expensive means possible.

If a product is designed to be as testable as possible, then the test strategy must be defined early in the design phase. In this manner, the selection of available DFT techniques can be optimized for the chosen test strategy, and tradeoff decisions can be made on the basis of the capabilities and limitations of the selected test strategy. The development of a test strategy should be considered an element of the DFT process and should occur early in the design phase.

**Considerations in Developing the Test strategy**

There is but one consideration in developing a test strategy: to support and further the company’s business objectives for the product as effectively as possible. Selection of a test strategy begins with a few questions:

1. **How good must the product be?** Given that a certain level of product quality must be assured, what is the minimum level of testing that guarantees that this quality level is consistently attained? Or, if applicable, are all contractually obligated provisions fulfilled with the proposed tests?

2. **How many units must be tested, and at what rate?** In general, high volumes imply fully automated test methods, and low volumes imply manual or semi-automated methods. The rate at which units must be tested and shipped has implications for the choice of test strategy; generally, high volumes dictate short test times, and low volumes tend to result in longer test times.

3. **How much money is available for test activities?** Obviously, we do not imply that the goal of testing is to exhaust all available funding; rather, we do say that there must be adequate funding available for whatever tests are proposed.

4. **When must the tests be available?** Given that different test methods have different test development times, will the proposed tests be completed in time for the scheduled introduction of the product?

5. **What are the product cost targets?** In other words, do the proposed tests fit within the established cost targets for the product throughout its life cycle? It is widely observed that the price of an electronic product will decline over time; many producers establish cost reduction targets over the life of a product to maintain competitiveness, market share and satisfactory profit margins.

The goals of any test strategy are implicit in these questions:

- Consistently assures the highest level of product quality;
- Supports the required throughput rates over the product life cycle;
- Can be carried out within budget and meet schedule requirements;
- Provides the lowest initial cost contribution and is capable of providing on-going cost reductions.

Considering each of these goals individually, let us examine the methods and techniques of achieving each goal.

**Quality:** From a test point of view, a quality product is a defect-free product. All test activities must provide assurance that the product is free of defects. The greatest assurance of quality arises from the highest levels of fault detection, and so a complete test strategy must be structured to provide the highest possible fault detection.

A test strategy will consist of a final test which is necessary to demonstrate the product can do what is supposed to and is most likely performed inside the final system or product. The fault coverage at this test stage is very high since the products functions are being tested at the speed in which it was intended to operate. However, final test usually offers poor or unacceptable levels of diagnostic capability. The detection and fast diagnosis of faults needs to be done at a test step that is more efficient thus more cost effective at detecting and diagnosing faults other than at final test. Various test platforms and test techniques are available that offer a wide range of fault detection and diagnostic capability.

The challenge in architechting a test strategy to achieve quality goals is to allocate as much fault detection and diagnostics as possible to one or more test steps which are executed before the final test.
Throughput: One might consider go/no-go test time as the benchmark of throughput, but this does not give the complete picture. Generally, failing printed circuit assemblies must be diagnosed and repaired (not scrapped), and so the ability to meet throughput must consider both raw test time and the time required to diagnose, repair, and re-test any failures. With this in mind, two important factors are apparent:

1. In a multi-stage test process, achieving high yields is crucial to satisfying throughput requirements. In particular, one must pay great attention to yield at the next stage of test, not just yield at this stage of test; it is a false economy to save test time at an earlier stage (by sacrificing fault detection) and deferring those tests to a later stage.

2. If the yield were 100% (that is, there were no failures), the time to diagnose, repair and re-test would be zero. Therefore, there are great potential savings to be had from preventing defects, even though one must still test to ensure that those defects are not present.

The challenge in architecting a test strategy to achieve throughput goals is to detect and diagnose faults as early as possible in the preliminary test steps; but even better, the test strategy should strive to help prevent defects from ever occurring.

Budget and Schedule: Here, we refer to budget and schedule for developing the test strategy itself. The big ticket budget items will undoubtedly be capital equipment (test systems and fixtures) and test development labor. The big schedule items will be equipment lead times (if new systems must be made or bought) and test programming times. In these areas, the ability to achieve satisfactory design for testability can save time and money. For example, the right amount of DFT may allow use of existing test systems, thereby precluding the need to invest in new test systems. Or, on the labor side, the right amount of DFT may allow direct use of canned tests in an in-circuit test library rather than custom tests unique to that application.

The challenge in architecting a test strategy to achieve budget and schedule goals is to make the widest possible use of test resources already on hand (both test equipment and test software).

Cost: Here, we refer to the test costs which will be incurred in carrying out the test strategy. For the most part, these will be recurring costs; test execution costs, diagnostic and repair costs, equipment maintenance costs and personnel training costs. As we said, the goal of the test strategy is to provide the lowest possible costs at the outset with provisions for systemic cost reductions over time.

Typical Test Strategy
In contemplating a test strategy, one is faced with numerous tradeoff decisions, instances where one can sacrifice one item to achieve a benefit in another item. It is not possible to provide absolute rules which are applicable in all circumstances; nevertheless, it is possible to discuss some of the more common principles in test strategy and discuss the specifics of the trade items. We start with two fundamental assumptions:

1. There will be a final test step, which is optimized for go/no-go test and is the single test which determines whether or not the product can be delivered to customers.

2. Quality, in the sense with which we define it, is not a tradeoff item; rather, we look for opportunities to allocate fault detection and fault diagnosis to other (less costly) test steps than final test.

Under these assumptions, the test strategy will consist of multiple discrete test steps, since final test is likely optimized for go/no-go testing and falls short of the need for diagnosing faults. Therefore, the first tradeoff item will be to settle the number of test steps prior to final test. To determine this, one must understand two things; the fault spectrum and the capabilities of available test platforms (test methods).

The fault spectrum is the distribution of the different categories of defects that occur on a board, a group of boards, or an entire production process. Although there are many different types of faults that can occur on a PCA, most faults can fall in to one of two categories; construction faults or functional faults.

Construction faults are faults associated with the construction of the board such as solder shorts, missing components, or mis-inserted components. Functional faults are those faults that cause functional failures on the board and do not have any identifiable construction faults, such as defective or out of tolerance components.

Understanding or being able to predict your anticipated fault spectrum, along with understanding the fault detection and diagnostic capabilities of available test platforms will be key factors in determining the discrete test steps for the test strategy.

Although there are many variations of test systems and test platforms that provide different fault detection and diagnostic capabilities, the bed-of-nails based test and the edge connector based functional test are the 2 fundamental techniques for providing construction and functional fault coverage.
Bed-of-nails based test methods (manufacturing defect analyzer (MDA) and incircuit) provide good coverage of construction faults (shorts, opens, missing/wrong components) and extremely precise fault diagnosis, but poor coverage of functional faults (interaction faults and speed/timing faults). Bed-of-nails techniques also require physical access to all circuit nodes, and such access may not be available with surface mount designs. The addition of test pads and increased routing difficulty associated with dense surface mount designs pose real estate issues for the layout designer. One hundred percent (100%) nodal access is not always possible.

We note the increasing number of cases where, even with full access to all device nodes, the devices cannot be incircuit tested for technical performance reasons; say, the incircuit tester cannot apply patterns at rate high enough to keep the device alive, or the number of patterns required for the test exceed the limits of the tester's pin electronics.

We perceive an increasing importance of faults which simply cannot be detected by bed-of-nails testing, sometimes termed "soft faults". In such cases, a circuit may appear to work properly if tested at a slow speed, but fails when tested at its rated operating speed. Generally, there are two problems at work here: first, the bed-of-nails probes introduce parasitics which prevent the circuit from operating at rated speed; second, the tester itself will most often not be able to operate the circuit at rated speed. Although bed of nails test methods have true value in detecting and quickly diagnosing faults, alone it falls short of being the "one-stop" test solution.

Edge-connector based test methods (board functional test) provide good coverage of functional faults, but generally require the use of powerful (expensive) test systems and potentially long test development times to achieve their high levels of coverage. Functional test also does not provide the precise diagnostic resolution that a bed of nails test would provide.

We believe in typical situations, two test steps are necessary prior to final test: a bed of nails test (most likely incircuit) which detects all of the construction faults, followed by a board functional test which detects and diagnoses the functional faults.

Therefore, we believe that a "typical" test strategy will contain three steps:

1. The first step will be some type of bed-of-nails test, either MDA or incircuit, which rapidly detects and explicitly diagnoses construction faults and as many as possible of the functional faults;

2. The second step will be some type of edge-connector functional test which detects and diagnoses the faults which escaped from, or cannot be detected by, bed-of-nails test;

3. The third step will be the final test, the one which determines whether or not the product can be shipped to the user, and which is optimized for go/no-go testing as well as provide the highest possible fault coverage.

![A Typical Test Strategy](image)

**FIGURE 3.** A typical test strategy consists of incircuit test to detect construction faults, functional test to detect functional faults, and final test for product verification.

**Optimizing The Test Process**

In our experience, most companies find it prudent to introduce a new product with the three step test strategy described above. Bearing in mind our belief that ongoing cost reductions are desirable, let's examine opportunities for cost savings as the product and its manufacturing processes mature:

Ideally, construction faults should be detected and corrected at the construction stage, before (potentially!) large quantities of the units are incorrectly fabricated. It may be possible to use automated inspection systems (visual/infrared/x-ray) to detect such faults during fabrication.

It is worthwhile to examine faults which occur at functional test to determine if the faults could be detected at bed-of-nails test (by adding or modifying those tests to increase fault detection). The potential savings from this course of action arise from the differences in fault diagnosis between the two techniques. Generally, bed-of-nails tests report multiple faults in one pass through the tests, while functional tests report a single fault per pass.

If the product is so equipped, it may be possible to move non-test steps into the test process. For products which require programming of non-volatile memory devices, it may be possible to program these parts immediately after incircuit test passes, thereby saving additional handling steps.

It may be possible to move some functional test diagnostic coverage to the final test step. This is
particularly true of embedded system products, where the ability to download special test software (or to hook into operational firmware) may provide test capabilities at that step which eliminate the need to run the functional test, since the testing could be done as required at the final test step.

Depending on the degree of coverage, if a product uses the more invasive DFT techniques (such as boundary scan and built-in test), it may be possible to use un-powered MDA tests followed by functional test (which exercises the scan and BIT features) to achieve the same levels of coverage and diagnosis.

Therefore, we believe that it is most desirable to introduce a product with the three-stage test strategy, but that this should be done with the intention of eliminating the functional test step as soon as practical. This can be done by reallocation of fault coverages and diagnostics to the first and third steps as appropriate.

THE COST OF TEST

Test Cost Overview
The total production costs of an electronic product are divided into three major elements. The relentless advances in a wide range of technologies have profoundly affected the distribution of those costs:

1. Materials Costs: the costs of the individual components and packaging / interconnection parts. Materials costs tend to decrease over time, as advances in chip fabrication and packaging technologies allow increasing integration (higher numbers of circuit functions per unit area), lower cost per function, higher speed and lower power consumption;

2. Assembly Costs: the costs of fabricating (putting together) the product from its individual parts. Assembly costs tend to decrease, as the number of discrete components and interconnections decreases with higher levels of integration and greater use of automated assembly equipment.

3. Test Costs: the costs of testing the individual parts and all subsequent levels of assemblies (boards, modules, subsystems, systems). Test costs tend to decrease less rapidly, as the products become more complex (with more functions to be tested), and circuits become less accessible to direct physical access needed for conventional test methods.

Test costs can be expected to assume an increasing percentage of the total cost of producing an electronic product, and producers of electronic products must pay greater attention to bringing those costs down. Before discussing details of the cost of test, we point out two additional items:

- Products must be tested throughout their useful lifetime: any meaningful consideration of test cost must take this into account.

- Test should be seen as an investment, and not strictly as a cost. Properly designed and conducted test activities add value to the product for the producer and the user, by providing a measurable return on the money invested in having the test, cost savings, and avoidance of costs which would be incurred if the tests were not performed.

Elements Of Test Cost Affected By DFT
We would divide test costs into four major categories:

1. Test Equipment Costs. This includes the test instrumentation itself (whether commercially available test systems or discrete instruments), computers or other controllers, fixtureing and other hardware necessary, and the cost of maintaining the equipment;

2. Test Software Costs: This includes generating test patterns and other software needed for testing, verifying the test software (including simulation, analysis and debug), and the cost of maintaining the software;

3. Test Operations Costs: This includes the cost of the time spent using the test equipment (however that cost is calculated), and the cost of the labor of the persons performing the tests.

4. Diagnosis and Repair Costs: These costs could be included as test operations costs, but in our view, they should be considered separately.

Design for testability plays an important role in helping to reduce each of these elements of test cost:

- DFT helps to control test equipment costs by helping to squeeze more performance out of available test systems and by simplifying test fixtureing and other hardware requirements;

- DFT is especially helpful in controlling test software costs by allowing higher fault coverage tests to be developed in less time;

- DFT helps to control test operations costs by reducing the total test execution time;

- DFT is perhaps most helpful when it allows rapid and accurate diagnosis of failing tests.
LIFE CYCLE VIEW

Test is a value judgment; one examines whatever is being tested to confirm that it does what it was designed to do. With this in mind, it is clear that such value judgments will take place many times throughout the useful life of a product.

When the product is designed; this is design verification test. At the outset, it is not known if the design itself is good, nor is it known if the actual realization of the design is good. This type of testing can be quite involved, requiring much manual (labor intensive) work and analysis, and requires great flexibility in responding to the need for changes. Further, design verification test involves very small quantities of the product.

When the product is manufactured; this is production test. At the outset, the design is known to be good, the question is whether a particular instance of the design was fabricated correctly and performs all required functions correctly. This type of testing must handle high throughput.

While the product is in service; this is in-service test. This includes any tests done by the user (as part of maintenance or diagnostics) and any tests done by a representative of the producer (field service engineer). In general, this type of testing must focus on rapid diagnosis, so that the product can be quickly returned to service.

When the product, or a field replaceable part of it, is returned to the manufacturer, this is field repair (or depot) test. This type of testing can be extraordinarily high pressure: the customer is (or may be) down and there may be guaranteed turnaround times to be fulfilled. In addition, it sometimes happens that the failing conditions at the user's site cannot be duplicated in the field repair test, and a prudent producer would probably want to gather not only diagnostic information (What failed?) but also reliability and failure analysis information (Why did it fail?). The above facts lead us to several observations:

The responsibility for developing and carrying out the various tests cuts across organizational boundaries within a company, and even extends outside of the company. Consequently, there are numerous opportunities for duplication of efforts and hidden costs.

The methods and goals of each of the necessary test steps differ; one would expect design verification test to be more detailed (and time consuming) than tests which would be executed in the field.

The need for fault detection and diagnosis does not change across the various test steps; rather, the methods for obtaining high coverage differ.

Consideration of the cost of test must take into account all test activities, throughout the life cycle of the product. DFT activities must encompass this view, and attempt to provide benefits to all types of testing. In addition we see a natural hierarchy or leveraging of the total test effort; there is much to be gained by the ability to recycle specific tests across all test activities, to avoid redundant efforts and costs.

Test As An Investment

We would define an investment as spending money today in exchange for future benefits and advantages; therefore, we believe that the cost of test, when seen in this context, can be seen as an investment, rather than just a cost. In other words, since it is necessary to test, it is desirable to spend as little as possible on testing; this is sometimes known as just enough test. But, it is also necessary to spend wisely; the tests must meet all of the requirements discussed above.

It is also necessary to test throughout the product's life cycle, it is desirable to have tests available which meet the needs of all test activities. Further, by taking the large scale view, it is apparent that any costs associated with these tests can be spread across a larger base, which helps to reduce the overall costs of test.

Although this paper is specifically concerned with manufacturing issues, we believe that it is proper to take the large scale view of all test activities, since the benefits of investing in test, if done correctly, are available at all stages of test, and not just manufacturing-related test.

“Hidden” Test Costs

Of the four categories of test costs previously described, we believe that equipment, software and operations costs are fairly visible, in the sense that one may readily determine the time and money spent on those items. The diagnostics and repair costs are of a nature which makes them less visible at all stages of test.

During design verification test, the major hidden cost is likely the labor of the people conducting DVT. If the product is designed to be testable, this hidden cost can be reduced before any revenue is derived from sales of the product. An additional hidden cost is the opportunity cost of increasing the time required to bring the product to market, which translates into lost revenue and possible, lost market share.

During production test, diagnostics and repair costs are generally less visible than the other costs; these costs generally do not appear in capital equipment budgets or payroll time sheets or purchase orders, and may not be formally tracked by the usual accounting systems. First consider the cost of labor to diagnose and repair failing
units as well as the cost of tying up whatever equipment is needed to do that work. The time it takes to diagnose and repair increases the time needed to move assets through the manufacturing process, thus increasing the work-in-process inventory and its associated costs. Finally that time also increases the time needed to fulfill a customer's order, possibly resulting in lost revenues. These hidden costs can be difficult to track.

During the service life at the customer's site, there can be hidden test costs which may be almost completely invisible. For example, if it is suspected that the product is malfunctioning, the customer bears some cost while the product is not available for use. If the product has some type of test which the customer can perform, the customer bears the cost of running that test. If the customer is unable to do the tests, it may be necessary for the producer to send field service personnel to the customer.

During field repair or depot test, either the customer has lost the ability to use the product (which results in a cost) or the producer provides a replacement item (which further results in costs) while the defective unit is being repaired. In addition, if the on-site diagnosis (which lead to the conclusion that the product should be returned) was faulty, there are costs associated with placing the product in a repair loop.

JUSTIFYING DESIGN FOR TESTABILITY
Overview
At the tactical level, justifying DFT involves a discussion between design engineers and test engineers; the test engineer must ask the design engineer to modify the product's design to render it easier to test. At the strategic level, justifying DFT involves tradeoffs which should be evaluated from the business point of view, in an attempt to arrive at a decision which makes good business sense. The points of contention in these discussions generally turn on three factors: cost, product performance and time.

We believe that justifying DFT should not be seen as a negotiation situation, nor as an exercise in which one organization forces its will on another; rather, it is an effort to raise the appropriate concerns for all parties in a manner which leads to the best business decisions.

We further believe that there is an after-the-fact side of DFT which is not often practiced; that it is desirable to re-examine the issues some time after products have been designed and are being manufactured and delivered, so that subsequent efforts can benefit from lessons learned.

DFT Cost Issues
Making a product more testable requires adding something to the product which inherently increases the raw materials costs of the product. Some examples:

- It may be necessary to use Pullup/Pulldown resistors on device pins which might otherwise be hard wired to power supply levels;

- Providing full bottom-side nodal access to a surface mount PCB may require more inner layers in the board, increased wiring density and lower functional density;

- The implementation of a PAL may consume all available Input/Output pins in the selected device, and adding DFT features may require using the next larger (more expensive) part in the family;

- For digital devices available with or without boundary scan, the scan part is likely more expensive, has four (or five) additional pins, and may be a sole source item;

- Adding a test-only connector (for functional test) may require more PCB real estate than is presently available.

In all of these cases, the test engineer is seeking to reduce a test cost by asking for higher materials costs. In general, the requested DFT feature allows higher coverage programs to be developed in less time, which provides savings in test software costs and diagnostics and repair costs.

From the business perspective, the correct decision is the one which provides the lowest overall cost. Therefore, the requested DFT features are cost-justified if the cost savings (and/or cost avoidance's) achieved by including DFT are greater than the increase in materials costs. While this may seem starkly obvious, there are problems in reaching the correct decision. The design engineer can probably say exactly what the increase in materials costs will be; the test engineer can probably only estimate what the savings in test costs will be, based on experience and intuition. Neither side will ever have the actual numbers to support its position. It would be unrealistic to carry out both courses of action in parallel, and let the final decision be made with both versions of the product available.

Justifying DFT on the basis of cost requires concessions from both the design engineer and the test engineer. Design engineers must not focus on material costs to the exclusion of all other product costs. Test engineers must do better at tracking, analyzing and disseminating historical test cost information, and at using this information to accurately predict the impact on future test costs of DFT.

DFT Product Performance Issues
Product performance is a somewhat broad topic. We confine ourselves to a few specific performance-related issues, pointing out instances where DFT may affect those areas:
- The Need For Speed. The most common example is the test engineer's request to use a boundary scan device, where the use of fully-1149.1-compliant scan adds delays in the circuits, degrading the performance of the design;

- With PCBs, the requested DFT features may require additional package parts, which decreases the amount of product functionality otherwise available;

- With ASICs, the requested DFT features may require additional gates and/or pins, decreasing the amount of product functionality otherwise available.

It is not possible to give "pat" answers when justifying DFT on the basis of product performance. Rather, we believe that design engineers should consider test, and DFT, as one other attribute of the product's design, subject to tradeoff as are other aspects of the design.

**DFT Time Issues**
Since designing a product to be testable requires adding something to it that would otherwise not be there, this is seen as adversely affecting the time to complete the design, and therefore having a negative impact on time to market for the product.

Time to market is many things to many people. We consider it to be the time from the point where product concept is begun to the point where the product is in the hands of a paying customer. From that viewpoint, such milestones as schematic capture complete, PCB layout complete, and design verification complete are indeed steps along the way, but not the only steps. One has to consider the various efforts after the design is completed (purchase materials, assemble, test) and consider the time necessary to conduct those activities.

Some argue that there are other, more meaningful times than the time at which the first instance of a product is in a customer's hands. Time to quality, is the point where the product is being consistently delivered at an acceptable quality level. Another is time to profit, which is the point where the revenues from product sales have paid back the fixed development costs incurred, and each unit shipped provides positive net income for the company.

As before, the test engineer seeks to reduce all relevant test times by asking for slightly longer design times, since the requested DFT feature allows better tests to be developed in less time. Further, if the correct DFT methods have been chosen, there should be some benefits in reducing design verification times.

From the business perspective, the correct decision is the one which provides the lowest total time. Therefore, the requested DFT features are justified if the time savings (and/or time avoidance's) achieved by including DFT are greater than the increase in any single time to in the entire project.

**DFT Retrospection**
While DFT is a forward-looking activity, there is also a time for looking back. As we said, one can never do a side-by-side comparison of an un-testable version of a product against a testable version. In the interest of adding some sanity and closing the loop, we make the following observations:

There must be credible incentives to use DFT. A designer who makes the tradeoff in favor of DFT must see the benefits of using it, and one who makes the tradeoff in the other direction must see the penalties of not using it. Therefore, it is desirable that the test engineer be able to show what happened. What was the actual test development time against scheduled test development time? What were the actual test equipment costs against budgeted test equipment costs? What are the actual recurring test costs against expected recurring test costs? While this places an additional tracking burden on the test engineer, we believe that this is an important part of the story, since it is the only way one can know if the right decisions were made. Such data collection and analysis can also give the test engineer more insight as to whether or not the correct DFT proposals were made, or whether other alternatives should have been considered.

If you share the belief that justifying DFT should be on the basis of what's best for business, then you will share our belief that we need to have the facts and numbers which support the use of DFT, and which enable us to make accurate, deliverable predictions of what those benefits will be.

**GENERAL DESIGN FOR TEST GUIDELINES**
The purpose of this section is to provide you with some fundamental DFT guidelines.

Though there are multiple aspects to design for testability, the basic fundamentals can be summed up in 3 elements; visibility, initialization, and control [6]. The board designer increases testability by ensuring the design has ample mechanical and electrical access, can initialize all circuits, and provide isolation and control for all circuits and components.

**VISIBILITY** - is the ability in which the automatic test equipment (ATE) drivers and detectors have physical access to contact the board under test (BUT) to provide stimulus and detect response. Virtual access to nodes where physical access is not possible can be provided by using IEEE 1149.1 boundary scan.
INITIALIZATION - is the ability to place a device/circuit/board into a known state from which all future states can be predicted.

CONTROL - is the ability to control the operation of a circuit or device, including the electrical isolation of circuits and components.

ELECTRICAL CONSIDERATIONS FOR INCIRCUIT TEST

Tri-State Devices Whenever possible use tristate devices instead of non-tristate. Tristate devices allow for easy initialization, isolation, and control for incircuit testing.

![Tristate Devices Diagram]

Not Preferred

Preferred

FIGURE 4. Tristate devices are preferred over non-tristate.

Control Pins Never tie device control pins such as Set, Reset, Chip Enable, Output Enable, Clear, etc. directly to a power or ground rail. Instead use a unique, resistor in series between the rail and each control pin. This technique will allow tester access to the control pins for initialization and control.

![Control Pins Diagram]

Not Preferred

Preferred

FIGURE 5. Use unique series resistors between power or ground rails and control pins.

Oscillators and Clocks To insure there is no interference by clock circuits or oscillators during incircuit testing, make certain that oscillators and clocks can be controlled. Many oscillators today come with built in control pins which turn the oscillator off. The same objective can be accomplished by using a gate to isolate the clock.

![Oscillators and Clocks Diagram]

FIGURE 6. Oscillators and clocks can be controlled by either selecting a device with built in control or adding a gate to block the clock signal.

Feedback Loops Feedback loops can interfere with incircuit testing and need the ability to be broken. Inserting a gate in the feedback path will provide isolation and control of the circuit.

![Feedback Loops Diagram]

FIGURE 7. Inserting a gate in the feedback path can provide isolation and control of feedback circuits.

Tester Capacity For 100% nodal access the testers pin capacity should be taken into consideration. Designs that exceed the pin capacity can result in reduced fault coverage or expensive multiple test process steps.
Non-Tristate Devices  Non-tristate devices need the ability to be easily initialized to a preferred state. A preferred state is a logic state that can easily be back driven by the tester during in-circuit test. Examples of preferred states are logic "1" for TTL or CMOS and logic "0" for ECL technology. Initializing to preferred states will reduce the likelihood of false failures or intermittent false failures due to marginal signals caused by improper initialization.

FIGURE 8. This CMOS field programmable gate array (FPGA) utilizes an ICT pin which initializes all outputs to a preferred logic high.

Adjustments  Avoid designing in adjustments that require intervention by an operator during the test process. Adjustments will increase test times as well as rule out complete automation or the ability to run overnight. Adjustments may also require special equipment or warrant added test process steps.

Device Drive Capability  Devices that have outputs which exceed the maximum drive current of the tester must be tristateable.

ASIC DFT RECOMMENDATIONS
The ability to cram more electrical gates into smaller packages has led to the increased use of ASICs in electrical designs. As a result more responsibility of ensuring testability has moved from the test engineers plate to the ASIC designer. Figure 9 is a Testability Development Flow [7] which guides one through a decision making process to determine the type of testability and test strategy that can best be taken advantage of for various ASIC designs.

Figure 9. ASIC Testability Process Flow

1. Select a technology that provides enough performance and gate count margin to allow the insertion of testability.
2. Commit to using testability design practices and review them with the design team before the design begins. Add a testability commitment to the design-requirements document developed for the design project.
3. Establish a fault-grade requirement. This can usually be provided by the manufacturing or quality organization. Establish this requirement before the first design review. Add the fault grade requirement to the design-requirement document.
4. Decide if IEEE 1149.1 will be a system requirement. When implemented an ASIC device, IEEE 1149.1 allows test of the interconnect between devices on a PCB through a four pin test bus.
5. Select an ASIC testability approach based on gate density: Designs with fewer than 10k gates are not generally complex enough to require structured test approaches. Designs with more than 10k gates but less than 20k gates are candidates for structured techniques. Designs with more than 20k gates usually require structured approaches to achieve high fault grades.
6. Choose structured tools. Scan testing is the preferred structured approach for sequential logic.
7. Establish a diagnostic functional pattern set to expedite debug. This is an important step in decreasing the time to market for an ASIC device.
8. Generate high-fault-grade-test patterns to ensure the best possible quality level attainable with that set of patterns.
9. Simulate test patterns and timing to verify both functionality and performance of the device.
BOARD LAYOUT AND MECHANICAL GUIDELINES

Access
(Bottom Side) Physical access must be limited to the bottom side of the board to eliminate the need for complex/costly test fixturing.
(Thru Hole) Access to thru-hole components are, by design, not an issue.
(Surface Mount) Surface mount designs must provide a test pad for every net to guarantee 100% physical nodal access.
(Virtual Access) Virtual access may be acceptable over physical access in cases such as use of IEEE 1149.1 boundary scan etc.

Tooling Holes
Each board must have a minimum of two unobstructed tooling holes located at opposing corners of the BUT. The tooling holes are not to be used for any other purpose except for board registration purposes. The tooling holes are 0.128" dia., +/-0.002", non-plated.

Plated Thru-Holes
In manufacturing, consider soldering all open plated thru holes. For boards that are tested on a vacuum actuated bed of nails fixture, this will minimize air leaks and avoid poor fixture contact that can result in mis-diagnoses. It can also avoid more costly fixturing solutions such as mechanical overclamps.

Silk Screen
A silk screen should be used that contains component reference designators for fast identification of components. For extremely dense boards where reference designators are not possible a grid system can be screened on the board or on the boards perimeter. A look up table can be created to locate components on the grid.

For high pin count SMT components, silk screened hash marks at every ten (10) or twenty (20) pin intervals is useful for identifying component pin numbers.

Test Pads Test Pads are any bottom-side via pads (SMT or thru-hole) used for probing.

Test Pad Diameter
Test pad diameters kept between 0.034 to 0.040 inches will ensure reliable contact using standard test probes.

Test Pad Clearance
Clearance between test pad to test pad should be 0.100 inches. This ensures that standard test probes can be used. Use of non-standard probes are more costly and less durable.

The clearance between the edge of a test point and the edge of a trace should be 0.020".

The clearance between the edge of a test pad and a via should be 0.020".

Bottom-side SMT components may present problems for a bed-of-nails test fixture. Test pads need to have a clearance from the edge of the pad to the edge of the component of 0.050". Components over 0.200" tall involves an additional review for fixturing problems. Test pads near components over 0.200" should have a minimum clearance between 0.100" to 0.200".

CONCLUSIONS
The continuous increase of densities in both components and printed circuit boards has resulted in challenges for test. Today's electronic designs are more dense and complex than ever. As these designs continue to grow in complexity and density, testing them has become increasingly difficult due to added test constraints and restrictions. In order for companies to be successful at performing test and remain competitive, design-for-test practices must be implemented. Though there are many advantages of embracing design for test, the overall benefits will yield a quality product at lower cost that can be delivered on a more timely and routine basis.

Design for test needs to begin as early in the product development cycle as possible. The later in the process that DFT begins, the less likely changes or modifications can be made for the benefit of testing. Not only is beginning early important but, once DFT is established, continuous communication needs to occur. Continuous communication is essential because of the dynamics that take place during the design phase. While in the design phase, design decisions can change frequently. The best method to facilitate continuous communication during the development of a product is through concurrent engineering. Concurrent engineering provides a communication link not only to the designer of the product but, also to various other groups in the company that have an interest or stake in the design. An additional element of communicating DFT is through an up-to-date documented set of guidelines. A general set of DFT guidelines has been provided as part of this paper.

The development of a test strategy should be viewed as an element of DFT and should also begin early in the product development cycle. Defining the test strategy early will allow design trade-offs to made while considering the impact on the test strategy.

When taking a life cycle view of test activities, test cuts across organizational boundaries. Test is performed at design during design verification test, in production test, at the customer site, and as product is returned from the
field. When implementing DFT, one must consider test activities and the associated costs at each stage throughout the products life cycle. In addition, one must also consider the hidden costs of test. The best decisions that are made during the DFT process are the ones that consider all aspects of the product, and the products life which will yield the greatest benefit to the company.

In completing the DFT cycle one must learn from the past and use that experience to improve the future. A robust DFT process includes steps to reflect on decisions that were made and incorporate improvements to future DFT processes.

REFERENCES

DESIGN FOR RELIABILITY
IN ADVANCED ELECTRONIC PACKAGING

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1. INTRODUCTION—KEYS TO RELIABILITY

The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. There exists a misconception in the industry, that quality manufacturing is all that is required to assure the reliability of an electronic assembly.

While of course, consistent high quality manufacturing—and all that this implies in terms of Design for Manufacturability (DFM), Design for Assembly (DfA), Design for Testability (DfT), etc.—is a necessary prerequisite to assure the reliability of the product, only a Design for Reliability (DFR) can assure that the design—manufactured to good quality—will be reliable in its intended application.

Thus, adherence to quality standards is necessary but not sufficient. For example, solder joint quality in the U.S. is generally measured against criteria in both IPC-A-620, Acceptability of Electronic Assemblies with Surface Mount Technologies, for overall workmanship and ANSI/J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies. However, meeting these criteria does not assure reliable solder connections, only quality solder connections.

To clarify the difference between the two requires an explanation and a definition of reliability. Reliability is defined in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, by:

Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

In the short term, reliability is threatened by infant mortality failures due to insufficient product quality; these infant mortalities caused by defects can be eliminated prior to shipping by the use of appropriate screening procedures. Long term failures are the result of premature wear-out damage caused by inadequate designs of the assembly.

It is for this reason that IPC-D-279, Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies, is being developed. Since DFM and DfA are treated in other SMC White Papers, DFR will be the emphasis of this paper.

2. EMERGING ADVANCED TECHNOLOGIES AND RELIABILITY

The emerging new technologies provide ever more challenges to assure the reliability of electronic products. Solder joint reliability is becoming an even more important issue with the advent of new surface mount packages, such as Thin
Small Outline Packages (TSOPs), Ball Grid Arrays (BGAs), Column Grid Arrays (CGAs), Multi-Chip Modules (MCNs), Chip-on-Board (COB), etc. These packages are characterized by larger sizes, finer pitches, and/or problematic materials which require an upfront DfR to meet reliability requirements.

The reliability of plated-through vias (PTVs) is also becoming more challenging as the diameters of PTVs in printed wiring boards (PWBs) and components decrease. New materials and material combinations, particularly those constraining the coefficients of thermal expansion (CTE) in the x- and y-directions, pose challenges that need to be addressed by a DfR approach.

Another reliability concern is the insulation resistance between assembly features at different electrical potential. Here the available knowledge is significantly less complete, because failures typically occur only in the artificially severe conditions of highly accelerated stress tests (HAST) and only rarely at use conditions. The reliability concerns arise from the use of new materials with unknown behavioral characteristics and the shrinking dimensional separation of features as the assembly densities increase.

3. SOLDER ATTACHMENTS

3.1 DAMAGE MECHANISMS AND FAILURE

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical, electrical, and thermal interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the PWB and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the PWB. The characteristics of these three elements—component, substrate, and solder joint—together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

3.1.1 Solder Joints and Attachment Types

Solder joints are anything but a homogeneous structure. A solder joint consists of a number of quite different materials, many of which are only superficially characterized. A solder joint consists of (1) the base metal at the PWB, (2) one or more intermetallic compounds (IMC)—solid solutions—of a solder constituent—typically tin (Sn)—with the PWB base metal, (3) a layer from which the solder constituent forming the PWB-side IMC(s) has been depleted, (4) the solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations, (5) a layer from which the solder constituent forming the component-side IMC(s) has been depleted, (6) one or more IMC layers of a solder constituent with the component base metal, and (7) the base metal at the component.

The grain structure of solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating fatigue damage. At the grain boundaries contaminants like lead oxides are concentrated; as the grains grow these contaminants are further concentrated at the grain boundaries, weakening these boundaries. After the consumption of ~25% of the fatigue life micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture as is schematically shown in Figure 1.

Surface mount solder attachments exist in a wide variety of designs. The major categories are leadless and leaded solder
between those without fillets, e.g., Flip-Chip C4 (Controlled Collapse Chip Connection) solder joints, BGAs with C5 (Controlled Collapse Chip Carrier Connection) solder attachments, BGAs with high-temperature solder (e.g., 10Sn/90Pb) balls, and CGAs with high-temperature solder columns; and solder joints with fillets, e.g., chip components, Metal Electrode Face components (MELFs), and castellated leadless chip carriers. The leaded solder attachments differ primarily in terms of their compliance and can be roughly categorized into components with super-compliant leads \((L_D<-9 \text{ N/mm } (-50 \text{ lb/in}))\), compliant leads \((-9 \text{ N/mm}<L_D<-90 \text{ N/mm})\), and non-compliant leads \((L_D>-90 \text{ N/mm } (-500 \text{ lb/in}))\).

The different surface mount solder attachment types can have significantly different failure modes. Solder joints with essentially uniform load distributions, e.g., Flip-Chip, BGA, CGA, show behavior as illustrated in Figure 1. Solder joints with non-uniform load distributions, e.g., those on chips components, MELFs, leadless chip carriers, and all leaded solder joints, show localized damage concentrations with the damage shown in Figure 1 preceding an advancing macro-crack.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches [Refs. 1-6], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches [Refs. 4, 7].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. In Table 1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated [Refs. 8, 9]. However, it needs to be emphasized, that the information in Table 1 should serve only as a general guideline; for some use categories the description of the expected use environment can be rather more complex [Ref. 9].

3.1.2 Global Expansion Mismatch

The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the PWB to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the CTEs and thermal gradients as the result of thermal energy being dissipated within active components.

Global CTE-mismatches typically range from \(\Delta \alpha=2 \text{ ppm/}^\circ\text{C} (1 \text{ ppm}=1\times10^{-6})\) for CTE-tailored high reliability assemblies to \(-14 \text{ ppm/}^\circ\text{C} \) for ceramic components on FR-4 PWBs. CTE-mismatches of \(\Delta \alpha<2 \text{ ppm/}^\circ\text{C} \) are not achievable in reality as a consequence of the variability of the CTE values of the materials involved on both components and PWBs.

Global thermal expansion mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch—the CTE-mismatch, \(\Delta \alpha\), the temperature swing, \(\Delta T\), and the acting distance, \(L_D\)—are large.
Table 1. Realistic Representative Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics by Use Categories [Ref. 10].

<table>
<thead>
<tr>
<th>USE CATEGORY</th>
<th>WORST-CASE USE ENVIRONMENT</th>
<th>Accept.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tmin °C</td>
<td>Tmax °C</td>
</tr>
<tr>
<td>1 CONSUMER</td>
<td>0</td>
<td>+60</td>
</tr>
<tr>
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<td>+15</td>
<td>+60</td>
</tr>
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<td>4 COMMERCIAL AIRCRAFT</td>
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<td>+95</td>
</tr>
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<td>5 INDUSTRIAL &amp; AUTOMOTIVE - PASSENGER COMPARTMENT</td>
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<td>+95</td>
</tr>
<tr>
<td>6 MILITARY GROUND &amp; SHIP</td>
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<tr>
<td>9 AUTOMOTIVE - UNDER HOOD</td>
<td>-55</td>
<td>+125</td>
</tr>
</tbody>
</table>

& = in addition

(1) ∆T represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.

Global thermal expansion mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch—the CTE-mismatch, ∆α, the temperature swing, ∆T, and the acting distance, Lp—are large.

This global expansion mismatch will cyclically stress, and thus fatigue, the solder joints. The cyclically cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint, of the component causing functional electrical failure that is initially intermittent.

3.1.3 Local Expansion Mismatch

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or PWB to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions [Refs. 4, 7].

Local CTE-mismatches typically range from ∆α ~ 7 ppm/°C with copper to ~18 ppm/°C with ceramic and ~20 ppm/°C with Alloy 42 and Kovar™. Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller—in the order of hundreds of μm (tens of mils).

3.1.4 Internal Expansion Mismatch

An internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension—in the order of less than 25 μm (~1 mil) [Ref. 11].

3.1.5 Solder Attachment Failure

The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the
component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists.

Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration (<1 μs) high-impedance event during either a mechanical or thermal disturbance. From a practical point of view, the solder joint failure is defined as the first observation of such an event.

For some applications this failure definition might be inadequate. For high-speed signals with sharp rise times signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

3.2 RELIABILITY PREDICTION MODELING

3.2.1 Creep-Fatigue Modeling

It has been experimentally shown [Refs. 2, 4, 12, 13] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation [Ref. 14] developed for more typical engineering metals. For practical reasons and as the direct consequence of the time-dependent stress-relaxation/creep behavior of the solder at typical use environments (see Table 1), the specialized case of the Coffin-Manson equation requires reversion to the more general strain-energy relationship of Morrow [Ref. 15]; it also requires that the cyclic strain energy be based on the total possible thermal expansion mismatch and that the exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process. The Engelmaier-Wild solder creep-fatigue equation [Refs. 1-6, 9, 12], subject to some caveats listed later, relates the cyclic visco-plastic strain energy, represented by the cyclic fatigue damage term, ΔD, to the median cyclic fatigue life for both isothermal-mechanical and thermal cycling [Ref. 16]

\[ N_f(50\%) = \frac{1}{2} \left[ \frac{2 \epsilon^f}{\Delta D} \right]^{\frac{1}{c}} \]  

(3.1)

where \( \epsilon^f \) = fatigue ductility coefficient, =0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of \( \epsilon^f \) is expected to be somewhat different).

Solder, uniquely among the commonly used engineering metals, readily creeps and stress relaxes at normal use temperatures; the rate of creep and stress-relaxation is highly temperature- and stress-level-dependent. Thus, the cyclic fatigue damage term, ΔD, for practical reasons, has to be based on the total potential damage at complete creep/stress relaxation of the solder. For cyclic conditions that do not allow sufficient time for complete stress relaxation, ΔD is larger than the actual fatigue damage. The temperature- and time-dependent exponent, \( c \), compensates for the incomplete stress relaxation and is given by

\[ c = -0.442 - 6 \times 10^{-4} \frac{1}{T_{SJ}} + 1.74 \times 10^{-2} \ln (1 + \frac{360}{t_D}) \]

(3.2)

where \( T_{SJ} \) = mean cyclic solder joint temperature, \( t_D \) = half-cycle dwell time in minutes.

The half-cycle dwell time relates to the cyclic frequency and the shape of the cycles and represents the time available for the stress-relaxation/creep to take place.

In Eq. 3.1 the exponent is given as (-1/c), which is mentally confusing: this format exists for historical reasons in that the underlying work [Refs. 14, 15] was always stated this way. For typical electronic applications (\( T_{SJ} = 0 \) to 100°C and \( t_D = 15 \) to 720 minutes) the exponent (-1/c) ranges between 2.0 and 2.6.

Equations 3.1 and 3.2 come from a generic understanding of the response of SM solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to the global thermal expansion.
mismatches between component and substrate. These shear displacements cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress relaxation strains. These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area, given as the damage term \( \Delta D \), is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained [Refs. 13, 17-19].

3.2.2 Damage Modeling

The assessment of the cyclically cumulating fatigue damage is not a straightforward task. While Eq. 3.1 is widely used, the question of how to best quantify the cyclic fatigue damage is still hotly debated. The choices are primarily between more complex finite-element analyses (FEA), which can give more detailed information and can include second-order effects, but require a large number of not fully-supported assumptions (Ref. 20); and closed-form empirically-based relationships of the first-order design parameters, which cannot include second-order effects and have use limitations due to their simple nature, but allow, due to their simple form, a direct assessment of the impact of the primary design parameters as well as design trade-offs.

The following cyclic fatigue damage terms are of the simplified closed-form type and should be utilized with the application caveats that follow [Refs. 1-6, 9, 12, 16, 21].

The cyclic fatigue damage term for leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength and cause plastic yielding of the solder, is

\[
\Delta D(\text{leadless}) = \left[ \frac{F L_D \Delta (\alpha \Delta T)}{h} \right]
\]

For solder attachments with leads compliant enough, so that the solder joint stresses are below the yield strength and thus are not bounded by it, the cyclic fatigue damage term is

\[
\Delta D(\text{leaded}) = \left[ \frac{F K_D [L_D \Delta (\alpha \Delta T)]^2}{133 \text{ psi} Ah} \right]
\]

where for metric units the scaling coefficient is 919 kPa instead of 133 psi. Equations 3.3 and 3.4 contain the design parameters that have a first-order influence on the reliability of SM solder attachments. They are

\[
A = \text{effective minimum load bearing solder joint area},
\]

\[
F = \text{empirical "non-ideal" factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, different solder crack propagation distances, brittle IMCs, Pb-rich boundary layers, and solder/bound-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 3.1 through 3.4; } 1.5 > F > 1.0 \text{ for ball/column-like leadless solder joints (C4, C5, BGAs, CGAs), } 1.2 > F > 0.7 \text{ for leaded solder joints with fillets (castellated chip carriers and chip components), } F = 1 \text{ for solder attachments utilizing compliant leads;}
\]

\[
h = \text{solder joint height, for leaded attachments } h = 1/2 \text{ of solder paste stencil depth as a representative dimension for the average solder thickness;}
\]

\[
K_D = \text{"diagonal" flexural stiffness of unconstrained, not soldered, corner-most component lead, determined by strain energy methods [see Refs. 22-25] or FEA;}
\]

\[
L_D = \text{maximum distance between component center and the most remote component solder joint measured from the component solder joint pad center; } L_D \text{ is sometimes referred to as the distance from the neutral point (DNP);}
\]

\[
T_C, T_S = \text{steady-state operating temperature for component, substrate (} T_C > T_S \text{ for power dissipation in component) during high temperature dwell;}
\]

\[
T_{C, 0}, T_{S, 0} = \text{steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles } T_{C, 0} - T_{S, 0} ;
\]

\[
T_{SJ} = (1/4)(T_C + T_S + T_{C, 0} + T_{S, 0}) \text{, mean cyclic}
\]

\( \alpha_c, \alpha_s \) = CTEs for component, substrate;
\( \Delta D \) = potential cyclic fatigue damage at complete stress relaxation;
\( \Delta T_c \) = \( T_c - T_c,0 \), cyclic temperature excursion for component;
\( \Delta T_s \) = \( T_s - T_s,0 \), cycling temperature excursion for substrate (at component);
\( \Delta(\alpha T) = |\alpha_s \Delta T_s - \alpha_c \Delta T_c| \), absolute cyclic expansion mismatch, accounting for the effects of power dissipation within the component as well as temperature variations external to the component;
\( \Delta \alpha = |\alpha_c - \alpha_s| \), absolute difference in CTEs of component and substrate, CTE-mismatch, because of the inherent variability in material properties \( \Delta \alpha < 2 \times 10^{-6} \) should not be used in calculating reliability.

3.2.3 CAVEAT 1—Solder Joint Quality

The solder joint fatigue behavior and the resulting reliability prediction equations, Eqs. 3.1 through 3.4, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the IMC layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the 'weakest link' in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing a proper metallurgical bond of the solder to the underlying metal; brittle IMC layers too thick due to too many or improperly long high temperature processing steps.

Some material choices can lead to lower quality and weaker solder joints because the material is more difficult to wet with solder. The nickel/iron alloys, Kovar™ and Alloy 42, fall into this material category. The resulting lower solder joint quality indicated in Table 2 is also clearly evident in Figure 2, where the solder joint pull strength is shown for a variety of differently prepared Alloy 42 and copper leads. Alloy 42 leads, even when etched or pre-reflowed at temperatures higher than can be tolerated by the component, show a substantial reduction in the solder joint pull strength relative to copper. In the worst instance, the leads from one Alloy 42 manufacturer have a pull strength of less than half of those with more typical Alloy 42 and are essentially non-wettable.

<table>
<thead>
<tr>
<th>Reflow Temperature °C</th>
<th>Solder Joint Quality</th>
</tr>
</thead>
<tbody>
<tr>
<td>60/40 Solder to Copper</td>
<td>60/40 Solder to Alloy 42</td>
</tr>
<tr>
<td>~210</td>
<td>just o.k.</td>
</tr>
<tr>
<td>~240</td>
<td>good</td>
</tr>
<tr>
<td>~260</td>
<td>good</td>
</tr>
</tbody>
</table>

Early failures of the solder attachments of components with Alloy 42 lead frames and leads during accelerated testing [Refs. 26-30] and manufacture [Ref. 31] have been documented.

Solder joints which have solder joint heights (gaps) of \( h < 50 \) to 75 µm (2 to 3 mils) also require special attention. For solder joints that thin, the gap is essentially filled with intermetallic compounds and those solder metals that do not go into solution with the base metals to form the IMCs. Therefore Eqs. 3.1 and 3.2 do not apply because these gaps are not filled with solder [Ref. 32]. These materials do not creep as readily, if at all, at the prevailing temperatures and are typically more brittle, but much stronger than solder. Thus, fatigue lives are longer than would be predicted from Eqs. 3.1 and 3.2 unless overstress conditions occur.

On the other hand, the fatigue lives of solder attachments can be underestimated by Eqs. 3.1 through 3.4 if the component is underfilled with a load-bearing substance, e.g., epoxy [Ref. 33]. Components that are glued down to the substrate result in higher solder joint fatigue reliability, since the solder joints are loaded in compression when the adhesive contracts on cooling from the solder reflow temperatures. Covercoats can either increase or decrease solder joint fatigue lives depending on the properties of the covercoat and when and how it is applied. Parylene™ has been
found to increase the solder joint fatigue life by about a factor of three.

In general, caution might be indicated in all instances were the predicted life is less than 1000 cycles, because the severe loading conditions producing such short lives are likely to produce different damage mechanisms in the failure modes.

3.2.4 CAVEAT 2—Large Temperature Excursions

Solder joints experiencing large temperature swings which extend significantly both below and above the temperature region bounded by $-20^\circ\text{C}$ to $+20^\circ\text{C}$, in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in Eqs. 3.1 and 3.2 [Ref. 34]. The damage mechanism is different than for more typical use conditions and is likely dependent on a combination of creep-fatigue and over-stressing, causing early micro-crack formation, and high stresses at these stress-concentrating micro-cracks causing faster crack propagation during the high stress cold temperature excursions, as well as recrystallisation considerations.

3.2.5 CAVEAT 3—High-Frequency/Low-Temperatures

For high-frequency applications, $f>0.5$ Hz or $t_p<1$ s, e.g., vibration, and/or low temperature applications, $T_{\min}<0^\circ\text{C}$, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson [Ref. 14] fatigue relationship might be more appropriate. This relationship is

$$N_f(50%) = \frac{1}{2} \left( \frac{2\gamma'}{\Delta\gamma_p} \right)^{-c}$$

where $\Delta\gamma_p$ is the cyclic plastic strain range and $c=0.6$.

It has to be noted, that the determination of $\Delta\gamma_p$ depends on the expansion mismatch displacements and the separation of the plastic from the elastic strains.

For loading conditions of this character, it is
possible that high-cycle fatigue behavior may be observed.

3.2.6 CAVEAT 4—Local Expansion Mismatch

For applications for which the global thermal expansion mismatch is very small, e.g., ceramic-on-ceramic or silicon-on-silicon (flip chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations 3.3 and 3.4 do not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an interfacial stress analysis [Ref. 35] and appropriate accelerated testing.

For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g., Kovar™ or Alloy 42, the results from Eqs. 3.1 and 3.2 will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included. Suhir (Ref. 35) has shown that the interfacial stresses resulting from the local expansion mismatch follow

\[ \tau \propto L \left( \alpha_{\text{Solder}} - \alpha_{\text{Base}} \right) (T_{\text{max}} - T_{\text{min}}) \]  \hspace{1cm} (3.6)

where \( L \) is the wetted length of the solder joint. In addition, besides substantial shear stresses at the interface between the solder joint and the base material to which it is wetted, even larger peeling stresses occur. Both of these stresses are proportional to the parameters given in Eq. 3.6.

From Eq. 3.6 it is quite clear that for leads consisting of Alloy 42, the wetted length of the solder joint, that is the length of the lead foot should be minimized to reduce interfacial stresses. That, of course, is contrary to the good practice that the foot length should be at least three times the lead width for optimum solder joint quality. However, since in most applications, the local expansion mismatch results in contributory damage to the more important damage caused by the global expansion mismatch, this contra-indication can be ignored without suffering catastrophic consequences.

From the available experimental data, the damage term, to be used in Eq. 3.1, for the local expansion mismatch alone is

\[ \Delta D(\text{local}) = \left[ \frac{L \Delta \alpha \Delta T}{L_0} \right] \]  \hspace{1cm} (3.7)

where the parameters are the same as in Eq. 3.6 and \( L_0 = 0.004 \) in. (0.1 mm), a scaling wetted length. The local expansion mismatch is then treated as an additional loading condition (see Sections 3.2.9 & 3.2.10).

3.2.7 CAVEAT 5—Very Stiff Leads/Very Large Expansion Mismatches

Equations 3.3 and 3.4 differentiate between surface mount solder attachments that are leadless and those with compliant leads. Leadless solder attachments presume substantial plastic strains due to yielding prior to creep and stress relaxation, whereas Eq. 3.4 assumes that the compliant leads prevent stresses in the solder joints to reach levels where substantial yielding, and thus plastic strains prior to creep and stress relaxation, can take place.

However, there is an intermediate region that is not covered by these assumptions. For very stiff, non-compliant leads (e.g., SM connector headers), perhaps at lead stiffnesses \( K_D > 90 \) N/mm (~500 lb/in) and/or for very large thermal expansion mismatches (e.g., ceramic MCMs on FR-4) resulting in strain ranges \( \Delta \gamma > -10\% \), the damage estimates in Eq. 3.4 can be substantially in error, because the assumptions underlying Eq. 3.4 are violated.

For very stiff leads the stresses calculated in Eq. 3.4 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. 3.4 needs to be bounded by the yield strength of solder in shear.

For very large thermal expansion mismatches the full displacements will not be transmitted to the solder joints, because the leads will accommodate displacements by plastic deformations of the lead material. Possible exceptions are situations where very stiff leads are also involved, in which case the solder joint reliability is best
estimated using Eq. 3.1 for leadless solder attachments. The strain range that can be accommodated by creep and stress relaxation in the solder joints can be significantly exceeded by the displacements resulting from very large thermal expansion mismatches and the cyclic fatigue damage would be significantly overestimated. Under these conditions FEA is required to determine the split in the accommodation of the displacements between the lead and the solder joints.

Under these circumstances, Eqs. 3.3 and 3.4 will provide lower and upper bounds for the reliability estimates, respectively. The higher the lead stiffness, the closer the expected results will be towards the results given by Eq. 3.3 for the leadless—"infinitely stiff leads"—solder attachments. Very high lead stiffnesses can occur in the case of through-hole component leads converted to surface mount and for connector headers where the male header pins have been simply bent into a gull-wing lead foot without any reduction in the lead cross-section. Very high thermal expansion mismatches occur primarily in accelerated testing and in extraordinary environments like storage and transport for products that are designed for benign operating environments.

3.2.8 Statistical Failure Distribution and Failure Probability

While the physical parameters define the median cyclic fatigue life from physics-of-failure considerations, solder attachment failures for a group of identical components will follow a distribution—like all fatigue results—which typically is best described by a Weibull statistical distribution [Ref. 36]. Given the statistical distribution, the fatigue life at any given failure probability for the solder attachment of a component can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable cumulative failure probability per component, \( x \), is—assuming a two-parameter (2P) Weibull statistical distribution—given by

\[
N_f(x\%) = N_f(50\%) \left[ \frac{\ln(1 - 0.01x)}{\ln(0.5)} \right]^{-\beta} \quad (3.8)
\]

where \( \beta \) = Weibull shape parameter or slope of the Weibull probability plot; typically \( \beta \approx 3 \) for fatigue tests, from low-acceleration tests of still leadless solder attachments \( \beta = 4 \) and \( \beta = 2 \) for compliant leaded attachments.

Experimentally, \( \beta \) can be found to be quite variable with more severely accelerated reliability tests resulting in tighter failure distributions and thus giving larger values for \( \beta \). Values of \( \beta \) in the range of 1.8 to 9.0 have been observed.

There is some, unfortunately as yet inadequate, evidence that for lower failure probabilities a three-parameter (3P) Weibull distribution, postulating a failure-free period prior to first failure [Refs. 32, 37], may be applicable. From physics-of-failure and damage mechanism considerations, a failure threshold as provided by a 3P-Weibull distribution makes sense, since the fatigue damage in the solder joints has to accumulate to crack initiation and complete crack propagation. While the 2P-Weibull distribution may be overly conservative for designs to very small acceptable failure probabilities \( (-x < 0.1\%) \), a too liberal choice of the failure-free period is definitely non-conservative. This area requires more work.

Also, when designing to low failure probabilities, the variability in the quality of the solder joints may no longer be negligible; also solder joints with latent defects that made it into the field will have in impact on the actual failure experience of a product in the field.

3.2.9 Multiple Cyclic Load Histories

The loading histories over the life of a product frequently includes many different use environments and loading conditions [Refs. 38, 39]. Multiple cyclic load histories (e.g., "Cold" temperature fatigue cycles combined with higher temperature creep/fatigue cycles (see Table 1) combined with vibration and local expansion mismatches) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative—this assumption underlies Eqs. 3.1 and 3.2 as well—and that the
simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [Ref. 40] can be applied.

Frequently the initial reliability objective is stated as an allowable net cumulative damage ratio (CDR). The CDR is calculated as the sum of the ratios of the number of occurring load cycles to the fatigue life at each loading condition and is

\[
CDR = \sum_{j=1}^{l} \frac{N_j}{N_fj} < 1 \tag{3.9}
\]

where
\[
N_j = \text{actually applied number of cycles at a specific cyclic load level } j.
\]
\[
N_fj = \text{fatigue life at the same specific cyclic load level } j \text{ alone.}
\]

The fatigue life is frequently not completely specified and is normally taken to be the mean cyclic fatigue life. Equation 3.9 can be used with the allowable CDR significantly less than unity to provide margins of safety, or more accurately, margins of ignorance.

Because the failure of solder joints results from wearout due to fatigue, the failure rate is continuously increasing. This is in stark contrast to the reliability design philosophy of MIL-HDBK-217 [Ref. 41] which presumes a constant failure rate. These increasing failure rates are properly represented by an appropriate statistical failure distribution.

Thus, to assure low failure risks, the fatigue life should be specified at the acceptable cumulative failure probability at the end of the design life as per Eq. 3.8. Thus, Eq. 3.9 is more appropriately written as

\[
CDR(x\%) = \sum_{j=1}^{l} \frac{N_j}{N_fj(x\%)} = 1 \tag{3.10}
\]

where
\[
CDR(x\%) = \text{cumulative damage ratio resulting in a cumulative failure probability of } x\%.
\]
\[
N_fj(x\%) = \text{fatigue life at the cyclic load level } j \text{ and a failure probability of } x\%.
\]

This approach works very well for the design of the solder attachment for a single component. However, it is inadequate for a reliability analysis of a the whole assembly.

3.2.10 System Reliability Evaluation

Equations 3.1 through 3.10 address the reliability of the SM solder attachment of individual components. Systems consist of a variety of different components most of which occur in multiple quantities. Further, as shown in Table 1, many use environments cannot and should not be represented by a single thermal cyclic environment, and accumulating fatigue damage from other sources, such as cyclic thermal environments as described in Caveats 2 to 4 as well as vibration, needs to be included also.

For a multiplicity of components, \(i\), in the system, the effect of the various components on the system reliability can be determined from

\[
F_s(N) = 1 - \exp \left\{ \ln(1 - 0.01x) \sum_{i=1}^{n} \frac{N_{ij}}{\sum_{j=1}^{l} N_{fij}(x\%)} \right\} \tag{3.11}
\]

where
\[
F_s(N) = \text{system cumulative failure probability after } N \text{ total cycles.}
\]
\[
n_i = \text{number of components of type } i.
\]
\[
N_{ij} = \text{actually number of cycles applied to component } i \text{ at a specific cyclic load level } j.
\]
\[
N_{fij}(x\%) = \text{fatigue life of solder attachment of component } i \text{ at load level } j \text{ at } x\% \text{ failure probability.}
\]
\[
\beta_i = \text{Weibull slope for SM solder attachment of component } i.
\]

3.3 DfR-PROCESS

Appropriate DfR-measures to improve reliability can take one of two forms, which are best employed in combination for improved reliability margins. These measures are:

1) CTE-tailoring to reduce the global expansion mismatch;
2) Increasing attachment compliance to
accommodate the global expansion mismatch;

Further, a DfR procedure aiming at high-reliability should also include:

3) Choosing base materials that have not too large a local CTE-mismatch with solder, or

4) In case item (3) cannot be done, reduce the continuous wetted length to reduce interfacial stresses.

CTE-tailoring involves choosing the materials or material combinations of the MLB and/or the components to achieve an optimum ΔCTE. An optimum ΔCTE for active components dissipating power is ~1-3 ppm/°C (depending on the power dissipated) with the MLB having a larger CTE, and 0 ppm/°C for passive components. Of course, since an assembly has a multitude of components, full CTE-optimization cannot be achieved for all components—it needs to be for the components with the largest threat to reliability. For military applications with the requirement of hermetic—and thus ceramic—components, CTE-tailoring has meant the CTE-constraining of the MLBs with such materials as Kevlar™ and graphite fibers, or copper-Invar-copper and copper-molybdenum-copper planes. Such solutions are too expensive for most commercial applications for which glass-epoxy or glass-polyimide are the materials of choice for the MLBs. Thus, CTE-tailoring has to take the form of avoiding larger size components that are either ceramic (CGAs, MCMs), plastic with Alloy 42 leadframes (TSOPs, SMTs [Ref. 26]), or plastic with rigid bonded silicon die (PBGAs).

Increasing attachment compliancy for leadless solder attachments means increasing the solder joint height (C4, C5, shimming, gluing [Refs. 42, 43], 10Sn/90Pb balls, 10Sn/90Pb columns) or switching to a leaded attachment technology. For leaded attachments increasing lead compliancy can mean changing component suppliers to those having lead geometries promoting higher lead compliancy or switching to fine-pitch technology.

The DfR-process needs to emphasize a physics-of-failure perspective without neglecting the statistical distribution of failures. The process might involve the following steps:

A. Identify Reliability Requirements—expected design life and acceptable cumulative failure probability at the end of this design life;

B. Identify Loading Conditions—use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation, which may vary and produce large numbers of mini-cycles (Energy Star);

C. Identify/Select Assembly Architecture—part and substrate selections, material properties (e.g., CTE), and attachment geometry;

D. Assess Reliability—determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here, a 'Figure of Merit'-approach [Ref. 44], or some other suitable technique; this process may be iterative;

E. Balance Performance, Cost and Reliability Requirements.

3.4 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES

The lessons learned over the past 15 years with surface mount technology (SMT) and fine-pitch attachments should be heeded and applied. However, some of the emerging advanced technologies fall outside the previous experience with SMT attachments. It is therefore important that appropriate design validation and qualification tests be carried out to extend and, if necessary, alter and augment, the existing understanding.

Following are short descriptions of some new technologies where DfR, particularly for the solder attachments, is of prime concern.

3.4.1 Flip Chip on Laminate

Here the biggest reliability concern is the large expansion mismatch between the chip silicon and the polymeric substrate. This either means relatively small chips or the use of organic underfill materials which relieve the solder joints from most of the thermal expansion mismatch loads. The underfill material does however make
repairs difficult if not impossible. Detailed information about this technology is being assembled in ANSI/J-STD-012, Implementation of Flip Chip and Chip Scale Technology.

3.4.2 Area Arrays (BGA, CGA)

Grid array components (GACs) come in a variety of styles and materials. The major variations are BGAs, available with plastic bodies as PBGAs or ceramic bodies as CBGAs, and solder attached with either the C5-process or with solder joints containing 105Sn/90Pb solder balls; and CGAs with 105Sn/90Pb solder columns.

The long-term reliability of the solder attachments to FR-4 PCBs is a big concern with GACs. The global thermal mismatch between the GACs and the PCB can be quite large as the result of the combination of large GAC sizes, large differences between the thermal expansion coefficients of the GACs and the PCB (ΔCTE), and the power dissipation within the GACs. Further, depending on the die attach and the GA material, a large localized global thermal expansion mismatch under the die and a not insignificant local thermal expansion mismatch between the solder itself and the GA surface can increase the threat to reliability. In addition, the implementation of the Government-mandated 'Energy Star'-program, the number of thermal cycles could be a multiple of the once-a-day diurnal/on-off cycles.

The solder attachments of GACs vary depending on the loading conditions to which the solder joints are subjected to and the reliability requirements for the product. As mentioned earlier, BGAs are attached with either the C5-process or with 105Sn/90Pb solder balls. The C5-process, similar to the C4- or flip-chip-process, results in solder joints heights that are less controlled and lower (h=400 to 640 μm (~16 to 25 mils)), while the 105Sn/90Pb solder balls typically with diameters of 760 to 890 μm (30 to 35 mils) result in uniform solder joint heights of the same dimension since the 105Sn/90Pb solder has a liquidus temperature significantly above the near-eutectic Sn/Pb solders and does not melt during a typical reflow process. The solder columns, which currently are only used for ceramic GACs, are 105Sn/90Pb columns with lengths of 1.27 to 2.29 mm (50 to 90 mils) that are either cast onto the CGA or are wires soldered to both the CGA and the substrate with near-eutectic Sn/Pb solder. The ratios of fatigue lives, all parameters other than the solder joint height being equal, are CBGA(0.41 mm/16 mils) : CBGA(0.76 mm/30 mils) : CGA(2.29 mm/90 mils) = 1 : 4 : 45. The height of the solder columns is limited by the requirement that the column height-to-diameter aspect ratio does not produce slender columns thus changing the loading conditions; cast columns can accommodate larger aspect ratios.

It is also of importance for PBGAs, how the silicon chips are attached to the BGA body. For 'cavity-up' components, only a thin plastic layer separates the solder joints from the die attach. As a consequence, the CTE underneath a rigid die attach can be as low as 6 to 8 ppm/°C (very similar to ceramic) locally raising the CTE-mismatch between the PBGA and the FR-4 PCB from ~2 to 10 ppm/°C. Thus, the die size can only be ~1/s the size of the BGA to not negatively affect the reliability. Typically, die sizes are significantly larger than that, with the result that the solder joints at the corners of the die fail before the outermost BGA corner joints. The larger the die, the worse the solder attachment reliability [Refs. 45, 46]. Thus, the trend towards Perimeter-PBGAs, where solder joints exist only on the package perimeter—with the possible exception of some thermal solder balls and vias in the package center—for routing reasons, is beneficial for reliability [Ref. 47].

Further, the solder joint fractures are typically near the interface between the BGA and the barrel-shaped solder joints; this is a consequence of the contribution to the solder joint loading of the local expansion mismatch between the solder and the die-constraint BGA body [Ref. 45]. Substantial increases in fatigue life have reported with a soft die attach [Ref. 48].

Of not insignificant influence on the reliability is the geometry of the solder joints as well as the solder pad metallization. Especially the solder masks can have a negative influence if they are used for solder mask-defined (SMD) pads with the solder mask on the metallization pads affecting the solder joint geometries. Stress
concentrations created by the SMD-solder joint geometries can be the origin of solder joint failures and reduced reliability. For equal solder joint height, increases in fatigue life by factors of about 1.25 to 3 can be anticipated with the use of non-solder mask-defined (NSMD) vs. SMD pads with the larger improvements for solder joints with the more severe loading conditions [Refs. 46, 48-51].

For PBGAs the additional reliability issue of via and trace failures has surfaced [Ref. 52]. The former issue is addressed in Section 4 and the latter can be remedied by wider traces and/or better copper foil [Ref. 53].

Detailed information about this technology is being assembled in ANSI/J-STD-013, Implementation of Ball Grid Array and Other High Density Technology.

3.4.3 Thin Packages (TSOP)
The biggest reliability issue regarding TSOPs (Thin Small Outline Packages) stems from the choice of Alloy 42 for the leadframe material by some component manufacturers [Refs. 27-31]. This material choice has the following consequences with regard to the solder attachment reliability:

1. Increases global CTE-mismatch, because component CTE is reduced to about the CTE of ceramic;
2. Increases lead stiffness due to higher modulus of elasticity reducing the effectiveness of the leads to protect the solder joints from expansion mismatches;
3. Reduces solder joint strength because of weaker solder/Alloy 42 interfacial bond (see Section 3.2.3);
4. Reduces solderability (see Section 3.2.4).

These potential reliability threats can be avoided with the choice of a copper lead frame; however, this requires a soft die attach and the reversion to higher CTE molding compounds for the components [Ref. 31].

3.5 VALIDATION AND QUALIFICATION TESTS
The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability

Testing of Surface Mount Solder Attachments.

However, for large components with significant heat dissipation and small global CTE-mismatches, temperature cycling tests are inadequate to provide the required information; full functional cycling—including external temperature and internal power cycling—is necessary.

3.6 SCREENING PROCEDURES

3.6.1 Solder Joint Defects
The solder joint defects of greatest reliability concern are those involving inadequate wetting for whatever reason. Well wetted solder joints, regardless of their geometric variations within the standards provided by IPC-A-620, Acceptability of Electronic Assemblies with Surface Mount Technologies and ANSI/J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies, and somewhat beyond, will not pose a reliability threat due to inadequate quality. In Figure 3 the results of thermal cycling and thermal shock tests are shown for solder joints of chip components with a wide variety of component offsets and overhangs.

Those solder joints have adequate strength even for severe mechanical loading conditions as well as no diminished thermal cyclic fatigue reliability. Only with severe offsets beyond Class 2 requirements is the reliability diminished. However, solder joints not properly wetted, can prematurely fail both as the result of mechanical and thermal cyclic loading [Refs. 1, 31].

Voids in the solder joints are generally regarded as not constituting a reliability threat [Ref. 48]. Possible exceptions are large voids reducing the solder joint cross-section enough to reduce a required thermal heat transfer function, and voids in high-frequency applications where the voids can cause signal deterioration.

3.6.2 Screening Recommendations
Effective screening procedures need to be capable of causing the failure of latent solder joint defects, i.e., weak inadequately wetted solder joints, without causing significant damage to high quality solder joints.
Figure 3 - Effect of Component Offsets on the Fatigue Reliability of Three Capacitor Chip (CC) Sizes with −55°C/+125°C Thermal Shock or −20°C/+100°C Thermal Cycling (TC) and Either Wave (W) or Reflow Soldered (R) [Ref. 54, 55]. The Lower Lives at Smaller Component Offsets Result from the Failure of the CC-Components not the Solder Joints. The Fatigue Lives are Normalized, Since the Data are from Glued-Down CCs which Typically Exhibit Longer Solder Joint Fatigue Lives than CCs not Glued-Down.

The best recommendation is random vibration (6-10 grms for 10-20 minutes), preferably at low temperature, e.g., −40°C. This loading does not damage good solder joints, but overstresses weakly bonded ones [Ref. 1].

Thermal shock can also be successfully used, however some damage to good solder joints can be expected, particularly for larger components.

4. PLATED-THROUGH VIA (PTV) STRUCTURES

4.1. PTV RELIABILITY ISSUES

Plated-through-holes (PTHs) serve to electrically connect different conductor layers in multilayer printed circuit boards (MLBs). In conventional interconnection technology employing through-mounted components, the PTHs also serve the function of providing a structure that accepts the component leads and to which these leads can securely be solder attached. This structure consisting of the copper PTH barrel containing a component lead and filled with solder provides a very robust, multiple-redundant electrical and mechanical connection between the component and the MLB.

The continuing drive towards higher functionality, higher density, and lower weight was brought about and made possible by the development of surface mounted technology. This reduced the purpose of the previously multi-functional PTHs to
providing only the electrical interconnections between the MLB layers and the diameters of PTHs could be reduced, since they no longer needed to be large enough for the component lead insertion operation. To distinguish the two types of PTHs, the PTHs without component leads are frequently referred to as 'PTH-vias' or PTVs. At the same time, the increased functionality and density of the components often brought about a need to increase the number of layers in MLBs, and thus to increase the MLB thickness.

The decreasing PTV diameters, particularly in combination with the increasing MLB thicknesses, make copper plating into the PTVs more difficult. This problem was first recognized during an IPC round robin study [Ref. 56], which led to a more detailed round robin study specifically focused on this issue [Ref. 57]. PTVs having a small diameter—less than -0.5 mm (-0.020 inch)—and/or a high aspect ratio of MLB thickness to drilled PTV diameter—more than 4—were found to require special treatment for adequate reliability.

During this study the material properties, processing parameters, and environmental test and use conditions important for the reliability of PTVs were identified. The results of these studies together with prior and subsequent work [Refs. 58-64] has been utilized to develop a practical methodology to aid in the DFR of PTVs, as well as to permit the assessment of the reliability of PTVs given the assembly and test procedures and the use environments in the field [Ref. 65].

In the IPC round robin test program [Ref. 56] the IEC test—designed to simulate solder reflow thermal shock cycles—was used to evaluate the reliability of small-diameter PTVs. It was found that assembly processes involving large temperature excursions constitute a significant reliability threat due to low-cycle fatigue for PTV copper barrels with low ductility or large stress concentrations. It was concluded that failures, to the extent they occur at all, occur typically in the first 10 cycles due to overstress crack initiation followed by crack propagation. This conclusion was reinforced by the findings of Oien [Refs. 58, 59], which showed that crack initiation occurs during the first or second cycle. Unless failure occurs within 10 cycles of the overstress loading typical of solder reflow, solder reflow over-stressing is not a problem. Additional cycles will eventually lead to fatigue-induced failures. The failures that occurred in the IPC study were observed in product from vendors rated 'poor' to 'good' on an arbitrarily subjective scale with some consistency in differentiation. No 'superior'-rated vendor product failed. This led to the definition of a numerical quality index that is now utilized in an improved more detailed vendor reliability modeling shown in Section 4.2 [Ref. 65].

During the product use, the severity of the thermal use environment has a great impact on the reliability of the PTVs. The MIL-T and COM-T thermal cycling tests [Ref. 57] were designed to simulate severe and relatively benign use environments, respectively. While failures in the MIL-T test occurred depending on the construction of the MLBs and the quality of the PTVs, failures did not occur as the result of the COM-T test. It needs to be noted however, that the MIL-T and COM-T thermal cycling tests unfortunately had arbitrary test cutoffs at 400 and 1000 cycles, respectively.

4.1.1 Copper Plating Processes

4.1.1.1 Acid Copper Plating

One finding of the IPC round robin study [Ref. 57] was that PTVs with aspect ratios larger than three and plated with standard electrolytic acid copper show decreasing thermal cyclic fatigue life. It was found that the copper plating process window narrows as the PTV aspect ratio increases and that the standard electrolytic plating processes become inadequate even with optimum process controls. These findings agree with earlier studies investigating the effects of plating current density and agitation level on copper deposit quality in PTVs [Ref. 60]. In this study it was shown that inadequate electrolyte replacement rates, which can clearly occur in high-aspect-ratio PTVs, will lead to mass-transport-limited plating conditions. Under these conditions, in combination with the non-uniform plating current densities that also get worse with increasing aspect ratios, the copper deposit quality rapidly deteriorates with increasing aspect ratios. The resulting copper deposits within the
PTV can have significantly lower ductility and strength than the copper deposits plated at the same time external to the PTVs, e.g., on plating mandrels. The decline in physical properties is frequently accompanied by increased ‘dog-boning’ and nodule formation as well [Ref. 65].

The copper deposits from standard acid copper baths in high-aspect-ratio PTVs, even with uniform plating in the PTV barrels and good intrinsic tensile properties, as determined by testing foil specimens from flat plating mandrels, perform only marginally in thermal cycling tests. For this reason, special plating solutions have been developed, that allow reduced plating current densities at the expense of increased plating times, but producing significantly improved PTV copper barrel reliability.

4.1.1.2 Pyrophosphate Copper Plating
Pyrophosphate plated copper was unfortunately not part of the IPC round robin studies [Refs. 56, 57]. It has however been shown, that pyrophosphate copper is less susceptible to the effects of non-uniform plating current densities and higher PTV aspect ratios.

4.1.2 Material Properties

4.1.2.1 Tensile Properties
The tensile properties of the PTV copper deposits are very important, both for the performance of the PTVs during subsequent processing and use, and for the DR for the PTVs. The properties that are needed are: (1) the tensile strength, (2) the yield strength, (3) the modulus of elasticity, (4) the modulus of plasticity, and (5) the fracture ductility.

It has also been found, that the electrolytically plated copper deposits have a modulus of elasticity significantly below that of cast and rolled copper reported in material property references. It therefore is necessary to measure the modulus of elasticity, which can be done during the tests to determine the yield and tensile strengths of the deposits.

The tensile strength, the yield strength, the modulus of elasticity and the modulus of plasticity can be determined from tensile tests. To properly determine the modulus of elasticity, the ‘interrupted tensile test’ method should be utilized.

It needs to be noted however, that these tensile properties come from samples plated onto flat stainless steel mandrels and only set the upper bounds for the strength and ductility of the copper deposit inside the PTV. The evidence is circumstantial, but very strong, that these properties are significantly degraded inside of high-aspect-ratio (board thickness/PTV-diameter) PTVs [Ref. 57].

4.1.2.2 Ductility
The tensile elongation for foil specimens is a very inaccurate and subjective test for foil samples because of the specimen geometry and the dependence on the test conditions [Ref. 65, 66]. Tensile elongation for foil materials is adequate for quality control and comparison purposes, but it significantly underestimates the fracture ductility of the material by about a factor of three (3) and gives the false indication of a ductility dependence on foil thickness.

It is for these reasons that the test cited in References 67 and 68 was developed. This test has a high discrimination power in terms of quality variations of the copper deposit, thus being very valuable as a process control tool as well as providing direct input for the all-important ductility of the copper deposit.

In order to assess the quality of the plated copper deposits, foil samples plated onto mandrels need to be subjected to fatigue ductility testing [Ref. 67].

It needs to be noted however, that this ductility comes from samples plated onto flat stainless steel mandrels and only set the upper bounds for the ductility of the copper deposit inside the PTV. The evidence is circumstantial, but very strong, that this property is significantly degraded inside of high-aspect-ratio (board thickness/PTV-diameter) PTVs [Ref. 57].

The ductility of the copper deposit in the PTV barrel can be determined from the performance of the PTVs in accelerated testing resulting in low-cycle fatigue. In Table 3 the results from two of the tests used in the Reference 57 applied to coupons from the same sample are given together with the stresses and strain ranges resulting
from the thermal cycling/shock excursions. Also given is the minimum ductility initial tensile strength resulting from the first failures in the tests.

Table 3. Estimates of Tensile Properties of Copper Deposit Inside the PTVs.

<table>
<thead>
<tr>
<th>Test</th>
<th>$\Delta T$ [$^\circ$C]</th>
<th>Fatigue Life $N_f$ [cycles]</th>
<th>Barrel Stress $\sigma$ [MPa/ksi]</th>
<th>Strain Range $\Delta\varepsilon_{\text{max}}$ (eff) [%]</th>
<th>Copper Strength $S_u$ [MPa/ksi]</th>
<th>Minimum Ductility $D_f$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC Hot Oil Thermal Shock</td>
<td>235</td>
<td>32</td>
<td>219/31.8</td>
<td>4.5</td>
<td>281/40.7</td>
<td>20.6</td>
</tr>
<tr>
<td>Temperature Cycling/Shock</td>
<td>190</td>
<td>150</td>
<td>177/25.7</td>
<td>2.2</td>
<td>281/40.7</td>
<td>23.3</td>
</tr>
</tbody>
</table>

The measured mandrel ductility was about 30%. Thus, the ductility in the PTV barrels as given in Table 3 indicates a significantly lower deposit ductility as compared to the ductility of the deposit on the MLB surface.

4.1.2.3 Fatigue Behavior

It has been found that annealed electrolytic acid copper strain-hardens upon the application of cyclic strain loads during fatigue tests [Ref. 66]. This results in high-cycle fatigue lives that are longer than expected based on the initial material properties.

Conversely, annealed pyro-phosphate-plated copper strain-softens as the result of the application of the cyclic strains during the fatigue testing. Therefore, fatigue life tests in the high-cycle regime as per Reference 67 need to be performed in order to obtain an indication of the changes in the material properties from either strain hardening or softening during high-cycle fatigue. By using larger bend mandrel diameters than are used for

![Figure 4 - Cross-Section Schematic of a PTV With a Barrel Fracture Near the Center of the MLB.](image-url)
the fatigue ductility test, the samples are subjected to high-cycle fatigue to assess the material behavior of the copper plating under extended fatigue loading.

4.13 Damage Mechanisms and Failure

4.13.1 PTV Quality
The quality of the PTVs, together with the severity of the thermal expansion loading, is the critical aspect in the reliability of PTVs.

Even good quality PTVs will eventually fail and will typically do so as the result of a PTV barrel fracture near the center of the barrel as is illustrated in Fig. 4. PTV failures can also occur as the result of PTV shoulder fractures (see Fig. 5) and internal land fractures. Failures of these types typically are the consequence of an inadequate material choice for the vendor copper foils [Ref. 53] used for the laminates or some processing error.

The most typical failure mode, however, is the fracture of the PTV copper barrel, which is the primary subject here.

In Section 4.2 on reliability modeling, an attempt is made to distinguish between three different quality aspects of PTVs. One of these is related to the quality of the PTV walls as the result of the drilling and desmear processes, and two to the plating quality in terms of the plating uniformity—'dog-boning'—and the reduced material properties in the center of the PTV.

4.13.2 Impact of Assembly Processes and ESS Procedures
The most severe stress condition and threat to reliability for PTVs takes place during the solder reflow processes necessary to make circuit board assemblies. Because of the large differences in the CTEs for the copper and the MLB resin, the larger the temperature excursions the larger is the resulting thermal expansion mismatch causing stresses in the PTV copper barrel and shoulders.

The large temperature excursions during the soldering and solder reflow processes combine with the difference in the CTE between the glass-reinforced epoxy layers surrounding the PTV and the plated copper of the PTV barrel to create tensile stresses.
in the copper barrel and bending stresses at
the PTV shoulder due to the PTV land
rotating as a result of the large z-direction
(the direction perpendicular to the plane of
the MLB) expansion of the epoxy. The CTE of
FR-4 in the z-direction is typically 38-97
ppm/°C below the glass transition
temperature, Tg, and 186-349 ppm/°C above
Tg [Refs. 69-74], whereas electrodeposited
copper foils have a CTE of about 17±2
µin./°C.

Of the about ΔT=180°C thermal excursion
during the soldering process, about
ΔT=100°C is below Tg at a mismatch in the
CTEs of Δα=20-69 ppm/°C, whereas about
ΔT=80°C is above Tg at a mismatch in the
CTEs of Δα=16-33 ppm/°C. This results,
for a 1.58-mm (62 mil)-thick MLB, in an
expansion mismatch between -25 and 53 µm
(-1.0 and 2.1 mils), providing the severe
loading conditions that can lead to fractures
in the PTV barrels or shoulders as well as
the cracking of inner copper layers near the
MLB surface.

Environmental Stress Screening (ESS)
procedures, in order to be effective, need to
resemble solder reflow excursions in their
severity. Therefore, ESS cycles have a

4.2 RELIABILITY PREDICTION MODELING

The fatigue behavior of metals can be described by [Refs. 75, 76]

\[
N_f^{-0.6}D_f^{0.75} + 0.9S_u\frac{\exp(D_f)}{E} - \Delta \varepsilon = 0
\]

(4.1)

where

- \(N_f\) = mean fatigue life, cycles-to-failure,
- \(D_f\) = fracture ductility, plastic strain at
  fracture, of the PTV copper deposit,
- \(S_u\) = tensile strength of the PTV copper
  deposit,
- \(E\) = modulus of elasticity of the PTV
  copper deposit,
- \(\Delta \varepsilon\) = total cyclic strain range.

The relationships underlying Equation 4.1
were developed to be able to predict the
fatigue life from tensile properties and
brought about a unified ductility-dependent
low-cycle fatigue and strength-dependent
high-cycle fatigue [Ref. 14] approach.
Equation 4.1 has been used for some major
study programs [Refs. 57, 66, 77] and the
development of test methods [Refs. 67, 68].

The full determination of the stresses and
similar impact as do solder reflow
excursions.

It is during these excursions to solder
reflow temperatures during solder reflow
operations or ESS procedures that PTV
barrel cracks can initiate due to overstressing
and subsequent thermal
excursions serve to propagate such cracks
to complete separation and failure.

4.1.3.3 Impact of Test Procedures and
Cyclic Operating Environments

During cyclic temperature testing and
operational use of the product, cyclic
thermal excursions can also lead to
fractures and failure due to cyclically
accumulating fatigue damage. The severity
of the fatigue damage is dependent on the
severity of the operational environment of
the application. In Table 1 guidelines as to
the possible use environments for nine of
the more common electronic applications
are illustrated [Ref. 9]. The fatigue damage
caused first by the thermal excursions
during processing and assembly, then by
cyclic temperature testing, and finally
during product use is cumulative and needs
to be accounted for in a reliability analysis.
\[ \sigma_{\text{avg}} = \frac{(\alpha_E - \alpha_{Cu}) \Delta T A_E E_{Cu}}{A_E E_{Cu} + A_{Cu} E_{Cu}}, \quad \text{for } \sigma_{\text{avg}} \leq S_y \]  

(4.2)

or

\[ \sigma_{\text{avg}} = \frac{(\alpha_E - \alpha_{Cu}) \Delta T + S_y \frac{E_{Cu}'}{E_{Cu}}}{A_E E_{Cu} + A_{Cu} E_{Cu}'} \]  

(4.3)

where

\[ A_E = \frac{\pi}{4} \left[ d^2 + d'^2 \right] \]  

(4.4)

and

\[ A_{Cu} = \frac{\pi}{4} \left[ d^2 - (d - 2t)^2 \right] \]  

(4.5)

and

\[ \sigma_{\text{avg}} = \text{PTV barrel stress}; \]

\[ S_y = \text{PTV barrel copper yield strength, typically } -172 \text{ MPa (25 ksi)}; \]

\[ \alpha_E = CTE \text{ of MLB in thickness direction, for excursions above } T_g \text{ the larger CTE at those temperatures needs to be considered, typically } -65 \text{ ppm/°C } \theta < T_g, -315 \text{ ppm/°C } \theta > T_g; \]

\[ \alpha_{Cu} = CTE \text{ of copper, typically } -18 \text{ ppm/°C}; \]

\[ \Delta T = \text{temperature range of thermal cycling}; \]

\[ A_E = \text{area of loading influence of MLB}; \]

\[ A_{Cu} = \text{area of PTV barrel}; \]

\[ E_E = \text{modulus of elasticity of epoxy, typically } -3.5 \text{ GPa (0.5x10^6 psi)}; \]

\[ E_{Cu} = \text{modulus of elasticity of PTV copper, typically } -83 \text{ GPa (12x10^6 psi)} \text{ for acid-plated copper and } -35 \text{ GPa (5x10^6 psi)} \text{ for pyrophosphate-plated copper}; \]

\[ E_{Cu}' = \text{modulus of plasticity of PTV copper, typically } -0.7 \text{ GPa (0.1x10^6 psi)}; \]

\[ t = \text{thickness of MLB}; \]

\[ d = \text{drilled PTV diameter}; \]

\[ d_E = \text{diameter of MLB dielectric surrounding the PTV and influencing the PTV loading}; \]

\[ t = \text{thickness of copper deposit in PTV barrel}. \]

The average strains in the PTV barrel are determined from

\[ \Delta e_{\text{avg}} = \frac{(\alpha_E - \alpha_{Cu}) \Delta T A_E E_{Cu}}{A_E E_{Cu} + A_{Cu} E_{Cu}}, \quad \text{for } \sigma_{\text{avg}} \leq S_y \]  

(4.6)

and

\[ \Delta e_{\text{avg}} = \frac{(\alpha_E - \alpha_{Cu}) \Delta T A_E E_{Cu} - S_y A_{Cu} E_{Cu}}{A_E E_{Cu} + A_{Cu} E_{Cu}'}, \quad \text{for } \sigma_{\text{avg}} > S_y \]  

(4.7)

where \( \Delta e_{\text{avg}} \) = the cyclic strain range during thermal cycling.

The diameter of MLB dielectric material surrounding a PTV and influencing the PTV loading, \( d_E \), is a measure of the stiffness of the MLB structure surrounding the PTV barrel. The degree of land rotation—and thus lower stiffness—and any other stiffening structures, such as reinforcement weave, neighboring PTVs, components and cooling plates, will have an impact on this stiffness. For bare MLBs it was found that \( d_E \) could vary from a relatively small diameter of influence [Ref. 65]

\[ d_E \equiv 2h \]  

(4.9)

for PTVs in MLB assemblies for which land rotation is essentially prevented by large stiff components and heat sink plates; the most probable representative value for bare MLBs is [Ref. 65]

\[ d_E \equiv \frac{h}{2} + 2d \]  

(4.10)

It has been found [Refs. 57, 62, 65] that the average barrel strains, \( \Delta e_{\text{avg}} \), thus calculated need to undergo a correction for the assumptions necessary for a closed form stress and strain analyses. Further, stress concentrations can occur due to the uneven PTV barrel geometries resulting from inadequate drilling and/or plating.

\[ d_E \equiv 3d \]  

(4.8)
processes. In addition, localized differences in the resin content (B-stage layers) and the influence of inner lands and power and ground planes can cause non-uniformities in the stresses and strains, and at temperatures above $T_g$, the material properties of the polymeric dielectric materials change dramatically and abruptly [Ref. 65].

Furthermore, PTV failures, as all failures due to wearout mechanisms, have a statistical distribution. The available data are not adequate to fully define a statistical distribution, but wearout mechanisms like fatigue typically follow a Weibull distribution with a shape parameter or slope of $\beta = 3$.

Typical data are reported as the first failure from a number of daisy chains with upwards of 100 PTVs each.

An effective maximum strain range to be used in Eq. 4.1 can be found from

$$\Delta \varepsilon_{max}^{(eff)} = K_{eff} \Delta \varepsilon_{avg}$$

(4.11)

where $K_{eff}$, the effective PTV strain coefficient, results from a combination of discernible deviations from a uniform stress and strain distribution, such that

$$K_{eff} = K_d K_h \left( \frac{100}{K_c K_Q} \frac{10}{200 - T_g} \right)$$

(4.12)

The coefficients in Eq. 4.12 are the PTV strain distribution factor, $K_d$, the plating thickness 'dog-boning' coefficient, $K_h$, the PTV stress concentration factor, $K_c$, and the PTV plating quality index, $K_Q$. Initially, the last three coefficients had been combined in a general PTV quality index [Ref. 57], but by separating the discernible quality variations, the source of the reduced quality can be identified and the impact less arbitrarily quantified. As a guideline it should be noted that the values for $K_{eff}$ in Reference 57 varied between about 1.2 and 10.

The PTV strain distribution factor, $K_d$, corrects for the model assumption of a uniform stress and strain distribution for a distribution that is in fact non-uniform. The non-uniformity is a function of the MLB thickness, $h$, with higher non-

uniformities resulting from thicker MLBs. The PTV strain distribution factor is also dependent on whether or not the temperature excursions exceed $T_g$, above which not only the thermal expansion increases, but the materials softens significantly. Thus, the plating thickness 'dog-boning' coefficient, $K_h$, accounts for any non-uniform stress and strain distribution in the PTV barrel due to the gradual thinning—

$$K_h = \begin{cases} 1 & , \text{ } T_{max} > 200^\circ \text{C} \text{ and } T_g \\ 1 + 1.5 \left( \frac{h}{0.090 \text{ in}} \right)^3 \frac{T_{max} - T_g}{200 - T_g} & , \text{ } T_{max} > T_g \\ 1 + 1.5 \left( \frac{h}{0.090 \text{ in}} \right)^3 & , \text{ } \text{otherwise} \end{cases}$$

(4.13)

'dog-boning'—of the copper deposit towards the barrel center. This 'dog-boning' can result from plating conditions that are slightly beyond the capability of the plating chemistry used. The coefficient is given by [Ref. 65]

$$K_h = \frac{t_{PTV \text{ shoulder}}}{t_{PTV \text{ center}}}$$

(4.14)

The PTV stress concentration factor, $K_c$, is a measure of the stress concentrations caused by the localized abrupt thinning of the copper deposit due to either drilling or plating defects. Its size may be taken from Figure 6 using the plating deposit narrowing to determine the local 'reduction in cross-section'.

Figure 6 contains a curve [Ref. 65] which quantifies the large impact stress concentrations due to localized thinning of plated copper conductors on flexible printed wiring have on increasing the stress—and thus the strain—locally. PTV copper barrels, however, due to their three-dimensional geometric structure are less susceptible to stress concentrations that occur as localized features visible on two-dimensional cross-sections. Figure 6 also contains a curve which is an attempt to quantify the impact of these localized stress concentrations, which do not affect the whole PTV barrel cross-section, in terms of
the portion of the basic material ductility that is required to accommodate these stress concentrations. From Figure 6 a localized reduction in plating thickness by 50% would result in a value for $K_c$ of about 82, raising the effective strain due to the stress concentration by about a factor of 1.22.

The PTV plating quality index, $K_Q$, is on a 10-to-1 scale with 10 being perfect, and is a measure of the quality of the plated copper deposit in terms of its material properties relative to those of a corresponding foil sample plated onto a plating mandrel. This index needs to be established by experience with PTVs in coupons or MLBs fatigued to failure.

4.3 DfR-PROCESS

A successful ‘Design for Reliability’-process requires that a number of issues be addressed at the design stage. The generally applicable guidelines for the DfR-process are:

1) Keep PTV diameters as large as possible and the MLB thickness/PTV diameter aspect ratio as small as possible;
2) Require a nominal copper deposit thickness of 1.2 mils (30 μm) to obtain actual plating thicknesses in the range of 1.0 to 1.5 mils (25 to 38 μm);
3) Use E3 copper foil for the signal, power, and ground layers for aspect ratios larger than 3:1;
4) Tent PTVs for applications with severe operational loading conditions (see Tables 1 and 4) with solder mask to prevent solder from partially filling the PTVs and causing stress concentrations.

It is much more difficult to plate consistent high quality copper deposits into small diameter PTVs using standard electrolytic processes. Also, smaller diameter PTV barrels, especially in thicker MLBs, are subjected to higher loading conditions.

A plating thickness of ~25 μm (~1.0 mils) has been found the minimum thickness to give good reliability; a plating thickness of ~38 μm (~1.5 mils) is optimum from a reliability perspective. Plating thicknesses greater than that tend to promote shoulder fractures (see Fig. 5).

The quality of the copper foil for the signal, power, and ground layers is of importance for aspect ratios larger than about 3:1.
Standard E1 copper foil [Ref. 53] has a coarse columnar grain structure with the grain boundaries perpendicular to the foil surfaces and has an elongation requirement of only 2%. Thus, brittle E1 vendor foil can lead to signal layer fractures and shoulder cracks as illustrated in Figure 5. ‘High Temperature Elongation'-E3 copper foil is recommended for PTVs with aspect ratios larger than about 3:1.

Tenting the PTVs is a prudent and pragmatic decision. PTVs entirely filled with solder certainly are more robust and reliable than PTVs without solder, the problem is that it cannot be guaranteed, that all the PTVs will be entirely filled with solder. Partially solder-filled PTVs have stress concentrations where the transition from fully filled to partially filled occurs; these stress concentrations reduce the reliability of these PTVs significantly. Therefore, it is best to avoid the possibility of these stress concentrations all together by tenting the PTVs. However, it needs to be emphasized, that this issue is important only for severe use conditions with temperature cycles of about ΔT≥50°C, as can be seen in Table 4.

In Table 3 in Section 4.1.2.2 the minimum fatigue ductilities resulting from two accelerated fatigue tests of PTVs in MLBS are given. These estimates of the copper deposit properties in the PTV barrels are used in Table 4 to estimate the minimum fatigue lives for a number of typical electronic use environments. The fatigue lives are given together with the pertinent information on the use conditions and the resulting stresses and strains.

The results in Table 4 indicate that the PTVs of good quality do not constitute a reliability threat to most product applications in the field. Only for the more severe use environments would premature failures be anticipated. However, the results in Table 4 would change drastically for PTVs of low quality.

Table 4. Estimates of the Fatigue Life and Time to Failure of PTVs in Some Typical Use Environments from Table 1.

<table>
<thead>
<tr>
<th>Use Environment</th>
<th>ΔT [°C]</th>
<th>Estimated Maximum Annual Cycles</th>
<th>Barrel Stress σ [MPa/ksi]</th>
<th>Strain Range Δε [%]</th>
<th>Effective Strain Range Δεmax (eff) [%]</th>
<th>Minimum Fatigue Life [cycles]</th>
<th>Estimated Time to First Failure [years]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Computers</td>
<td>20</td>
<td>1460</td>
<td>67/9.7</td>
<td>0.08</td>
<td>0.20</td>
<td>8.0x10⁶</td>
<td>5 500</td>
</tr>
<tr>
<td>Telecomm</td>
<td>35</td>
<td>365</td>
<td>117/16.9</td>
<td>0.14</td>
<td>0.35</td>
<td>75 000</td>
<td>205</td>
</tr>
<tr>
<td>Industrial</td>
<td>60</td>
<td>250</td>
<td>173/25.1</td>
<td>0.28</td>
<td>0.71</td>
<td>2 900</td>
<td>12</td>
</tr>
<tr>
<td>Automotive</td>
<td>80</td>
<td>365</td>
<td>174/25.2</td>
<td>0.38</td>
<td>0.95</td>
<td>1 200</td>
<td>3.3</td>
</tr>
</tbody>
</table>

The DfR-process needs to emphasize a physics-of-failure approach. The process might involve the following steps:

A. Identify Reliability Requirements—expected design life and acceptable cumulative failure probability at the end of this design life;
B. Identify Loading Conditions—use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation;
C. Identify/Select Assembly Architecture—substrate selections, material properties (e.g., CTE). PTV diameter. aspect ratio;
D. Assess Reliability—

determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here; this process may be iterative;
E. Balance Performance, Cost and Reliability Requirements.

4.4 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES

The emerging advanced technologies are characterized by denser packaging resulting in ever smaller structures. Thus, the temptation exists to drive the PTV diameters even smaller and the aspect ratios higher. The DfR principles detailed in
Section 4.3 need to be kept in mind in the design and application of these emerging technologies.

4.5 VALIDATION AND QUALIFICATION TESTS

Validation and qualification tests have not been established for PTVs. However, the test procedures used in the IPC round robin program reported in IPC-TR-579, Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards [Ref. 57], could be utilized for this purpose.

Efforts are underway within the IPC via a round robin test program to establish both qualitative and quantitative correlation for a number of promising test methods.

4.6 SCREENING PROCEDURES

The crucial task is the elimination of the MLBs with thin-plated PTVs without significantly affecting the remainder of the MLBs. The fact that the defects not only involve very thin plating (<10 μm (0.4 mils)), but occur in conjunction with substantial stress/strain concentrations, makes this task possible.

An Environmental Stress Screening (ESS) could employ the same test setup as the Hot Oil Test (IEC Specification 362-2, Test C) [Ref. 57], for three (3) to five (5) cycles. Thus, together with the solder reflow operations necessary for production, the MLBs would experience between eight (8) to ten (10) such temperature excursions.

Given the result, based in standard IEC test criteria, that the life under these loading conditions is 32 cycles, this would consume between 25 and 30% of the MLBs lives. Considering the results in Table 4, that still would leave adequate life for most use environments.

5. INSULATION RESISTANCE

5.1 DAMAGE MECHANISMS AND FAILURE

The damage mechanisms work generally in two distinct regions: at the surface and in the bulk of the electronic assemblies, particularly the printed wiring board (PWB). It has been reported, that surface and bulk phenomena exhibit different time constants in the response to temperature changes [Ref. 79]. The insulation resistance for a sample circuit is the measured integrated effect of both surface and volume resistivity as defined by ASTM [Ref. 80]. The measured bulk resistance will depend upon the nature of the laminate, solder mask and/or conformal coating under investigation. It will also depend upon the degree of cure of the polymers and for PWBs on the quality of the drilling process for the plated-through holes (PTHs) and vias (PTVs), and will be affected by soldering flux/paste residues if they dissolve into the polymeric material during the soldering and/or cleaning processes.

Insulation resistance measurements provide important data in the characterization of PWB laminates, multi-layer boards (MLBs), soldering fluxes, solder masks, and conformal coatings. Such measurements have been used to study the effect of aging at accelerated conditions (temperature, humidity and/or bias voltage) to determine any detrimental effects on the reliability of the product.

Ohm's law states that the magnitude of the current, \( I \), flowing through a circuit with a given resistance, \( R \), is a linear function of the applied voltage, \( V \), such that

\[
V = IR
\]

(5.1)

The resistance is an extrinsic property of the material sample dependent on the resistivity of the material and the geometry of the sample. The resistivity, \( \rho \), of a material is an intrinsic material property. The resistivity is determined from the length, \( l \), of the sample and its cross-sectional area, \( A \), and is related to \( R \) by

\[
\rho = \frac{RA}{l}
\]

(5.2)

Resistivity that measures the resistance to current flow through the bulk of a sample it termed volume resistivity, \( \rho_v \).

\[
\rho_v = \frac{RA}{t}
\]

(5.3)

where \( t \) is the thickness of the bulk sample.

Surface resistivity, \( \rho_s \), measures the ability
of an insulator to resist the flow of current on its surface, such that

$$\rho_s = R \frac{A_s}{l}$$  \hspace{1cm} (5.4)$$

where $A_s$ is the surface area and $l$ is the length of the insulating strip.

### 5.1.1 Surface Insulation Resistance (SIR)

Surface insulation resistance (SIR) measurements will depend on the nature of the surface contamination and the amount of moisture present during the measurement. Although SIR readings are a combination of both bulk and surface resistance, 99.9% of the current leakage for FR-4 epoxy/glass laminate will occur on the surface of the laminate, since the ratio of the surface resistivity to the volume resistivity is 1:1000 [Ref. 81]. Test patterns for measuring volume resistance will either use electrodes on the top and bottom of the substrate (for z-axis measurements) or PTVs to PTN-patterns for measuring the x, y-resistance. SIR patterns are typically interdigitated comb patterns such as the IPC-B-24 coupon.

### 5.1.2 Electrochemical Corrosion

Electrochemical corrosion of metallic conductors and the migration of metal ions between anode and cathode on a PWB can lead to circuit failure. It is important to understand the cause of these failures in order to select materials and processes for PWB manufacture, soldering, and cleaning which will minimize the occurrence of these failures. The tendency of the metal conductor to migrate under a bias voltage in humid conditions has been shown to decrease across the following series of metals [Ref. 82]

$$\text{Ag} > \text{Pb} > \text{Solder} > \text{Cu}$$  \hspace{1cm} (5.5)

Those metals whose hydroxides are more soluble at pH 7-9 have a higher migration rate. This is related to the pH gradient between the anode and cathode when a film of moisture is present.

In the case of SIR testing, the cathode is connected to the high voltage source while the anode is connected to ground. For electrochemical migration to occur, the pathway must exist for ions to move from the anode to the cathode. In the presence of moisture, the following electrochemical reactions can occur at the anode:

$$\begin{align*}
\text{H}_2\text{O} & \rightarrow \frac{1}{2}\text{O}_2 + 2\text{e}^- \\
\text{Cu} & \rightarrow \text{Cu}^{+1} + \text{e}^- \\
\text{Cu} & \rightarrow \text{Cu}^{+2} + 2\text{e}^- \\
\text{Pb} & \rightarrow \text{Pb}^{+2} + 2\text{e}^- \\
\text{Sn} & \rightarrow \text{Sn}^{+2} + 2\text{e}^- \\
\text{Sn} & \rightarrow \text{Sn}^{+4} + 4\text{e}^-
\end{align*}$$  \hspace{1cm} (5.6)

The preferred species in the case of copper will depend on the anion that is present. In water Cu$^{+2}$ is the preferred species except when Cl$^-$ is present. In this case the formation of CuCl$^2-$ will favor the formation of Cu$^+$ rather than Cu$^{+2}$ [Ref. 83]. At the cathode the possible reactions are

$$\begin{align*}
\frac{1}{2}\text{O}_2 + \text{H}_2\text{O} + 2\text{e}^- & \rightarrow 2\text{OH}^- \\
2\text{H}_2\text{O} + 2\text{e}^- & \rightarrow 2\text{OH}^- + \text{H}_2 \\
\text{Cu}^{+2} + 2\text{e}^- & \rightarrow \text{Cu} \\
\text{Pb}^{+2} + 2\text{e}^- & \rightarrow \text{Pb} \\
\text{Sn}^{+2} + 2\text{e}^- & \rightarrow \text{Sn}
\end{align*}$$  \hspace{1cm} (5.7)

### 5.1.3 Dendrite Growth

In normal electrochemical dendritic growth, electrolytic dissolution of the metals occurs at the anode and reduction of the metal ions by plating out occurs at the cathode. Typical dendrites associated with a solder-coated copper comb pattern will be lead-needles with some tin. These appear as "tree-like" dendrites which begin at the cathode. As these surface dendrites grow, their effect on the total SIR reading is minimal until they are very close to the anode. At the point of bridging, the dendrite will burn out quickly due to the high current density. For this reason, the presence of dendrites is not easily determined by the electrical SIR readings. These readings are not taken frequently enough to insure that a measurement will be taken exactly when the dendrite bridges. Thus, it is customary to examine SIR samples under the microscope with back lighting after the test is terminated to visually observe if dendrites have formed.

### 5.1.4 Conductive Anodic Filaments (CAF)

In the late 1970's a new electrochemical migration failure mechanism was reported
by Bell Laboratories [Ref. 84]. During the study of potential failure modes associated with high voltage switching applications, the subsurface formation of conductive filaments along the glass/epoxy interface was observed at high humidity conditions under application of a high (200-500 V) voltage. This conductive anodic filament (CAF) formation involved the dissolution of copper at the anode and the formation of a copper-containing conductive filament along the glass/epoxy interface. Augis and coworkers reported that these CAF contain copper associated with chlorine or sulfur [Ref. 85]; these contaminants are associated with the board manufacturing process. Others have observed only chloride- or bromide-containing copper filaments [Ref. 86]. It has been suggested that moisture causes hydrolysis at the glass/epoxy interface [Ref. 84]. It is postulated that the absorption of moisture by the epoxy causes swelling which can lead to a debonding between the epoxy and the glass fiber [Ref. 87]. This moisture-induced debonding can be accelerated with damage to the bond between the glass fibers and the surrounding epoxy during the drilling process [Ref. 88]. A capillary of moisture at these damaged interfaces is available for the electrochemical reactions described in Eqs. 5.6 and 5.7 when a bias voltage is applied.

5.2 INSULATION RESISTANCE MODELING

In order to make predictions as to the behavior and reliability of electronic assemblies in environments with varying levels of temperature and humidity, data from representative accelerated high stress tests are used to extrapolate to milder operating conditions. This extrapolation requires an appropriate valid extrapolation model. It has been found that neither obtaining good accelerated test data nor appropriate extrapolation models is a simple task [Ref. 89].

5.2.1 Insulation Resistance Degradation

SIR measurements are a relatively quick way to evaluate the interaction of processing materials with a given substrate. Reliability assessment, however, requires significantly more effort. Assumptions must be made about the relationship of the operating and use environments to the accelerating test conditions with elevated temperatures, humidities, and bias voltages chosen to accelerate the rate of degradation by known mechanisms without introducing extraneous damage mechanisms. If the assumptions are correct, extrapolation of the results from the accelerated tests back to operating conditions will provide an estimate of the product reliability.

To accomplish this task, a statistically significant number of samples must be processed and tested to failure at different accelerated test conditions. The effect of the temperature on the rate of failure follows for these processes an Arrhenius relationship [Ref. 90]

\[ k_T = k_0 \exp \left( -\frac{E_a}{kT} \right) \]  

(5.8)

where \( k_T \) = the reaction rate at absolute (Kelvin) temperature, \( T \), \( k_0 \) = a constant, \( E_a \) is the activation energy of the reaction, and \( k \) is Boltzmann's constant.

The effect of relative humidity can be described by

\[ k_H = k'_0 \exp(C(RH)^b) \]  

(5.9)

where \( k_H \) is the reaction rate at a given relative humidity, \( RH \), \( k'_0 \) is a constant, \( C \) is described as a constant but is likely temperature dependent (see Eq. 5.10), and \( b \) is an exponent empirically observed in the range from 1 [Refs. 79, 85] to 2 [Ref. 91].

For tests with a bias voltage of 52 V, the insulation resistance, \( IR \), was found to have the following dependence on temperature and humidity [Ref. 79]

\[ \ln IR = \ln IR_\infty + \frac{E_T}{kT} - \frac{RH}{100} E_{RH} \exp \left( \frac{E_{RH}}{kT} \right) \]

\[ = \ln 3.7 \times 10^{-29} + \frac{2.51}{kT} - \frac{RH}{100} 0.31 \exp \left( \frac{0.12}{kT} \right) \]  

(5.10)

where \( IR_\infty \) is an empirical constant interpreted as the insulation resistance of the test sample at infinite temperature and zero humidity, \( E_T \) is the activation energy for the temperature dependence, and \( E_{RH} \) and \( E_H \) are activation energies for the humidity dependence; for the activation
energies in eV, \( k = 8.62 \times 10^{-5} \text{ eV/K} \).

The form of Eq. 5.10 is the consequence of the fact that the driving parameter, the vapor pressure of water, \( p_v \), is dependent on temperature. The relationship of the vapor pressure of water with \( RH \) can be approximated in the temperature range from 0 to 75°C by

\[
p_v = \frac{RH}{100} \exp \left[ \frac{16.82 - 5250}{7[K]} \right] \quad (5.11)
\]

Under the assumption, that the effects of temperature and humidity are independent of each other and that the relationships can be validly extrapolated, the expected life can be calculated from results of the accelerated tests using an acceleration factor, A.F., using

\[
A.F. = \exp \left( \frac{E_a}{k} \left( \frac{1}{T_{life}} - \frac{1}{T_{test}} \right) - C \left( RH_{life} - RH_{test} \right) \right) \quad (5.12)
\]

where the subscript \( life \) refers to the normal operating conditions and the subscript \( test \) to the accelerated test conditions.

The failure mechanism is highly temperature dependent with activation energies, \( E_a \), variably reported as a very low 0.02 eV for some samples below 60°C and 0.6 to 2.5 eV for all samples above 60 65°C [Ref. 92], 0.6 eV [Ref. 91], 0.9 eV [Ref. 85] and 2.51 eV [Ref. 79].

The value of \( C \) associated with humidity can be taken from Eq. 5.10 with \( b = 1 \); for \( b = 2 \) and \( RH \) expressed in percent \( C \) has been reported as 4.4x10^{-4} [Ref. 91].

5.2.2 Conductive Anodic Filament Failure

The determination of the mean-time-to-failure (MTTF) for the CAF failure mode is more complicated.

The CAF-MTTF is not only dependent temperature, humidity, and bias voltage, but also on the PCB materials [Refs. 85, 93], and the quality of the manufacturing processes, particularly drilling [Ref. 88].

Further, preconditioning in terms of both thermal shock [Ref. 94] and exposure to high humidity [Refs. 88, 94], has been observed to reduce CAF-MTTF. There appears to be a two-step process in which pre-conditioning at an accelerated relative humidity will reduce the time for CAF failure to occur once voltage is applied. (1) Moisture absorption by the substrate leads to interfacial degradation at the glass/epoxy interfaces. This interfacial degradation can also be enhanced by prior thermal cycling or thermal shock or, by mechanical stresses. (2) Electrochemical corrosion and oxidation of Cu to Cu\(^{++}\) creates the ions which migrate under a bias voltage. The time to failure can be expressed as the sum of these two steps

\[ t_F = t_1 + t_2 \quad (5.13) \]

Studies where the application of the bias voltage was delayed indicate that \( t_1 = t_2 \) [Ref. 88].

There is evidence of a threshold relative humidity below which this degradation mode will not be observed. It has been proposed that for a given voltage, \( V \), and a temperature \( T \), the relative humidity, in percent, corresponding to a constant failure probability is [Ref. 85]

\[
RH = \left[ \frac{2.3975 + \ln(c) + 0.9}{kT} - 1.52 \ln(V) \right] \quad (5.14)
\]

where \( c = 6.9 \times 10^{-4} \) for a failure probability of 0.5%.

5.3 Dfr-PROCESS

For insulation resistance Dfr should perhaps stand for ‘Design for Robustness’ rather than ‘Design for Reliability,’ reliability assurance implies some numerical certitude which is not attainable in this context.

Thus, a successful Dfr-process is one that assures the highest level of robustness that is practically and economically achievable, requires that a number of issues be addressed at the design stage. The generally applicable guidelines to maximize robustness are:

1) Keep conductor lines and spaces on the PWB as wide as possible;
2) Provide a controlled operating environment;
3) Conformally coat electronic product if it is subject to temperature fluctuations such that condensation can occur;
4) Provide a controlled storage environment;
5) Avoid water-soluble fluxes and fusing fluids containing polyglycols, since they have been implicated in enhanced CAF formation;
6) Utilize CAF-resistant PCB materials for assemblies with high voltage gradients and high humidity operating environments,
7) Avoid testing conditions which create failure mechanisms and failure modes which will not be observed during normal operating life and use conditions.

5.4 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES
The emerging advanced technologies are characterized by dense, packaging resulting in ever finer conductor line widths and spacings. Without changes in the material and the operating environment, which for economical and practical reasons are not likely, finer lines and spacings result in reduced insulation resistance and increased threat of CAF formation. The DfR principles listed in Section 5.3 need to be kept in mind in the design and application of these emerging technologies.

5.5 VALIDATION AND QUALIFICATION TESTS

5.5.1 SIR Test Procedures
The most commonly used test vehicle for measuring SIR is an interdigitated comb pattern. These patterns exist in a variety of configurations with spacing between conductors ranging from 0.15 mm to 1.25 mm (5 to 50 mils). SIR tests are carried out at elevated temperature and humidity levels; however, some tests are performed with a bias voltage applied throughout the duration of the test, while others are performed without electrical bias being applied.

Bias voltages applied during testing ranges from 10 V to as much as 500 V. Periodically a test voltage of typically 100 V, for the electrically biased tests with reversed polarity, is applied to measure the insulation resistance. In the case of the electrochemical migration tests required by Bellcore [Ref. 95] the bias voltage and the test voltage have the same polarity.

SIR tests are normally performed at accelerated conditions with elevated temperature and humidity levels. The test conditions range from 35°C/95%RH to 85°C/85%RH with test durations varying from 100 to 500 hours. Pass criteria also vary from 100 MΩ to 200 MΩ. The electrochemical migration test requires that any decline in insulation resistance be less

<table>
<thead>
<tr>
<th>Parameters</th>
<th>IPC-TM-650 Solder Flux</th>
<th>Bellcore SIR</th>
<th>Bellcore Electromigration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Voltage</td>
<td>100 V</td>
<td>100 V</td>
<td>45 to 100 V</td>
</tr>
<tr>
<td>Bias Voltage</td>
<td>50 V</td>
<td>50 V</td>
<td>10 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Reverse</td>
<td>Reverse</td>
<td>Same</td>
</tr>
<tr>
<td>Environment</td>
<td>85°C/85%RH</td>
<td>35°C/85%RH</td>
<td>85°C/85%RH</td>
</tr>
<tr>
<td>Duration</td>
<td>7 days</td>
<td>4 days</td>
<td>500 hours</td>
</tr>
<tr>
<td>Lines/Spacing</td>
<td>0.4/0.5 mm</td>
<td>0.64/1.27 mm</td>
<td>0.32/0.32 mm</td>
</tr>
<tr>
<td>Number of Squares</td>
<td>-1000</td>
<td>-100</td>
<td>-500</td>
</tr>
<tr>
<td>Failure Criteria</td>
<td>100 MΩ</td>
<td>$10^5$ MΩ</td>
<td>SIR less than 1 decade decline</td>
</tr>
<tr>
<td></td>
<td>$2 \times 10^4$ MΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
than a decade for the sample to pass. Table 5 compares the variation in the test conditions for the IPC SIR test [Ref. 96] for soldering flux and the Delcor SIR and migration tests [Ref. 91].

The variation in the test parameters, as illustrated in Table 5, results in a large variation in observed SIR data. As indicated previously, the insulation resistance is an extrinsic property of the material sample under investigation. This property will be affected by the test parameters such as temperature, humidity, bias voltage and duration chosen for the test as well as the contamination associated with prior processing steps. This contamination may result in electrochemical corrosion.

SIR readings are sensitive to and affected by a number of factors.

5.5.1.1 Factors Affecting SIR Readings
Geometry. The geometry of the test pattern is of primary importance. When a bias voltage is applied, an interdigitated comb pattern experiences a distributed resistance due to the number of parallel traces over which the measurement is taken. The length of the interacting conductors divided by the separation between conductors is defined as the number of squares. In comparing data from two different comb patterns, the readings are sometimes reported as ohms/square.

Humidity. When a monolayer of water is absorbed onto the surface of an epoxy/glass PWB, the water molecules hydrogen-bond to the epoxy making them essentially immobile. These hydrogen-bonded water molecules can exist as either continuous coatings or as discrete islands [Ref. 97]. As subsequent water layers are added, thicker films are formed allowing the dissolution of contaminants and the formation of hydrated ions which can move under the influence of an electric field [Ref. 98]. Conductivity measurements made on aluminum oxide revealed that for films with thicknesses of less than three (3) monolayers, the surface conductivity is two orders of magnitude below that of bulk water [Ref. 99]. The surface conductivity increased asymptotically with the increase in the number of monolayers with equilibrium being reached above 20 monolayers. Evidence indicates that there is a critical relative humidity at which a compound exhibits a surge in moisture absorption [Ref. 100, 101]. For example, it has been demonstrated that dendritic growth of gold on alumina surface is dependent upon the relative humidity and that these existed a threshold for gold migration to occur [Ref. 102]. It has been shown, that the critical relative humidity for epoxy coatings is 70% and that the epoxy degrades over time when exposed to humid environments [Ref. 103].

Contamination. The presence of contamination on the surface will increase the moisture absorption. The critical relative humidity can be lowered by the presence of contaminants. The nature of these contaminants will determine how much moisture is absorbed at a given humidity level. If these contaminants are ionic in nature, they can enhance electrochemical reactions that occur in the presence of a bias voltage.

Voltage. The bias voltage applied across the insulator will set-up a response in the dipolar polymer substrate. In performing SIR testing, it is important that the bias voltage chosen is realistic as it relates to the actual operating and use conditions of the electronic assembly. Typical test methods require 45-50 V bias because this represents a moderate accelerating condition relative to the +/- 15 V circuits common in telecommunication hardware. Excessively high voltage tests for routine circuits can lead to damage mechanisms and failure not representative of product use.

5.6 SCREENING PROCEDURES
For the threats to reliability from low SIR and CAF formation no effective screening procedure exists. The best that can be done is following the DFR recommendations in Section 5.3 and the testing of representative samples using the test procedures discussed in Section 5.5.

6. SUMMARY AND CONCLUSIONS
From the foregoing, it should be clear, that the reliability of a product is driven to a very large extent by parameters determined at the design stage rather than in processing. Therefore, appropriate Design for Reliability-procedures,
carried out concurrently with the other design functions, are required to assure the long-term reliability of electronic assemblies.

The most critical threats to long-term product reliability have been discussed in this White Paper together with the necessary DfR-procedures. Specific critical reliability issues for some of the advanced packaging technologies have been highlighted.

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DFE: MORE THAN JUST DESIGN FOR THE ENVIRONMENT

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Lincolnwood, IL

ABSTRACT
Design for the Environment (DFE) is the systematic consideration during new product and process development of design issues associated with environmental, safety and health effects over the full product life cycle. The goal of DFE is to create more environmentally friendly products without compromising product cost, quality, or delivery. Although several factors such as regulations, public pressure and international standards are driving interest in DFE, the primary drivers are the costs and liabilities caused by toxic materials and pollution. The three fundamental elements necessary for DFE are as follows: Metrics, to measure needs, goals and performance; Design Practices, based on relevant technologies; and Analytic Methods, to assess designs with respect to metrics, costs and quality. The most common DFE metrics fall into four categories: energy, emissions, materials, and economics. When the appropriate metrics are selected, the designer can consider different DFE practices such as pollution prevention, material substitution, Design for Disassembly & Remanufacture, Design for Reclamation & Recycling, and Design for Maintainability. Analytical methods to assess different designs include life-cycle assessment (LCA), chemical use cluster analysis, and material/energy balance models.

INTRODUCTION
Although Design for the Environment (DFE) may be a new term, its roots go back at least 100 years.[1] In the 1800’s, manufacturing methods in the fur and pelt industry used mercury, causing “mad hatters” disease among hat makers and furriers and, undoubtedly, environmental damage. In the 1930’s, industrial dye workers developed bladder tumors from the benzidine used in manufacturing dyes at that time. And in modern times, the list of issues and concerns caused by manufacturing methods and products has escalated into the hundreds. Design for the Environment is one approach to ameliorate or eliminate these problems, but this one approach includes many possible methods:

- Pollution Prevention
  - Material Substitution
  - Design for Disassembly & Remanufacture
  - Design for Reclamation & Recycling
  - Design for Maintainability

Fundamentally, Design for the Environment is the systematic consideration during new product and process development of design issues associated with environmental, safety and health effects over the full product life cycle. The overall goal of DFE is to create more environmentally friendly products without compromising other product characteristics such as cost, quality, or manufacturing time.

DFE is the latest evolution in environmental management practices, and the foundation for future environmental management approaches leading to sustainable development (see Figures 1 and 2).

Figure 1: Evolution of Environmental Management[2]

Sustainable Development has been defined as "development that meets the needs of the present without compromising the ability of future generations to meet their own needs."[3]

Although many people and organizations embrace the term "sustainable development," they vary considerably in translating that phrase into concrete terms for steering policy development or technology selections.

Industrial ecology is a more concrete and objective field of study that tends to quantify the links between natural ecology systems and the industrial and economic systems interacting with them.

A Design for the Environment infrastructure is a system in which companies or societies provide the necessary tools for individuals or corporations to implement industrial ecology. Thus, DFE infrastructure would include legal and economic systems as well as specific methodologies, data banks, and other resources.

Design for the Environment itself is the implementation of specific industrial ecology principles by a particular company, individuals, or other entity. DFE is usually more short-term or limited in scope than general industrial ecology or sustainable development.

REASONS TO IMPLEMENT DFE
There are six basic reasons to do DFE:
1) Reduce costs  
2) Increase customer satisfaction  
3) Reduce liabilities  
4) Increase public relations image  
5) Reduce compliance issues  
6) Increase social responsibility

DFE will lower the costs associated with the wastes generated by inefficient designs and poor manufacturing practices. The more significant savings, however, usually come from reducing the costs associated with storage, treatment and disposal of pollutants and hazardous wastes.

In addition, DFE can reduce health concerns and problems associated with using environmentally unfriendly or toxic materials in the manufacturing process. It can also eliminate the liabilities associated with those toxins. This includes not only the immediate liabilities for worker safety and health in the workplace, but future liability potential from long-term health effects, manufacturing site contamination or ultimate end-product disposal.

Even though most contract electronic assembly companies do not manufacture final consumer products, their circuit assemblies do wind up in consumer products, which ultimately wind up in municipal landfills.

Environmental regulatory compliance problems and other related issues are also reduced by DFE approaches. By reducing toxic uses, wastes, and pollution, DFE can significantly reduce or even eliminate many regulatory compliance issues, both local and federal. DFE can get your company out of some regulatory loops.

But in addition to regulatory compliance, DFE can solve problems associated with international standards compliance. For example, just as ISO 9000 is becoming a de facto international standard for quality, the ISO 14000 environmental standards may soon become de facto international specifications for environmental aspects of electronic products. In some instances, ISO 14000 standards are required in order to sell products in Europe. These standards may necessitate environmental labelling, life cycle analysis or other requirements which DFE can help you meet.

Along similar lines, many customers are beginning to demand environmentally friendly components and products. These customers not only include public consumers, but many OEMs and federal agencies such as the Department of Defense. They are driven to demand environmentally friendly products for the same reason you are: to eliminate potential liability, costs, and environmental regulatory problems. Your customers need reliable suppliers. As such, they want to insure not only that you are not causing them additional problems, but that you are not causing yourself problems which could put you out of business.

In addition to improving your customer satisfaction, DFE can also improve your company’s public image. Many companies, large and small, are winning local, state or federal awards and recognition for their environmentally pro-active work. DFE can launch this pro-active approach.

Finally, many companies are embracing DFE because they feel that it is their social responsibility to protect environmental quality for their employees, their families, and their communities. While this may be the least tangible reason to do DFE, it may also be the most rewarding.

FUNDAMENTAL ELEMENTS OF DFE
Although there are myriad aspects to DFE, the fundamentals can be boiled down to three key elements: metrics, design practices, and analytical methods.

DFE Metrics
Metrics are the methods used to measure needs, goals, and performance. Although a company may look at many different DFE metrics, the most common DFE metrics fall into four categories: emissions, economics, materials, and energy.

Economics and Emissions
Most contract electronic assemblers and PWB manufacturers are more interested in the economics and emissions metrics. They want to know how much implementing DFE approaches will cost, and how much it will save over the long-run. They also want to know how DFE will lower their waste generation and pollution emissions.

While the cost of DFE implementation may be reasonably easy to estimate, the cost savings may not. In many companies, the costs of waste generation, treatment and disposal as well as regulatory compliance expenses are buried in overhead. In addition, the potential savings from reduced or eliminated liabilities are even harder to estimate.

Two points warrant mention here. First, while costs and savings may be difficult to estimate, most companies have found that the savings more than pay for the costs in the long run, and sometimes even in the short run. Pay-back periods may be only a few months. Second, just because DFE issues are difficult to quantify, they should not be disregarded. Many of us tend to ignore an issue which cannot be quantified. It’s easier than dealing with the issue. But ignoring DFE because clear data is lacking does not mean the environmental and health costs and problems which DFE is meant to address go away. They simply go quietly on.

Materials
The next DFE metric typically involves material characteristics, costs, and hazards. A designer needs to estimate how substituting a more environmentally friendly material will affect all of these parameters, and especially...
product, quality, reliability, and turn-around time. While your material supplier may be helpful in estimating these effects, you should keep in mind their vested interests. Perhaps the most important person to contact regarding possible material changes is your customer. They may have specific reasons for specifying a material, or they may be helpful in discussing performance parameters which any material in the product must meet.

Energy

Finally, the last DFE metric involves estimating changes in energy consumption associated with DFE implementation. The results may not always be what was expected. For example, one electronics manufacturer substituted an aqueous cleaning system to replace the closed-loop solvent cleaning system. Except for fairly minor fugitive emissions, the solvent system had no major health or environmental problems associated with it. Nonetheless, to reduce TRI reporting numbers and be environmentally pro-active, the company implemented a new aqueous cleaning system.

While this eliminated the use of solvents, it considerably increased not only water consumption and water disposal, but energy consumption as well. The aqueous cleaning system used considerable energy for heating. It also required an ion exchange system. The ion exchange system, in turn, consumed considerable energy and produced waste ion exchange resin which had to be shipped off-site for regeneration, thereby increasing costs and transportation liabilities. What seemed to be an environmentally-friendly choice turned out to be the opposite.

DFE Design Practices

Once a company or designer has selected which metrics are most important to their particular operations and products, the designer can consider different DFE practices to meet the goals identified by the DFE metrics. While the DFE design practices can be as numerous and varied as the DFE metrics, some of the more common practices include the following:

- Pollution prevention/waste source reduction
- Material substitution
- Design for disassembly and remanufacture
- Design for reclamation and recycling
- Design for maintainability
- Design for energy recovery

Pollution Prevention

The EPA generally presents pollution prevention as a hierarchy of four choices. The most desirable option is source reduction. This may fundamentally mean implementing good housekeeping procedures to reduce waste and practising material/water/energy conservation wherever possible in the manufacturing process. Pollution prevention also includes insuring that your pollution prevention control equipment is operating properly.

The next choice in pollution prevention is substitution. Substitution includes replacing toxic manufacturing processes and materials with less hazardous ones. This will be discussed in more detail in the next section on Material Substitution.

The third pollution prevention option is recycling, in which the materials generated during the manufacture and life cycle of a product are recovered and recycled in some way. Most PWB manufacturers and electronic assemblers are doing this to some extent by recycling solder dress and pot dumpings back to a smelter and sending scrap boards and assemblies to a metal reclamation site. Unfortunately, many local, state and federal laws actually hinder the material recycle loop. A number of IPC member companies are involved in the EPA's Common Sense Initiative (CSI) to help identify pollution prevention and recycling barriers, and revise the regulations to eliminate those barriers.

Finally, the last pollution prevention option, and least desirable, is to dispose of waste safely and properly. This disposal option or strategy should include not only disposing of immediate manufacturing waste properly, but ensuring that the final consumer product can be disposed of safely and properly.

Material Substitution

Material substitution is another major DFE practice that many companies are implementing, though the analysis may not be as straightforward as imagined. While the general goal of material substitution is clear (replace toxic materials with less hazardous alternatives) the trade-offs involved in material substitution are often not clear. One test case demonstrated this clearly.

Year after year, Congress considers some kind of legislation to reduce or eliminate the use of lead in electronics manufacturing. The goal would be to eliminate toxic lead from the environment and therefore improve environmental quality. However, what does a detailed DFE analysis regarding lead solder substitution indicate regarding environmental impacts?

In a detailed paper entitled "Testing Design for the Environment: Should Lead Solder be Used in Printed Wiring Board Assembly?" Dr. Brad Allenby of AT&T conducted a careful Design for the Environment Information System (DFEIS) analysis for printed wiring board assembly options. This analysis looked not only at the effects on air, water, soil, and resource consumption but also the effect of these
SUSTAINABLE DEVELOPMENT
↓
INDUSTRIAL ECOLOGY
↓
DESIGN FOR ENVIRONMENT INFRASTRUCTURE
↓
DESIGN FOR ENVIRONMENT
↑

DFE

GENERIC
↓

GREEN ACCOUNTING

SPECIFIC
↓

GREEN BUSINESS PLANNING

GREEN SPECS AND STANDARDS

DESIGN CHECKLISTS

CAD/CAM MATRIX

DFE TOOLS SYSTEMS

Figure 2: Position of DFE in Sustainable Development

Manufacturing Primary Matrix

<table>
<thead>
<tr>
<th>Initial Production</th>
<th>Primary Processing/Manufacturing</th>
<th>Packaging</th>
<th>Transportation</th>
<th>Consumer Use</th>
<th>Industrial</th>
<th>Disposal</th>
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<td>Performance</td>
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<td>Energy Consumption</td>
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<td>Resource Consumption</td>
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Figure 3: DFEIS Manufacturing Primary Matrix
### Social/Political Primary Matrix

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<th></th>
<th>Raw Material/Processing/Manufacturing</th>
<th>Packaging</th>
<th>Transportation</th>
<th>Consumer Use</th>
<th>Market Practices</th>
<th>Disposal</th>
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<tr>
<td>Legal</td>
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<td>Community Status</td>
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<td>Community Impact</td>
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### Environmental Primary Matrix

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<tr>
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<th>Initial Production</th>
<th>Secondary Processing/Manufacturing</th>
<th>Packaging</th>
<th>Transportation</th>
<th>Consumer Use</th>
<th>Reuse/Recycle</th>
<th>Disposal</th>
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<td>Ocean</td>
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<td>Waste</td>
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<td>Resource Consumption</td>
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</table>

### Toxicology/Exposure Primary Matrix

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<th>Secondary Processing/Manufacturing</th>
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<th>Transportation</th>
<th>Consumer Use</th>
<th>Reuse/Recycle</th>
<th>Disposal</th>
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<td>Consumer Exposure</td>
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<td>Environmental Impact</td>
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<td>Medical</td>
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<td>Other Environmental Impact</td>
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<td>Significant Exemptions</td>
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<td>Other</td>
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</table>
Figure 7: DFEIS Summary Matrix Options

Environmentally responsible product assessment matrix

Matrix elements are assigned a number ranging from 0 (highest impact on the environment) to 5 (lowest impact). The numbers in each box are the matrix element indices.

<table>
<thead>
<tr>
<th>Environmental concern</th>
<th>Life cycle stage</th>
<th>Materials choice</th>
<th>Energy use</th>
<th>Solid residues</th>
<th>Liquid residues</th>
<th>Gaseous residues</th>
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</thead>
<tbody>
<tr>
<td>Premanufacture</td>
<td>(1,1)</td>
<td>(1,2)</td>
<td>(1,3)</td>
<td>(1,4)</td>
<td>(1,5)</td>
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</tr>
<tr>
<td>Product manufacture</td>
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<td>(2,2)</td>
<td>(2,3)</td>
<td>(2,4)</td>
<td>(2,5)</td>
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<td>Product packaging and transport</td>
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<td>(3,2)</td>
<td>(3,3)</td>
<td>(3,4)</td>
<td>(3,5)</td>
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</tr>
<tr>
<td>Product use</td>
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<td>(4,2)</td>
<td>(4,3)</td>
<td>(4,4)</td>
<td>(4,5)</td>
<td></td>
</tr>
<tr>
<td>Refurbishment-recycling-disposal</td>
<td>(5,1)</td>
<td>(5,2)</td>
<td>(5,3)</td>
<td>(5,4)</td>
<td>(5,5)</td>
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Figure 8: Environmentally Responsible Product Assessment Matrix
various options on the compatibility for processes, materials, and components, the effects on performance and energy consumption, the costs and availability of alternatives, and the effects on resource consumption. Dr. Allenby used various matrices as shown in Figures 3-7. The results were quite interesting.

Even if their were enough bismuth and indium in the world to significantly substitute for all existing lead solder used in PWB assembly (which there is not), the overall risk posed by current PbWA lead solder use would be roughly comparable to the risks presented by widespread substitution of bismuth, indium or even silver. This does not mean that these various options are undesirable or shouldn’t be implemented as appropriate for various reasons. It simply indicates that without DFEIS analysis, what appears to be an obvious answer on the surface may in fact not have the desired result.

Design for Disassembly & Remanufacture

One of the next major DFE practices is design for disassembly and remanufacture [6]. Fundamentally, this approach means that product should be designed for safe, easy disassembly with as little labor or energy as possible. The basic approaches to ensure that this is possible include the following:[6]

- Parts requiring disassembly and materials requiring sorting into component materials are minimized
- Disassembly is safe (harmful liquids/gases can be easily and safely extracted; dangerous components cannot be dismantled by non-professionals)
- Components and subassemblies (PWBs, chips, materials, screws) must be easily identifiable and separable.
- Snap assembly is preferred over screws and bolts, and any screws or bolts used should have the same head configuration.
- Metal parts should not be imbedded in the plastic.
- A minimum number of different materials should be used in the product.
- Plastic should be clearly marked for identification for recycling
- Plastic should not be painted

To help implement design for disassembly and remanufacture concepts, manufacturers must work with their suppliers and customers to develop an integrated strategy which includes a product plan that considers all of the possible post-consumer uses or applications for both the product and its component parts. Because components will be recovered and re-used, manufacturers will need to estimate component lives and failure rates to determine when components need to be permanently replaced. As part of this, of course, the product plan or strategy will need some system for identifying how many times a component has been recovered and reused. In addition, the product plan will need more extensive testing procedures and inspection to ensure that refurnished equipment and components maintain acceptable quality.

Of course, a new design for disassembly and remanufacture approach will require changes not only in the manufacturing chain but in the final consumer’s mind and in government. Consumers will play a vital role not only in returning products after purchase and use, but in accepting that a remanufactured or “used” product is of acceptable quality. U.S. law will also be important in changing labeling requirements for remanufactured products and in allowing manufacturers to recover used products without being caught in the EPA RCRA solid waste net.

Design for Reclamation and Recycling

If a product cannot be designed for disassembly and remanufacture, another environmentally friendly option is design for reclamation and recycling in which the product is reclaimed so that either the materials can be recycled or used for energy recovery. As with design for disassembly and remanufacture, design for reclamation and recovery involves many of the same fundamental concepts. In order to separate materials for recycling, the product will probably need to be easily disassembled and component parts or materials easily identified. However, there are a few additional principles in design for reclamation and recycling that should be kept in mind.

First, avoid using hazardous materials that will cause the reclaimed product to be considered a hazardous waste. If you do use the hazardous materials, try to make them easily removable or segregated from the main product. Reduce the material diversity in the product by eliminating the number of materials specified as well as the number of fillers and colors or their contaminants (lead stabilizers, flame retardants, coatings or films,) used in the product. In addition, avoid the use of heavy metals in the product wherever possible. Even if regulations were changed to allow recovery of waste streams containing heavy metals, if the material is ultimately going to energy recovery (incineration) heavy metals can cause environmental problems there.

Another design for reclamation and recycling approach is to use recycled materials in making your products. By using recycled materials, you help guarantee that a market exists to take your own products and materials at the end of manufacturing or useful life.

Design for Maintainability

One last DFE practice is life extension, sometimes also called design for maintainability (DFM). The goal of DFM is to reduce the environmental impacts associated with
end-product disposal by extending the life of the product, or by reducing the environmental impacts associated with long-term operation and maintenance of the product.

The most fundamental DFM principle is basically design for repairability. Systems should be designed so they can be easily repaired or if necessary replaced on-site and repaired back at the manufacturing location. That means that components, parts, and subassemblies should be replaceable and separately repairable. It also means that product maintenance requirements should be minimized, and the materials required for maintenance be environmentally friendly, such as aqueous cleaners instead of chlorinated solvents.

**ANALYTICAL METHODS**

The last basic element in DFE after metrics and design practices is the set of analytical methods to assess DFE design practices relative to DFE metrics and other parameters such as product quality, turn-around time, and so forth. Three basic analytical methods in common use are as follows:

1) Life cycle analysis
2) Chemical use cluster analysis
3) Utility/energy balance

**Life Cycle Analysis**

Life cycle analysis or assessment (LCA) can be an extremely complicated and uncertain science. However, one of the more straightforward approaches recommended by researchers at AT&T is the LCA matrix. This matrix (see example in Figure 8) addresses the five life cycle stages for a manufactured product.

While this approach may be less detailed and comprehensive than either classic inventory analysis or a detailed life cycle impact analysis, the LCA matrix is more practical and utilitarian, and therefore more likely to be used. It provides a relatively rapid way to assess several different scenarios or choices.

In essence, the designer studies the various matrix element indices and assigns each element a rating from 0 (highest environmental impact or very negative) to 4 (lowest environmental impact or most positive). Once each element matrix has been evaluated, the overall environmentally responsible product rating (ERP) is computed as the sum of the matrix element values:

\[ ERP = \sum_{ij} \text{ERP}_{ij} \]

Since there are 25 matrix elements and each one can have at most a value of 4, the maximum environmentally responsible product rating is 100. In other words, a low rating indicates a serious environmental impact while a high rating indicates a relatively environmentally friendly product.

Although the questions used in this K&K example are too long to list here, some sample questions include the following:[8]

- Are products designed to use recycled materials?
- Do products use minimal energy in manufacturing, use and recycling or disposal?
- Are products designed to generate minimal and nontoxic residue (solid, liquid & gaseous) in manufacturing, use and recycling or disposal?
- Have all processes been dematerialized (evaluated to insure that they have minimum resource requirement and that no unnecessary process steps are required)?
- Do processes generate waste heat or emit harmful residues, and if so has capture and reuse of these resources been explored?
- Have processes been evaluated for energy efficiency?

**Chemical Use Cluster Analysis**

Chemical use cluster analysis is another common analytical method to evaluate different material or manufacturing alternatives. A chemical use cluster is defined as a set of chemicals, processes, and technologies used to accomplish a specific task in manufacturing. In printed wiring board manufacturing, for example, making holes conductive would be considered a use cluster, and the different options for that use cluster would include traditional electroless plating as well as newer direct metallization options.

In electronic assembly, component joining might be one use cluster. Different options for component joining would include traditional lead soldering using either wave solder or different reflow solder techniques. Other options for this use cluster might include conductive adhesives or isotopic conductive elastomers or wire bonding.

In a use cluster analysis, all the potential hazards and exposure scenarios for the various chemicals and processes used are identified and evaluated. This allows a fairly direct comparison of different potential substitutes within a use cluster.

**Energy/Utility Balance**

Finally, one of the last analytical methods used is a utility or energy balance. This approach evaluates the consumption of water, electricity, natural gas and other utilities in the manufacturing process. This step of analysis may be absolutely crucial in considering material substitution because, as was pointed out for aqueous cleaners vs. solvents, the toxicity trade-offs in eliminating, more toxic materials may be less than the environmental impact of increased water and energy consumption in switching to a less toxic alternative material.
THE DFE PROCESS: HOW TO GET STARTED

Thomas Jefferson once said "Great innovations should not be forced on slender majorities." In this case, implementing DFE innovations will be easier if the slender majority includes top management.

Design for the Environment is in the same position that quality was in ten or fifteen years ago. At that time, top management for most companies was focused almost exclusively on sales and financial figures. Eventually, however, the mindset changed and upper management realized how crucial quality is in improving sales and financial standing.

Today, upper management is slowly becoming aware of how integral environmentally friendly manufacturing processes and products are to the overall business scheme. It's usually easy to persuade upper management of the importance of DFE, however, if the various costs and liabilities associated with environmentally unfriendly manufacturing and products have been quantified. This is not always easy, but it is a critical step. Many environmental costs at companies today are lumped into overhead. Managers and designers must breakout specific environmental costs associated with each process and product including energy consumption, waste production, waste treatment and disposal, health costs, and so forth.

The next step for building a DFE foundation is to review customer specifications and preferences. With all this information at hand, senior management will probably be much more likely to recognize the cost savings and competitive advantage in implementing DFE.

The next step in DFE implementation is usually to broaden the education circle to include plant managers, quality personnel, sales personnel, designers, purchasing departments, vendors and suppliers outside the company. Their involvement is crucial for a number of reasons.

First, since DFE implementation may initially make life more difficult for a number of personnel, they need to be sold on the overall benefits to the corporation and perhaps to them personally. Second, they need to be involved in the decision making to ensure that DFE implementation will not hurt product quality, turn around time or marketability, and in fact may improve the marketability of the product.

Next, environmental considerations must be given the same emphasis as other considerations such as cost and quality. Companies must review their own specifications and vendor requirements to make sure they are not causing unnecessary environmental impacts in the supply chain. Similarly, you will need to work with your customers and question any customer specifications that cause environmental problems to ensure that they are absolutely necessary.

As part of this stage, you should review your material specifications to make sure they are consistent with DFE goals as well as national and international standards.

Finally, DFE issues must be considered at the earliest stages in product planning and development. These DFE issues should include life cycle analysis and recycling potential. As part of this stage, design reviews and assessments should be modified to include a DFE assessment.

CONCLUSION

Competition demands innovation. In order to remain competitive, electronics manufacturers must reduce costs while improving quality and performance. DFE is one way to meet this competitive challenge. DFE can reduce waste, reduce costs, and reduce liabilities while improving workplace and environmental quality, and perhaps product quality, as well as corporate performance. DFE is also a way to heed the words of Francis Bacon, who said that "Nature, to be commanded, must be obeyed."

REFERENCES