SURFACE MOUNT COUNCIL WHITE PAPER

Soldering Capability
INTRODUCTION

What does good solderability mean?

Solderability has been defined to varying levels of detail depending on the observer’s immediate perspective. The fundamental definition from which they develop, however, is that good solderability means the ability of a base metal to be evenly wetted with an adherent coat of solder[1][2]. Due to a desire for a cosmetically “shiny” joint, the definition has been pragmatically expanded by some to also include additional characteristics of solder fillet surface luster or smoothness.[3]

How is poor solderability identified? How is it measured?

Poor printed circuit (PWB) solderability may be identified in any one of several ways both prior and subsequent to the soldering process. A number of industry standard tests[4] and equipment exist for evaluating both the extent of solder wettability of a surface and the resulting mechanical strength of the bonds accomplished. Frequent, statistically validated, testing has become standard practice at most of the world’s major PWB suppliers to provide manufacturing process control and screen outgoing lots.

Why is it important? Results of poor solderability.

Poor product solderability at the least involves added inspection and touchup costs. At worst it may precipitate a catastrophic circuit failure.

Unfortunately, often the most common point of solderability problem identification is after components have already been assembled to the circuit and it has passed through the soldering process. The purpose of soldering components to a circuit is to provide both a low resistance electrical path and a primary (surface mount) or secondary means of mechanical retention in/on the circuit.

Inadequate solder at the component/circuit interface leads increases the probability of increased electrical resistance, circuit “hot spots”, intermittent performance, and potential circuit failure. In a consumer product, this may be of relatively small consequence. In a system control or life support application, it may have catastrophic results.

One of the most frequent symptoms of poor solderability is a dewetted PWB surface[5]. A second may involve plated through holes which fill partly or not at all. The lack of fill may not decrease the reliability of any specific hole, but in the case of an MLB,
can be a "process indicator" alerting the assembly operation of other latent problems with overall interconnection quality and reliability.

What are the primary design issues influencing soldering capability?

Good product soldering performance occurs as a result of good design practices, well specified and sourced materials, strong manufacturing process controls, and attention to detail. The first phase of ensuring product solderability is rooted in the fundamentals of the product design process. The product should be viewed as a system of interrelated parts, assembled to accomplish a customer defined function (who else would you build it for?).

Given a failure of any one of those composite parts will result in some limitation of product performance to specification. The must take into consideration issues relating to materials, layout, process capability/limitations.

MATERIAL ISSUES

Basic circuit laminate characteristics (e.g. thermal dissipation)

The printed wiring laminate serves as the basic carrier for the circuit lines and pads, components and any additional structural hardware. Laminate materials may include Teflon® paper, epoxy glass, and ceramic, each with its own unique electrical and material characteristics. The choice of laminate may have a substantial effect on solderability based on material thickness, thermal dissipation, and distribution of circuitry/vias.

Even when the discussion is narrowed down to a common epoxy glass material, such as FR-4, there may be unanticipated results. As an example, epoxy glass is generally regarded as a good electrical and thermal insulator. When used in thin sections (e.g. .031" thick) the heat from a solder wave against the bottom of the board will provide substantial soldering heat to the top side components, generally improving wetting provided the to be soldered surfaces are wettable. As you might suspect, the thicker the printed wiring substrate becomes, the greater the insulative effect through the material becomes.

Basic circuit metallurgy (e.g. fired Ag frit, Cu plate)

Circuit metallurgy may be any of a number of materials. Although most printed circuits use a copper plate over an initial thin (< .001") copper foil laminated to the circuit laminate, conductors may range from fired on gold and silver thick film frits to conductive carbon materials. This paper will focus primarily on the copper conductors found on the majority of circuits.

Copper serves as the most common circuit conductor material for several reasons. It is a relatively inexpensive, highly malleable, easily plateable and etchable material with low
resistivity and high rate of wettability in molten solder. In an initially plated form, it is readily wettable by tin lead solders[6]. This high initial solderability may diminish rapidly with time and exposure to either oxidizing, corrosive environments, or organic contaminants.

Solder site finish metallurgy (e.g. HASL, SnPb Plate and Reflow, SnNi)

Several methods have been developed to retain circuit solderability. In general, these methods involve the sealing off of the surface with a secondary coat of non-oxidizing or slow oxidizing protective metal with the oxide formed removable by acceptable fluxes. Tin lead is the most common of these materials and may be applied by cladding, electrolytic or electroless plating, or by one of several "hot-dipping" processes. Electroplated tin nickel is also used as a protective overcoat material. With decreased trace spacing and increased component density, bare copper with anti-oxidant protection has become an accepted method of providing good solderability.

Solder resist materials (e.g. "active" atmosphere compatibility)

Solder resist is a non-wettable surface coating placed on the circuit surface to prevent solder from adhering to, and forming "bridges" between, adjacent conductive circuit lines. The material is commonly a polymer and applied to the circuit as a liquid or film overlay. Portions of the material, over areas to remain solder free, are then cured with heat and/or UV light. The remaining uncured resist is then flushed away exposing the areas to receive solder.

Recent developments with "active or protective atmosphere" wave soldering designed to preserve or enhance wetting may result in unanticipated results with some solder resists. Initial experience has indicated potential sensitivity of some photo-defined resists to elements of the active atmosphere gas mixture resulting in the generation of excessive solder balls. These conductive balls may be temporarily embedded in the resist material, becoming dislodged during later product handling or use and causing the circuit to malfunction or fail. This possible issue will be clarified as we gain more experience with active atmospheres and more stable resists are developed.

LAYOUT ISSUES

There are a number of layout issues that may act individually or together to affect solderability including the size, orientation and location of the solder site.

Solder site size (e.g. pad size/dimensions for wave vs. reflow)

The dimensions of the solder site are a function of component size, circuit current, soldering process type, product use environment, and reliability requirements. Whether the components to be soldered are surface mount or through hole, the solder site must be
physically large enough to provide an adequate wetting surface to the component termination to permit worst case (max. spec current load at max. operational temperature) circuit functionality.

Practice has also indicated that pad size will be influenced by the manufacturing processes available. Wave soldering, particularly those using hot air knives, require sufficient solder site surface area exposed (that is, not covered by the component body or lead) to allow the solder to wet to both the PWB solder pad and component lead. This dimension is frequently on the order of 1.5 to 3 times the lead width (or diameter). Reflow type processes, however, have controlled portions of solder paste placed (screened) onto the solder pad prior to any component being placed.

With SMT components and reflow techniques, it is theoretically possible to reduce the size of the solder pads to substantially less than the "lead" width, although common practice generally uses pads on the order of 1 to 1.5 times the lead width[7]. A significant amount of testing and practical experience indicates that 0.7 to 1 provides better first pass yield and improves operational life.

Solder pad dimensions, for passive SMT components, have been demonstrated as having a direct correlation to solder joint life[8]. Testing done in Japan in the late 1970's indicated that the operational life of solder joints on surface mount resistors and capacitors was significantly extended when the width of the solder pad to which the devices were attached was equal to or less than the width of the component. The length of the pad did not appear to be a significant variable.

Component pad orientation

Component solder pad orientation may influence solderability depending on the manufacturing process used. As mentioned previously, reflow soldering techniques may offer some additional margin in orientation flexibility due to the screening of a controlled portion of solder paste onto specific known locations on the circuit.

Wave soldered components must not only provide additional unencumbered solder pad real estate for wetting but must also provide it in an orientation accessible to the wave action of the machine. Components oriented in other configurations are subject to non-wetting due to "shadowing" of the solder pad by the component body. As you might expect, the higher the part above the surface of the PWB, the greater the "shadowing" effect.

Component pad co-proximity

A subset of the "shadowing" effect discussed previously concerns components located closely adjacent to one another (Fig. 1). Wave soldering practice has shown that, as a general rule of thumb, components located closer than twice the height of the component preceding it into the wave have a substantially increased probability of non-wetted solder pads.
A similar effect is evident on boards soldered in radiant only IR solder ovens when tall adjacent shields or devices may effectively shield a component from adequate heat to accomplish reflow of the solder paste.

Component pad location

Irrespective of the influence of component shadowing, components which are reflow soldered may be influenced by the effect of edge heating. Thermal transfer within an infrared reflow oven is not homogeneous throughout. A circuit passing through the oven receives not only the primary heating provided by the lamps/panels/et al but also secondary heating from energy reflected by the effect of edge heating.

It turns out that the edges of the circuit also have more exposed surface area available to absorb heat (at top + bottom + side edge area). The net effect is that solder pads adjacent to a circuit edge are subject to greater overall heating than the interior surfaces of the circuit. This offers a good opportunity for soldering thermally massive components but may damage others if not compensated for. The increased use of convection ovens and IR furnaces with significant volumes of recirculated air or nitrogen has reduced the extent of edge overheating.

Figure 1. Wave Solder Process Component Spacing Guidelines
PROCESSING/HANDLING - ANTICIPATION AND PLANNING

Assuring received circuit cleanliness

It is fundamentally inconsistent to pursue the development and manufacture of high QUALITY products without assuring a foundation of high QUALITY components. Unfortunately, printed circuits have often been overlooked in the consideration of circuit components. However, as clock frequencies and operational speeds continue to climb, PWB’s are becoming increasingly important as both structural elements and active circuit elements.

Pre-manufacturing evaluation of PWB’s has characteristically been pursued with little more than a visual check for dewetting. More recent sensitivity, borne out of SMT experience, has motivated a more thorough evaluation of surface finishes, flatness, solder coating, and cleanliness[10]. Cleanliness testing may be carried out by either simple measures of surface conductivity with deionized water or a more comprehensive solvent extract conductivity method (e.g. Ionograph®).

Maintaining PWB cleanliness and solderability is often a substantial challenge in itself. The PWB is typically delivered to the point of incoming test still safely ensconced within the manufacturer’s original packaging. Once tested, however, the accepted test lot is often inadvertently exposed to oxidizing or corrosive atmospheres, handled with contaminated gloves or perspiration laden hands, and stored on soiled shelves. Even then, they may remain in a generally uncontrolled (e.g. temperature and humidity) for many months. While it is not required that boards be handled in an antiseptic manner, the better the surface finish is maintained and the more rapidly the boards are used, the better the solderability will be.

Non-oxidizing/non-corrosive packaging (e.g. no sulfur papers or cardboard) - Benzotriazole coupons

PWBs may encounter a variety of environmental conditions between the time they leave the suppliers line to the time they are ready for component assembly. To minimize the influence of high humidity and oxidizing agents on the solderable surfaces, several commercial coatings have become available.

Tin-lead and tin-nickel are two of the metallurgical coatings applied to maintain solderability. Some circuits, however, use bare copper for perceived reasons of cost, flatness, or solderability. Given a less than controlled environment bare copper may corrode rapidly.

Copper benzotriazole is an example of a corrosion inhibitor which may be used to protect the solderability of bare copper surfaces[11]. Either sprayed directly onto the PWB surface and subsequently dried or soaked into a coupon and packaged with the boards, the benzotriazole will provide a corrosion resistant chemical layer on the circuit copper for several months. The material then readily breaks down and dissipates in the pre-heat process immediately prior to soldering.
Non-warping packaging (e.g., no tie strapping of boxes)

The soldering performance of PWB's may also be affected by issues other than circuit metallization. PWB flatness, as an example, is important for a number of reasons. Circuit flatness will influence ease of assembly fixturing, component insertion, and testability.

It may also have a substantial effect on circuit solderability. PWB flatness may be affected by supplier packaging (e.g., boards tie-strapped together), shipper handling, and user storage conditions. PWBs exhibiting excessive warp[12] may exhibit substantial problems in the soldering process. Wave soldering of boards with excessive concave warp may scoop into the wave resulting in top-side solder "flooding" while those with excessive convex warp may have portions of the circuit which never make contact with the wave (Fig. 2).

Fig. 2. Printed circuit board warp

- Concave board warp
- Convex board warp
Reflow processed boards will experience difficulty in the accurate and consistent deposition of solder paste on the warped circuits and may develop secondary problems with components becoming displaced due to insufficient retaining solder paste.

Rapid inventory turnover (e.g. minimize intermetallic growth)

Minimize thermal exposure (e.g. accelerated oxidation and intermetallic growth)

PWB surfaces are frequently coated with either plated or hot tin lead as a protective anti-oxidant. This coating has been demonstrated as effective in retaining the solderability of both air and steam aged boards for as long as two years[13].

**SUMMARY/RECOMMENDATIONS**

Good soldering performance is a result of good design practices, well specified materials, effective manufacturing process controls and attention to detail.

Major impact issues

The three most influential design issues effecting solderability include the availability (e.g. layout size and orientation) of a wettable surface appropriate to the soldering technology chosen, wettability of the surface to be soldered, and circuit flatness.

**Recommendations to avoid solderability problems**

Solderability problems may develop from a number of sources. They may be minimized by the specification of a high integrity conductor/pad plating, protective solder coating, surface cleanliness and handling/packaging criteria.

Plan for a "systems" approach. Do not focus only on the PWB or the component. The product should be viewed as a system of interrelated parts, assembled to accomplish a defined function. Good product solderability occurs as a result of both good component and PWB solderability. Design with the components and their requisite nuances (e.g. body size, lead configuration, and number) in mind.

Plan for synergy with the circuit supplier and assembly process (e.g. early involvement). Circuit design has developed far beyond the alcove of the engineer and the draftsman. To be successful at arriving at a cost effective new design now requires inputs from people knowledgeable with circuit media, components, assembly technology, and purchasing -- a team effort.
The most effective teams also have links directly to the PWB supplier and work with him on a frequent basis. This synergistic approach allows the design team to develop the lowest "Design for Manufacturing" (DM), fastest turnaround, and most easily manufactureable product.

References


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SOLDERING CAPABILITY
PWB FABRICATION VIEWPOINT

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ABSTRACT

Soldering of electronic assemblies has changed significantly over the last 40 years. At virtually every step, the demands on the Printed Wiring Board (PWB) solderability have increased. The incorporation of fine pitch Surface Mount Devices (SMD) has continued the demand for improved solderability and new factors have also complicated the soldering of SMD boards. Irregular tin lead thickness, multiple mass soldering requirements, and difficulties in joint rework have all added to the Surface Mount Technology (SMT) soldering problems. This paper seeks to identify these problems, strategies to minimize their effects, where the SMT board requirements are headed, and what actions must be taken to meet the new demands.

Three basic types of soldering methods are commonly used to join components to printed circuit boards. They are:

1) Hand soldering
2) Flow soldering
3) Reflow soldering

Hand soldering had its major uses in the early days of the electronics industry. It was used almost exclusively to join components to the single sided print and etch circuits of the early 50s. Today hand soldering is used to repair/rework unacceptable joints formed during mass soldering or to attach special components which are chemically/thermally sensitive or have large thermal masses.

Hand soldering is generally insensitive to marginal solderability problems because of the feedback provided by the operator.

Flow soldering achieved dominance during the mid-60's when the plated-thru-hole (PTH) Printed Wiring Boards (PWB) allowed reliable solder joints to be produced in mass.
This Pin-in-Hole (PIH) joining technology has proven to be a low cost method of interconnecting components to circuits, but requires better solderability than hand soldering from both components and boards.

Reflow soldering has been developed to meet the joining requirements of Surface Mount Devices (SMD). Originally, reflow soldering was achieved by using the "Hot Bar" technique. This method worked well when only one or two surface mount components were attached per assembly, but in the early 1980s when Surface Mount Technology (SMT) begin to boom another approach had to be developed.

Since the early 1980s several approaches have been developed to do mass soldering by reflow. Three approaches used are:

1) Vapor phase - an inert high temperature vapor into which boards with components placed in deposited solder paste are immersed until the solder melts and forms a joint.

2) InfraRed reflow - in which the solder paste or preforms are melted using radiant heat from an infrared heating source.

3) Convection oven reflow - uses heated gases (sometimes inert) to melt the solder paste or preforms for joining.

The equipment and technology for mass soldering using reflow is being continually improved. The solderability demands on the SMT boards and components are more critical than with PIH technology because of the reduction in attachment surface area and the difficulty of inspection.

**PWB GEOMETRY IS IMPORTANT**

Geometry of the board and circuit features (factors related to design) has a significant impact on the solderability of SMT circuits. It has been shown that tin lead thickness has a direct effect on solderability [1]. In a PTH, when the solder is melted, gravity and surface tension withdraw the solder from the top side pad into the hole and onto bottom pad. This re-distribution of solder leaves very thin deposits on the top pad (particularly the weak knee)[2].

In surface mount, the same situation can occur if small termination pads are attached to large planes or PTHs. The resulting thin solder coatings will not resist solderability degradation well in storage.

The thickness variation caused by tin lead reflow of SMT boards not only can reduce solderability, but also causes planarity problems for surface mount device placement. To
reduce the planarity problems many SMT boards are coated with molten solder and the excess material is removed using Hot Air Leveling (HAL). This process results in solder coatings which can be more uniform than "plate and reflow", but they are significantly thinner (typically 50-150 microinch).

With PIH technology the components are generally on one side only and multiple mass soldering operations are rare. However, since the interconnects on SMT parts do not interfere with component placement, the back side can be used for additional SMDs. This occurs frequently in commercial applications.

These multiple reflow soldering operations degrade the board solderability due to intermetallic growth. If the intermetallic compounds are exposed to air even for a few seconds they will oxidize [3] and cause solder dewetting during reflow.

The situation on the surface of SMT boards is critical and causes failures, but the SMT boards also have the problems with thermal inertia during assembly. Since most SMT boards have several inner layers, each termination will experience a different heat-up rate because of differences in the copper thickness and number of inner layer attachments as well as the size and mass of the device. The time that the parts are exposed to the reflow temperatures can not be optimized for each joint, but is regulated by the most severe joint on the entire assembly. If a solder joint stays molten too long, it may dewet from the outer edge of the termination as the copper is dissolved into the solder [4].

Planck [5] has shown that, for PIH technology, when marginally solderable components are attached to solderable boards the results are poor. Only when good solderable components were used could the impact of board solderability on assembly defects be measured. For SMT boards the situation is more complicated, but it is reasonable to assume that solderability of the PWB is more important for SMT than PIH technology.

SHELF LIFE AND STORAGE CONDITIONS ARE SIGNIFICANT

In addition to the thickness of the solder over the copper circuits, several environmental elements affect the solderability of the boards during storage. The four major elements are:

1) Storage time

Storage time is a factor because it determines the amount of degradation which will occur from the other three elements. Even with no additional factors excessive storage time allow intermetallic Compound (IMC) layers to grow and the tin lead surface to oxidize, which can reduce solderability.

Storage time should be kept as short as is practical. A "first-in-first-out" stock rotation should always be used.
2) Storage temperature

Storage temperature affects the rate of almost all chemical reactions. In the case of solder, the primary reaction is between tin and oxygen. As the tin oxide forms on the surface of the solder the ability to get quick heating and fast joining of the solders from the board, paste, and component is reduced. In severe cases the oxide layer can be thick enough to prevent wetting altogether.

Storage temperatures should be moderate (70-80 F) and carefully controlled.

3) Storage humidity

Storage humidity will enhance the corrosivity of almost all oxidizers by providing a vehicle to remove the reaction products. Liquid water is corrosive to solders without any other chemicals present and condensation in the storage environment should be avoided.

The storage environment should be maintained at or below 50% relative humidity and the boards should be packaged in a low permeability plastic.

4) Pollutants

Pollutants in the storage environment, particularly in the presence of high temperatures and humidities, will attack tin lead rapidly and form a non-wettable barrier between the remaining solder on the board and the solder from the paste and component. Common pollutants may include nitrous oxide, hydrogen sulfide, carbon monoxide from auto exhausts, as well as halogenated solvents and by-products from degreasers.

All pollutants should be reduced in the storage environment.

SOLDERABILITY TESTING CAN HELP

All of these factors apply equally to both PIH and SM technologies, but the cost and ability to accomplish acceptable rework strongly favors the PIH. As the component cost and lead count continue to increase, it will become increasingly more difficult to perform cost effective rework.

In addition, it is even difficult to define when there is a need to perform rework on SMT assemblies. Soldering defects on Leadless Ceramic Chip Carriers (LCCC) are mostly hidden from visual inspection and difficult to repair after they are identified.

Most board fabrication specifications require the manufacturer to meet some minimum level of solderability before delivery. However, solderability can be lost due to:

1) Post fabrication modification of the boards - thermal plane bonding, legend application, etc.
2) Handling after testing - transport from the fabricator and incoming inspection

3) Storage - environment and time

4) Pre-soldering bakes

None of these factors are under the board manufacturer's control.

Few soldering assembly operations routinely perform tests on boards, either "as-received" or "before-use". Because board solderability is a small portion of total PIH soldering problem and rework is relatively easy and effective, the users have come to accept the moderate variations in board solderability as the rule. However, as SMT expands it is less and less cost effective to assume that the boards are solderable and most assembly operations are beginning to do inspection at receiving and before use.

The methods used for solderability testing of SMT boards are not clearly defined in the current specifications. The IPC is updating IPC-S-804 to include specific samples and techniques to test the surface mount terminations. Generally, "fabricators" are using some variation on the "dip and look" test to assess the solderability of SMT boards, while assembly operations are using "use tests" in which solder paste is applied and the board is reflowed in their typical production process.

Several companies are evaluating the Wetting Balance as a replacement for these qualitative tests. The Wetting Balance has the advantage of being quantitative and usable by both the board manufacturer and the board users. Currently only a few board manufactures are working with the wetting balance.

The key to using solderability testing at fabrication is process control (not lot acceptance). At assembly, testing is a method to control risks and to certify suppliers. For both sides to gain full advantage from their investment in testing, the evaluations must be correlated to assembly results. In only a few cases has this correlation really been demonstrated.

**PROCESS CONTROL IS THE KEY AT FABRICATION**

As discussed earlier, there are two methods of applying solder to copper circuits. The first method is to plate tin lead followed by fusing. The alternate is to apply molten solder directly to the copper circuits and remove the excess material using hot air knives (HAL) or hot oil spray.

Both methods have advantages, but each suffers from one common flaw. Both methods are very process sensitive. Which means that process control is a "must" if consistent solderability and shelf life is to be obtained.

Since the solderability testing at fabrication is used for lot acceptance and only a small number of lots fail, it is easy for the fabricator to assume that his solderability is
excellent and that there is no requirement for additional effort. This is seldom the case, but due to lack of correlation between test results and soldering defects plus poor communication from users, there is little information on which to base a change in direction.

We (Texas Instruments) have found that just meeting the specifications does not necessarily meet the needs of our assembly operations. We have undertaken a long term project to reduce the process variation in tin lead plating and reflow. Reduced process variation has resulted in a better ability to correlate process data to soldering defects. In this way the fabrication process can be optimized to give the best soldering results not necessarily the best test results.

In the plating and reflow process, we have found that alloy and reflow contamination are the most significant contributors to soldering defects. Variability in alloy has been decreased by 50% in the last two years and reflow contamination has been eliminated.

The major advantage of Hot Air Leveling is that the solder thickness is more consistent over the part than the plated and reflowed process. However, the coverage is thinner, on average, which results in a short solderable shelf life for HAL coated boards. Many variables contribute to this thickness control, making it difficult to insure uniform, thick deposits using this method.

It is not possible to improve solderability based solely on the end item test results, but the data can be used to isolate and optimize fabrication process control characteristics. By identifying these key process characteristics, the fabricator can improve his ability to determine process consistency and thereby enhance the correlation between his process results and soldering defects.

**THE USERS ARE RESPONSIBLE**

Lack of correlation between fabrication level testing and soldering defects is not the sole responsibility of the supplier. First, the board supplier may be supplying a consistent (solderable) product, but due to assembly process variation the final results are still poor. Some of the user solderability impact areas are:

1) Pre-solder baking
2) Storage
3) Soldering process control (impacts soldering performance)
4) Number of soldering steps

Second, effective communication between users and suppliers is usually poor. In many cases the assembly areas have accepted significant levels of board related defects
as "good enough" and chronic problems are covered-up by high levels of rework. In other cases, information concerning defects is conveyed to the supplier more as an ultimatum instead of as a request for assistance. The result is short term "fixes" which generally translate into higher costs instead of long term solutions. In the end, effective communication can reduce costs for the user and improve profits for the supplier (a win-win situation).

The user must take the initiative to insure this "win-win" scenario works. As users, we must:

1. Insure that our incoming assessment of solderability agrees with the fabricator's results for both good and bad products. We must communicate success as well as failures.

2. Evaluate the solderability of new suppliers continuously in the beginning. As they demonstrate their control of operations the sampling can be reduced.

3. Insure that assembly process control and improvement efforts are equal to our expectations from the board fabricators. Nothing turns-off people as much as having to cover for someone else's problems. Actively pursuing variability reduction in the assembly area and communicating the results to our suppliers will not only improve productivity, but will also set the tone for the customer/supplier relationship.

4. We must request assistance, instead of issuing ultimatums. We should be receptive to inputs and requests from the suppliers. This will build an atmosphere of trust and support.

This does not mean the users should protect their suppliers. The suppliers must know exactly what is "going on" in-order to be effective and responsive. The user should be direct and helpful not evasive and accustative. The user should also expect full and complete solutions to their problems. Half truths and paper corrective actions may sound good and come quickly, but will not be very satisfying in the long run for either party.

THE FUTURE WILL BE INTERESTING

The future of surface mount technology will be power and size driven. We should expect to see lines and spaces reduced as more and more components are made available on 15 and 20 mil pitches. Component pitches will be reduced below 15 mil as new "pick and place" and soldering equipment becomes available. TAB devices and multichip modules are now at the 8 mil pitch level.

The multilayer will continue to be used for most SMT boards. The number of layers will increase as the number of I/O's increase. Ultimately heat dissipation will be a problem, so expect to see external and internal heat sinks to become common on SMT boards. As circuit density increases the PTHs will get smaller and smaller. The need for reliable
vias and higher circuit routing densities will drive buried via technology and/or sequential processing.

Solderability may be affected by the use of double sided soldering allowed by this higher density PWB technology. As the boards and components become more complex and more expensive, we will be unable to accept any significant risk in the joining process. Solderability testing will have to improve and become more predictive. The tin lead finish will have to be more robust relative to long term storage or storage time will have to be significantly reduced.

Assuming thick coatings are required using solder, as the protective finish and JIT measures can’t reduce the storage time effectively, then new finishes for SMT will become economical. Look for Palladium/Nickel or other semi-precious metal to be used to replace solder on high end SMT boards.

If JIT is effective we could see solder replaced by organic coatings particularly on high volume boards. Another driver in the coatings area, will be the board land size and the solder paste printing capability. The effective limit in printing solder pastes today is approximately 0.010 inch wide features. In the future terminations may be as narrow as 7 mils. This will require a change in the method of delivering the solder to the termination area.

One way to overcome this problem is to plate tin lead onto the termination directly without reflow. Flux could be screen printed in “block form” to temporarily attach SMDs.

As our knowledge of SMT solder joint reliability improves and the demands increase it is possible that solder may be eliminated entirely from SMT interconnects. It may be replaced by “ball bonding”, “ultrasonic bonding”, or “thermal spot welding.”

In this event, the solderability problem may become a welding or bonding problem. This would require a Gold plated termination area and, due to costs, spot platers may become common in the PWB fabrication area.

A PLAN FOR ACTION

The assessment of solderability and correlation of the results to soldering defects will be the first order of business. It is imperative that the SMT suppliers and user agree on a meaningful test method and begin to evaluate the solderability limits.

The IPC and EIA are actively pursuing the wetting balance as this test method, but results to date have been mixed and another generation of improved test equipment may be needed in-order to get this approach off-the-ground.

In addition to solderability measurement, we need an accelerated aging method which translates to a measure of shelf-life. The steam aging method appears to be significantly more severe than necessary [1], but it is the only recognized method to date. The IPC &
EIA are working together to test the limits of the steam aging capability. More work needs to be done on other approaches to accelerated aging.

Development of age resistant solderable coatings for SMT terminations will increase as the demand for "zero defect" soldering increases. Initially the work will define the true limits of solder as a protective coating. Other metals and organic coatings will be evaluated and implemented based on the solder work. Cost and process reliability will be the keys to success in protective coatings work.

Assembly areas and equipment manufactures must continue to push for more forgiving and capable soldering processes. Tench and Anderson [3] demonstrated a method to re-activate an unsolderable surface in the lab both electrolytically and chemically. Some companies are working with inert atmospheres in the soldering operations and still others are evaluating flux modifications which will allow soldering over a wider range of starting conditions. SMT assembly areas and PWB suppliers must stay in constant communication. Needs must be supported with man power and money. Problems must be solved using whichever method is most effective, and everyone must remain open to innovative ideas.

REFERENCES:


SOLDERING CAPABILITY
COMPONENT VIEWPOINT

JOHN MATHER, ROCKWELL INTERNATIONAL, CEDAR RAPIDS, IOWA
LES HYMES, GE MEDICAL SYSTEMS, WAUKESHA, WISCONSIN

SOLDERABILITY

The solderability of as-received components is variable and appears to be a function of a
number of factors, including lead finish, original basis metal condition and burn-in
history. The following are some specific items of concern:

* There is no adequate or accepted solderability test for leadless and fine pitch
  components. The Mil-Specs call out the dip and look test but this test is not
  adequate. The wetting balance may be a capable instrument, but there is no
  universally accepted test method or pass/fail criteria. In addition, the Mil-Specs
  do not recognize wetting balance testing for most classes of SMT components.

* Hot solder dipping of Mil-Spec components is a problem. If the component is solder
  dipped by anyone (including a distributor) but the original manufacturer, it is no
  longer a JAN part. This makes procurement more difficult. Hot solder dip needs to
  be an allowable finish for all the components specifications.

* The purchase cost of solderable components is easy to measure but the cost of using
  SMT components having poor solderability (cost of quality) is difficult to determine.
  As a result, it is difficult to justify the added cost of procuring the known
  solderable component and soldering performance suffers.

LEAD CONFIGURATION

The following “geometry” issues have a profound impact on soldering performance because
they relate to the lead’s position relative to the pad and the solder comprising the joint
to be made.

* Fine pitch technology in the 15 to 25 mil range creates an inspection and repair
  problem. Inspection must be done under 10 to 50X magnification and repair of
  individual terminations is virtually impossible at 15 mil pitch or smaller. Better
  upstream processes and process controls are needed so the requirements for inspection
  and repair are eliminated. If lead pitch below 15 mil is required, the attachment
  technology must change. The attachment process must be characterized, capabilities
  confirmed and assembly process controls implemented.
Adequate cleaning of fine pitch components after soldering assembly is difficult. New fluxes, soldering methods and/or cleaning processes will likely be needed to meet both the environmental imperatives and the equipment performance requirements when fine pitch components are used.

* Allowable variations in package/termination shape and size make it impossible to design a solder stencil having optimum aperture size for achieving "perfect" fillet geometry for all permitted components. Tooling for lead forming may also need to be specific to the component supplier to accommodate dimensional variations between component bodies from different sources and still meet component mounting requirements for the end product being assembled.

* There is a delicate balance between the desire to procure parts with leads already formed and the ability to successfully mount and solder the parts. This is particularly true for high lead count, fine pitch components. Component handling during burn-in testing and printed wiring assembly may destroy lead spacing and/or coplanarity, forcing the undesirable addition of a lead forming operation prior to component placement. It is incumbent on the component manufacturer to provide the parts packaged to withstand "normal" handling, storage and presentation to placement equipment systems.

RELIABILITY

All of the efforts of the assembly solder processes are focused on creating a product which provides functionality over an extended period of time. Design information and manufacturing practice must assure this reliability.

* Industry knowledge is incomplete regarding "what constitutes a reliable solder joint." Except for a few obviously bad joints, inspectors and technologists do not know what should be reworked and what should be left alone. More research is needed on this subject and computer based predictive tools need to be made available to the product designers so that land/lead relationships can be designed into the product to provide for long term reliability. The major factor determining solder joint reliability is design of the component and product for the environment. With this in mind, it is also necessary to provide a lead/land relationship that provides an acceptable process window to carry out the assembly and soldering process.

* The application of a gold finish should not be permitted in the area of the component lead/termination where the solder fillet will be forming. This would remove the concern over gold embrittlement of the solder joints and eliminate the need for user lead forming and/or subsequent lead damage in solder dipping operations. Development of cost effective selective plating techniques is required.

* The permitted heat up rate of ceramic bodied components is a heavily debated issue and needs resolution. If slow heatup rates are needed, then soldering process
equipment will need modifications. More investigation should be undertaken to confirm or put to rest the perception that the slower heatup rates are required. Use of the slower heatup rates not only can have an adverse impact on competitiveness, it also results in the exposure of all component terminations to extended time at elevated temperature. This exposure can lead to degradation of the lead/termination surfaces with resultant negative effects on the solder joint quality and reliability.
SOLDERING CAPABILITY
PWB ASSEMBLY VIEWPOINT

BILL COBB, ROGER VEST, DAVID SPITZ
TEXAS INSTRUMENTS INC., AUSTIN, TX

SOLDER PASTE ISSUES

Stencil Design

There is one key design factor that significantly impacts the paste quality in PWB assembly. This factor is pad design (or size) of stencil openings. There is a direct correlation between the stencil thickness and stencil opening. Consider for a moment that each stencil opening has a surface area around the sides of the opening. The solder paste normally sticks to the PWB during normal printing process (one of the solder paste controlling factors is tackiness). The stencil wall area is also competing for retaining this solder paste. There is a method of predicting which of these two forces will prevail. This is referred to as the “80% RULE”.

Exceptions to the 80% rule do occur, but sporadic solder printing problems (here today-gone tomorrow) have also been noted. No problems associated with design have been found when the 80% rule is used. A few dimensions will be identified to perform this 80% rule calculation.

Stencil thickness = T
Stencil X-opening = X (assuming rectangular pads)
Stencil Y-opening = Y (assuming rectangular pads)
Stencil print area = X * Y square inches
Stencil wall area = 2T * (X + Y) square inches

NOTE: Calculations for oval pads are done with similar math using standard.

The 80% rule simply states that the ratio of:

Stencil print area / Stencil wall area = must be greater than or equal to 0.80

For example: A stencil thickness of 0.010 and opening size of 0.020 x 0.050 yields the following results:

Stencil wall area = 0.010 * 2 * (0.020 + 0.050) = 0.0014 sq.in.
Stencil print area = 0.020 * 0.050 = 0.0010 square inches

Stencil print area 0.0010 / 0.0014 Stencil wall area = 0.71 or 71%
This example "WILL NOT" reliably print. There are several factors that can be changed in stencil opening design to make the features printable: 1) Stencil thickness 2) X dimension or 3) Y dimension. Table 1 shows a matrix of opening sizes from 0.010 (10) to 0.070 (70) in the Y dimension and 0.008 (8) to 0.016 (16) in the X dimension.

This matrix table shows typical values used for 0.025 and 0.020 pitch pitch component land sizes used today. Again referencing Table 1, one will find that a pad size of 10 x 35 with a 0.005 thick stencil offers a 78% rule and will not reliably print. Increasing the Y dimension to 0.045, however, offers a size that is correct. Table 2 offers identical X and Y sizing but offers a 0.006 thick stencil as an option.

Any value less than 0.80 will not reliably print in a manufacturing production environment. Problems experienced can often be traced to violations of this 80% rule. Other factors (i.e. solder paste quality) will also impact the printability, but stencil design will not be a factor when the 80% rule is used.

### TABLE 1
**STENCIL THICKNESS 0.005**

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Note: All values below line are acceptable.

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**STENCIL THICKNESS 0.006**

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Note: All values below line are acceptable.
Solder Paste Quality

Work Life

The work life requirement for a solder paste is largely a function of the type of assembly being built and the type of pick and place equipment available. The solder paste must retain tackiness so the parts stay in place during the pick and place operation. Relatively simple assemblies can be populated in a single pass, and therefore, only a short work life (2-4 hours) is required. However, more complex assemblies with a large number of unique part types may require multiple passes through the pick and place equipment. Work life requirements of 12-24 hours are not unusual for these type applications.

Viscosity

The desired viscosity for a solder paste depends upon the feature sizes being printed. Typical paste viscosity for printing standard pitch features (0.050") is in the 600-700K centipoise (cps) range with a metal content of 87-88% by weight. For fine pitch (<\=0.025") applications higher viscosity pastes (1.0-1.3M cps) are usually used. Metal content for these pastes range from 90-91%. The higher viscosity pastes reduce slump and squeeze-out between pads which is of more concern on fine pitch components. However, they are also more difficult to print.

Particle Size

Much like viscosity, the particle size desired in a solder paste is a function of the feature sizes being printed. For standard pitch applications, -200/+325 mesh pastes are typical, whereas -325/+500 mesh particle sizes are used for fine pitch. The larger particle size pastes usually exhibit less solder balling at reflow than do smaller particle size pastes. This is due to the smaller overall surface area per volume of the larger particle pastes. The greater the surface area, the greater the oxidation of the particles, and oxidation of the particles can lead to solder balling. However, printing the large particle pastes onto the smaller fine pitch features is very difficult and if an acceptable print is achieved, the fine pitch components have a tendency to "roll around" on the larger particles.

Printability

Various factors must be considered when examining the printability of a solder paste. The texture of the paste must be such that it "rolls" in front of the squeegee during printing. This allows the paste to fill the cavity of the stencil. If the paste is too dry, it will not fill all the cavities, resulting in skips. If the paste is too loose, bridging between adjacent pads may result. Even if an acceptable print is achieved, consideration must be given to the tendency of the paste to slump after printing. Excessive slump most often results in solder bridges after reflow.
Wetting/Cleanability

The solder paste used in an SMT operation should have sufficient activity to promote good wetting on all surfaces to be soldered. The activity required will depend on the wetterability of the components and PWB, the level of oxidation of the solder particles, as well as the type of reflow equipment being used. On the other hand, the activity of the paste should be limited so that adequate cleanliness levels can be achieved, both visually and ionically. This will depend greatly on the type and cleaning power of the cleaning system after reflow.

Rosin-based RMA type solder pastes have typically been used for SMT reflow. They have sufficient activity to promote good soldering in most cases, yet they are very safe from a cleanliness standpoint. However, with the push to eliminate the use of CFC based solvents (the solvents typically used to clean RMA flux residues) other, more aggressive solder pastes are being developed which can be cleaned in water only environment. If these types of pastes are used, care must be taken in the selection of cleaning equipment so that acceptable cleanliness levels are achieved.

COMPONENT ISSUES

Composition

The two common compositions for component bodies are plastic and ceramics with plastic bodied components being used primarily for commercial applications and the ceramic bodied components being used primarily in the military applications.

The plastic bodied devices are more user friendly because the leads/terminations do not require pre-tinning and these components are compatible with the more common FR-4 PWB material.

One disadvantage of the plastic devices is the need to control the large devices against moisture adsorption. If the devices are not received in moisture-proof packing, then baking is required. There are two problems associated with the baking. First, the handling can create bent pin problems. Secondly, there is little commonality among the various vendors relative to the required time and temperature of bake. and the component vendors are reluctant to approve any bake cycle other than the cycle they chose to use.

Lead Planarity

Several manufacturing experimental studies have been done to confirm the following lead planarity recommendations. In general, it is felt there is a conflict between what the semiconductor industry can cost effectively achieve in lead planarity versus the requirement specified by the PWB assembly industry.
Planarity has a definite impact at assembly yield. For 0.050 mil pitch devices (regardless of lead type - gullwing or J lead) the acceptable standard is 0.004 inches. Some industry trends offer a +/- 0.002 number, but this does not represent a number that can be readily verified by different measurement devices or techniques.

One mechanism that offers a more universal measurement technique is to lay the device on a flat seating plane. No lead shall rise above this seating plane (at rest) more than 0.004. Fine pitch devices (0.025 or 0.020) have different requirements however. The leads are thinner, narrower, and often shorter. Planarity required for 0.025 devices is 0.003 or less. For 0.020 devices the planarity required is 0.0025. Many vendors balk at these specifications due to the fact that: 1) these specs are not easy to achieve 2) current lead forming tools and technology create many scrap devices at these levels and 3) most fine pitch devices are often large high value components.

It becomes an economic industry interest in trying to use any and all devices (even if the above specifications are slightly violated), but much rework effort is usually expended by PWB assembly operations in trying to correct for coplanarity problems. Single sourced parts often lead to few alternatives, but are made to work with assembly rework techniques and additional expended costs. Recomining operations with stamping dies have been used with some success in several operations, but cost and unique dies per component often make this alternative unattractive over normal rework techniques. Lead time for designing and fabricating these die tools also makes them less attractive as a normal alternate recovery technique.

Lead Configuration

Two common lead configurations exist for most fine pitch components. These two are gullwing and J lead. Exotic spring clip mechanisms exist for converting leadless to leaded but these are not included in this discussion. Gullwing devices have achieved a greater following in component choice over the older J leaded format. One exception, however, is memory components where J leads are still favored. One may ask why this anomaly? The reason is for component density.

J leaded memory devices can be packaged in tighter density than gullwing devices. SIMM memory modules are one example. J leads did have some bad press when initially introduced with "wicking" and "coplanarity" and probably several other initial Surface Mount Technology introduction problems. Lead forming is one other cost advantage the gullwing devices have over the J formed leads.

Gullwing devices have long foot, short foot, and several have almost no foot length. The industry specification does not have tight enough tolerances, especially when EIA-J and JEDEC specifications are compared. The same device from different vendors often does not fit on the same footprint. Trying to design a footprint that is universal in nature, flexible with alternate component vendors, often only degrades manufacturability and impacts yields at SMT assembly. Some memory J lead devices have a very similar problem.
That is non-exacting multiple vendor compatibility at the expense of assembly yields. When was the last time you heard of 100% SMT assembly yields? Component lead style and sizes are one large factor in the fishbone chart of causing problem factors.

**Lead Pitch - Machine Capability**

There are several generations of SMT assembly placement machines now in existence in the SMT industry. A fair statement is that machines that were not accurate enough for 0.050 pitch component placement are probably not still in production. Fine pitch, however, demands a new set of requirements.

Devices with lead pitch of 0.025, or less, require SMT placement machines with the following capabilities:

1) Vision based PWB fiducial recognition/correction equipment. Some equipment is sold with this as an option. Never consider fine pitch placement equipment without this being at least an option. PWB’s are fabricated with several kinds of stretch and shrink factors.

Even the routing or die blanking operations at final fab offer dimensional differences between boards of the same manufacturing lots. Simply relying on calculated dimensions or features do not have the repeatability required for fine pitch component placement.

2) Component centering capability. Many machines rely on mechanical centering; others have vision recognition. There are industry conflicting options on the merits or weaknesses of these two techniques. If one considers that if the components being placed never are touched by any mechanical devices, there is no chance of damage.

Mechanical centering techniques, however, always leave diagnostic repairmen questioning whether the centering devices are worn, miscalibrated, or otherwise maladjusted. Vision has been shown to be a significant centering advantage over mechanical centering, even after initial cost is comprehended.

3) Machine accuracy. This is another factor that industry leaders do not agree on. What accuracy is required for 0.025 lead pitch? It depends on lead width, pad land design, and component lead straightness specifications. One can compensate for several of these factors with footprint design and often lessen the exacting placement accuracy required. An exacting design requires even more exacting accuracy. As the lead pitch goes down (i.e. 0.020), the required machine placement accuracy also increases.
Typical numbers found in industry are that placement accuracy should be at least 1/10 of the lead pitch. For example, 0.025 devices require a machine with +/- 0.0025 accuracy. Don't get caught in the machine accuracy/machine repeatability specification game. Use final component placement accuracy as the judge of success, regardless of where the specification problems occur.

SOLDERMASK ISSUES

Flux Compatibility

Often, compatibility problems arise between the liquid fluxes used at wave solder and the type of soldermask on the PWB. These problems can manifest themselves as hard to remove residues left on the mask surface, or more seriously, as solder webbing or solder balling. Careful consideration must be given to find a suitable mask for a particular wave solder operation.

Thick Soldermask

Very thick soldermasks (typically 4 mil dryfilms) should be avoided on surface mount PWB’s. Thick mask can cause paste printing problems due to the stencil resting on the mask instead of on the pads. This is particularly a problem on fine pitch features. Also, thick mask can cause solder skips on backside SMT components because it inhibits the solder from making contact with the pads. If a thick mask must be used, ample clearance should be given around the pads.

Tenting

Attempts are often made to tent vias with soldermask on SMT assemblies. Tenting is used to keep additional flux from penetrating under SM devices at the wave solder operation or to eliminate bridging across tightly spaced vias. Only a few classes of masks can be used for tenting, among these being dryfilms. The biggest risk with via tenting is partial tenting or cracked tents.

These conditions allow flux to be driven into vias during the wave solder operation which cannot be removed, resulting in corrosion inside the vias. This is especially of concern when aggressive, water soluble fluxes are used. Completely clearing the vias of mask eliminates the problem, but the cleaning systems after wave solder must have adequate power to remove fluxes from beneath devices.
REFLOW METHODS

Vapor Phase

In vapor phase or condensation soldering, solder paste reflow is accomplished in an inert environment. Because of this, less aggressive flux systems can be used in the solder pastes compared with other reflow methods. Also, the level of solderability required of PWB's and components is somewhat less than with other methods. One problem noted with vapor phase soldering is the wicking phenomenon on PLCC leads.

This problem can be reduced by placing preheaters just prior to the vapor entrance, or by using specially formulated solder pastes which have a reflow delay built into them. Also of concern is the compatibility of vapor phase with water cleanable solder pastes. Problems have been seen with solder balling and splattering when using these pastes in vapor phase.

Infra-Red

IR reflow has become the reflow method most widely used in the SMT assembly industry. Both panel and lamp varieties are in wide use. One of the problems with IR is the temperature differential that develops across the board as the assembly is processed. To minimize this differential, relatively long process times are required. This puts a huge demand on the solder paste to remain active through long soak periods and into the reflow portion of the soldering process. For this reason, more active pastes are required, as are highly solderable PWB's and components.

The problem of long process times are being addressed by adding forced convection to the IR soldering equipment. This allows the temperature differential to be minimized in a shorter period of time, thus reducing total process time. The use of inert atmospheres is also becoming popular as a means of reducing the oxidation of solder particles in the paste and oxidation of the PWB's and components. No-clean solder pastes will probably require the use of inert atmosphere in IR systems to be effective.

New Reflow Technologies

New technologies are being developed to address some of the problems associated with the more established reflow methods. Full convection systems are currently being developed and used. These systems are designed to reduce the temperature differential across the board and thus reduce process time. They are also designed to use inert atmosphere if desired to either enhance solderability with existing materials or use no-clean materials. Reactive atmosphere soldering systems are also being developed, mainly to eliminate the need for fluxes and thus, cleaning after reflow. However, these systems may use some rather exotic and dangerous chemicals which may be safety concerns.
PWB FINISHES

Solder Plate & Reflow

When a pads only outer layer PWB design is used, the solder plate and reflow finish is the finish of choice. Typically, this finish exhibits excellent solderability. However, the solder is relatively thick and because it has been reflowed, it lacks flatness. While this is not a problem for solder paste printing on standard pitch, it does cause difficulty on fine pitch (< 0.025") features. Because solder paste is being printed on top of reflowed solder, the total volume of solder can be excessive for fine pitch, resulting in solder bridges after reflow.

Also, solder plate and reflow is not recommended on SMT boards where soldermask is used. Because the board goes through a reflow step, the solder on the conductors under the mask also reflows. This can lead to bridging under the mask on closely spaced conductors. Selective stripping of reflowed solder can be used but typically this will add to the cost.

SMOBC, HASL

The main advantages of hot air solder level (HASL) over solder plate and reflow are: 1) its relative flatness, and 2) it can be used on SMT boards with soldermask. However, solderability can be a problem with HASL. Because one of the goals with HASL is to yield flat surfaces to print on, very thin solder deposits can result.

In fact, in the leveling process, the solder can be stripped off down to the intermetallic compound (IMC). Once the IMC has been exposed, it oxidizes and becomes difficult to wet, even when using very aggressive fluxes.

Also, mixed technology assemblies may see up to three heating steps (PWB bake, reflow, and adhesive cure) before the thru-hole and backside SMT components are soldered. If the IMC is exposed, or the solder on the pads is very thin, extreme solderability problems may result.

In order to prevent IMC exposure or excessive solder thickness, the users would like to have a known, measurable, controllable thickness of solder after the leveling operation. Unfortunately, current conditions do not allow these desires to be obtained for several reasons:

First, the board design will normally have both very small and very large areas to be leveled, and this process will no produce a uniform thickness on surface areas of varying sizes.

Secondly, there is not a good way to measure the solder thickness. X-ray fluorescence appears to be the tool of choice, but we have experienced great
difficulty attempting to use this technique to either initially measure the solder thickness or confirm a solder thickness submitted by the supplier. Calibration and measurement drift are major barriers to precise measurements.

Thirdly, there is no industry standard that establishes a thickness range(s).

This area definitely needs additional work to establish (1) where to measure, (2) how to measure, and (3) thickness range(s).

SMOBC, Benzotriazole Finish

The main advantage of this finish is its flatness, which improves the solder paste printing operation on SMT boards. The problem with this finish is that it breaks down during the first soldering operation, allowing the copper to begin oxidizing. While this is not a concern for thru-hole only assemblies, it is for all mixed technology assemblies. The cycle time from SMT reflow to wave soldering of the thru-hole components must be minimized if solderability is to be maintained.

In addition, boards with components on the backside see an additional heating step (adhesive cure) which accelerates the oxidation of the copper. For Entek (a type of benzotriazole) coated SMT boards, aggressive fluxes are required at the wave solder operation to achieve acceptable soldering.

Also, baking of PWB’s prior to processing to prevent delamination is not recommended unless absolutely necessary.

REWORK CAPABILITY

Device Removal - Hot air is the most common means for removal of surface mount components from PWB’s. This method works well for both standard pitch and fine pitch components. Some means of process control is required for the hot air process to avoid overheating the PWB or adjacent components.

Hot air heats up boards and components more quickly and to a higher temperature than does the reflow operation. When removing components, the moisture sensitivity of the device should be considered before a decision is made to reuse the part.

It has also been found that some PWB’s are incompatible with hot air rework. These PWB’s are permanently "dished" by the localized heating of the hot air operation. This condition has been observed only on the higher layer count multilayer PWB’s (ten layers and above) and all boards of the same part number will not necessarily reflect this condition. In these instances, an alternate component removal method such as pin clip and desolder should be used.
QUALITY ISSUES

Workmanship and Quality Standards

Industry currently suffers from the lack of a comprehensive proven, and generally accepted workmanship and quality standard. This condition exists because of the newness of the technology. If this high density packaging technology advancement ever slows down, the IPC specifications have a very good start and will be the desired standard. This problem is particularly troublesome in the contract manufacturing industry and, surprisingly, few customers are aware of, or use, the existing IPC standards.

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