SURFACE MOUNT COUNCIL

SURFACE MOUNT TECHNOLOGY

STATUS OF THE TECHNOLOGY
INDUSTRY ACTIVITIES
AND ACTION PLAN

August 1999
The Surface Mount Council is made up of key industry representatives dedicated to promoting the use of surface mount and advanced electronic packaging technology in the design and production of electronic hardware.

Council Members represent user, supplier and equipment manufacturing companies engaged in surface mount implementation and production for automotive, telecommunication, computer, instrument, government, consumer and medical electronics.

The mission of this Council is to facilitate, coordinate and promote the orderly implementation of surface mount technology through standardization, the development of technical documents and other means.

This annual report is published by the Council to highlight the current status of surface mount technology in the year of publication. This report also contains a coordinated Action Plan, which is defined and monitored by council members to establish key objectives, milestones and accomplishments as a benefit to the electronics industry.

Comments to the Council regarding this report may be addressed to EIA, IPC or SMTA.

Original release January 1987
First Edition January 1987
Third Edition January 1989
Fourth Edition January 1990
Fifth Edition August 1991
Sixth Edition August 1992
Seventh Edition August 1993
Eighth Edition August 1994
Ninth Edition August 1995
Tenth Edition August 1996
Eleventh Edition August 1997
Twelfth Edition August 1998
Thirteenth Edition August 1999

Published & Copyrighted by
EIA, 2500 Wilson Blvd
Arlington, VA 22201-3834
Ph: (703) 907-7500
Fax: (703) 907-7501

IPC, 2215 Sanders Rd., Suite 250
Northbrook, IL 60062-6135
Ph: (847) 509-9700
Fax: (847) 509-9798

SMTA, 5200 Wilson Road, Suite 215
Edina, MN 55424-1343
Ph: (612) 920-7682
Fax: (612) 926-1819
SURFACE MOUNT COUNCIL
STATUS OF THE TECHNOLOGY
INDUSTRY ACTIVITIES AND ACTION PLAN

EDITOR: Paul Williams, Intel Corporation

INTRODUCTION

SECTION 1
TECHNOLOGY OVERVIEW

SECTION 2
INDUSTRY ROADMAP STATUS

SECTION 3
DESIGN FOR MANUFACTURABILITY

SECTION 4
COMPONENT TECHNOLOGY

SECTION 5
SUBSTRATE TECHNOLOGY

SECTION 6
ASSEMBLY TECHNOLOGY

SECTION 7
ACCEPTANCE AND RELIABILITY CRITERIA

SECTION 8
CONCLUSIONS AND ACTION PLAN

APPENDIX

1999 Section Chairperson

Rob Rowland
Dieter Bergman
Greg Munie
Ray Prasad
Mark Bird
Foster Gray
Dan Ward
Greg Munie
Marty Freedman
David Bergman
INTRODUCTION

Dear Reader:

This is the thirteenth edition of the Surface Mount Council’s “Status of the Technology, Industry Activities and Action Plan.” The following sections review many of the changes and ongoing activities that have occurred in the last year in Surface Mount Technology.

Area array technology, commonly known as Ball Grid Arrays (BGA) and Chip Scale Packages (CSP), continues to drive advances in packaging technology. Chip-on-Board (COB) and Flip Chip technology continues to move forward as well. Other technologies of interest include Multi-chip Modules (MCM), Fine Pitch technology (FPT), micro-passives, and an increasing interest in surface mount connectors and other high density interconnects.

Companies and various supporting organizations, such as the EIA, IPC and SMTA, continue to work together to keep our industry competitive in a global market. Many of today’s technologies are too complex and too expensive for a single company to develop. Cooperation, shared visions, and shared knowledge are necessary for the continued growth of SMT. The Vision 2010 roadmap activity is one example of industry wide cooperation.

The Surface Mount Council continues to stress the importance of Designing for Excellence (DFX), i.e. manufacturability, testability, reliability, etc. Our industry must continue to accept, define and implement DFX in order to avoid Design for Failure.

This document is intended to provide the reader with a brief review and status of the electronic assembly industry, with a focus on key technical changes that have occurred in the past year. It does not replace the technical and marketing information published by other organizations. We hope this useful tool gives you a better understanding of a complex subject.

1.1 BACKGROUND

This document was created back in 1986 to highlight and focus on critical issues that challenged the implementation of complex and process intensive technologies, such as Surface Mount Technology. Many of the critical issues discussed in 1986 still exist today.

The Surface Mount Council adopted a Status and Action Plan in order to summarize, clarify and identify the problem areas we all face in converting from through-hole mounting (TH) to surface mounting (SM). Over the years more complex technologies, such as fine pitch (FP), ball grid array (BGA), chip mounting (CM) and micro-passives, have been introduced.

This status document identifies and discusses the critical problems and solutions associated with these technologies. To maintain this level of awareness, the Council will continue to update the “Status of the Technology and Industry Activities and Action Plan” annually. The ideas and concepts expressed in this document were initially prepared by focused subgroups of the Surface Mount Council and revised over the past twelve editions as the technology has matured.

1.2 COUNCIL FORMATION

The Surface Mount Council was formed in September of 1986 and is composed of a maximum of 20 industry experts who are senior personnel of electronic suppliers, users and manufacturers. The mission of the council is to facilitate, coordinate, and promote the orderly implementation of surface mount and other advanced technologies by standardization and other means. Also
participating in council activities is an Advisory Panel consisting of various EIA, IPC, SMTA, industry, and government representatives.

Correspondence to the council may be addressed to EIA, 2500 Wilson Boulevard, Arlington, VA 22201-3834, IPC, 2215 Sanders Road, Suite 250, Northbrook, IL 60062-6135, or SMTA 5200 Wilson Road, Suite 215 Edina MN 55424-1338.

SURFACE MOUNT COUNCIL MEMBERS

Martin Freedman, Chairman

Members
James Bergenthal
Kemet Electronics
Dennis Bernier
Kester Solder
Mark Bird
Amkor Electronics
Richard Boulanger
Universal Instruments
Jack Fisher
ITRI
Juergen Gamalski
Siemens
Foster Gray
PC Interconnects
Helen Lowe
Celestica
Phil Marcoux
PPM Associates
Dr. Gregory C. Munie
Lucent Technologies
Ray Prasad
Ray Prasad Consultancy Group
Robert Rowland
Radisys
Vern Solberg
Tessera
Dr. Laura Turbini
Georgia Inst. of Tech.
Dan Ward
Delco Electronics
Joe Weddington
Manu-Tronics
Paul Williams
Intel Corp.

Members at Large
Martin Barton
Preferred Designs
Dr. William Beekenbaugh
Hadco

Vianney Shiel
Airtonic Circuits

Liaison Members
Ron Boyce, Tektronix, SMTA
Edward Hale, AMT, SMCBA

Staff Personnel
EIA
Pete J. Walsh, Vice President
Bernie Aronson, Director Technical Programs

IPC
Thomas Dammrich, President
Dieter Bergman, Director, Technology Transfer
David Bergman, Vice President
Standards Technology

SMTA
JoAnn Stromberg, Executive Administrator

Past Chairs
Dr. William Beekenbaugh
Hadco
Chuck Tillett
Avex Electronics
Dr. William Beekenbaugh
Motorola
W. Bennett Conner
AMP Incorporated
D. Rayhill
Corning

Past Council Members
Martin Barton
Rockwell International
Robert Black
Zevatech, Inc.
Charles Bodine
Signetics Corporation
Tom Borkes
The Jefferson Project
Glenn Carter
MEC, Inc.

Robert Checkaneck
AT&T Tech Systems
Winston Chen
Solectron Corp.
Bob Curnings
NASA
John Endee
Photocircuits
John Evans
NASA
Skip Fehr
LSI Logic
Ken Gillo
Alpha Metals
Steve Hinch
Hewlett Packard
John Kikta
Grayhill, Inc.
Patrick J. Layden
U.S. Army Labcom
James Madison
CTS, Inc.
W. Dean McKee
Naval Air Warfare
Kenneth Ogle
Hadco Corporation
Norbert Socolowski
Alpha Metals
Joseph Spalik
IBM
Ellis Speed
DOSO
Bruce Sorenson
Hadco
Dr. Iwona Turlik
Motorola
Harvey Waltersdorf
Thomas and Betts
Edmund J. Wescott
U. S. Air Force
Bill Wun
Hewlett Packard
Dr. Tom Kennedy
Solectron
Whitney Ackerman
Universal Instruments
Section 1
Technology Overview

1.1 Technology Overview

Surface Mounting has become a mature process, and is implemented on a global basis. What started out as a new name for “planar mounting” has become the industry norm for electronic assemblies. The most obvious benefits of Surface Mount Technology (SMT) compared to older through-hole (TH) technology is increased circuit density and improved electrical performance. Less obvious benefits include reduced process costs, higher product quality, reduced handling costs, and higher reliability. Most of the SMT package types also ease assembly automation, rework and repair. Because of the complexity and density of some assemblies (e.g. intermixed components on both sides of a printed board), proper design and process control are essential if the reduction of processing costs, rework and repair are to be achieved. Also, skilled component sourcing and procurement have a profound impact on cost reduction.

Space savings depend on the type of product and the ratio of SMT to through-hole components. Space savings of 50 to 90 percent have been achieved. Some of the savings are due to being able to mount components on both sides of the printed board. However, the greatest savings occur for products that have a large percentage of integrated circuits that are available in SMT, FPT, ultra fine pitch (UFP), array surface mount (ASM) or chip scale package (CSP) mounting.

Improved electrical performance usually appears as higher operating speed and frequency. Surface Mounting Components lower the parasitic lead and conductor inductance while improving capacitance, resistance and other performance characteristics.

Reduced product costs may initially elude the novice SMT and FP user. Skill and experience are necessary to secure packaged components at reasonable prices in a configuration that matches the assembly capability, to implement and control the process, and to design the printed board for optimum manufacturability. Once these skills have been learned, costs will decrease.

Every electronic system consists of various parts: interfaces, electronic storage media, and the printed board assembly. Typically, the complexity of these systems is reflected in both the type of components used and their interconnecting structure. The more complex the components, as judged by the amount of input/output terminals they possess, the more complex is the interconnecting substrate.

Cost and performance drivers have resulted in increased component density, and a greater number of components attached to a single assembly, while the available mounting real estate has shrunk. In addition, the number of functions per device has increased and this is accommodated by using increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for both assemblers and bare board manufacturers. Assemblers encounter handling, coplanarity and alignment problems. The board manufacturers must deal with land size issues, solder mask resolution and electrical test problems.

Manufacturing products with SMT in any significant volume requires automation. For low volume, a manually operated machine or a single placement machine may be sufficient. High volume requires screen or stencil solder paste deposition systems, multiple and varied placement machines, in-line solder reflow systems and cleaners. The degree of automation in many instances is driven by the quantity and type of components being placed. The problems and solutions are different for placing millions of chip capacitors and resistors versus several hundred high pin count integrated circuits.

The heart of Surface Mount is the machine that places the components onto the printed board land areas prior to soldering. Unlike through-hole (TH) insertion machines, some surface mount placement machines are very
versatile, capable of placing many different components, while other SM placement machines are dedicated to a few component types. Placement machines use vacuum pickup tools to hold the components, and many also provide vision assisted alignment. In general, placement machines offer better speed, accuracy, and flexibility than through-hole insertion machines or other earlier generation placement systems.

Fine pitch (0.5mm) and Ultra Fine Pitch (0.4mm - 0.3mm) placement machines require greater dexterity and precision placement capability. Some of these machines cut and form the leads of the IC package at the time of placement in order to avoid component lead damage due to mishandling. This feature increases process accuracy and precision capabilities. The new array type packages are somewhat more forgiving in that the pitch of the array is large and can provide for more liberal tolerance conditions; however, chip scale package or flip chip mounting in the array format requires good process control.

Based on industry predictions one would believe that all component packages have over 200 I/Os and are increasing in I/O count. Actually, components with the highest usage have I/O counts in the 16–64 I/O range. Over 50% of all components fall into this category, while only 5% of all components used have over 208 I/Os, which may be the threshold for determining the cross-over point between peripheral leaded component style packages and array type formats. Many peripherally leaded, lower I/O count devices, such as memory and logic devices are being converted to area array packaging formats as either BGAs or Fine Pitch BGAs.

Although the percentage of high I/O components used on an electronic assembly is small, they play a big part in driving the industry infrastructure for both bare board and assembly manufacturing. These high I/O components determine the process for bare board imaging, etching, testing and surface finishing. They determine the materials used for fabrication and drive assembly process improvements in a similar manner.

The number of machines required to adequately assemble all surface mount components varies greatly depending on the type of components being assembled and the throughput desired by the manufacturer. Dedicated surface mount component placement equipment can achieve the greatest through-put; versatility and flexibility in the ability of the equipment to handle a variety of different components, reduces the speed and effectiveness of a single machine for meeting all the needs of the assembly function.

Rework and repair of components uses both new and old tools. Since the leads are Low Mass and sit on the surface of the board, little heat and time are required to remove and replace a component. Fine-tip soldering irons and hot-air jets have become the standard tools. Hot air jets that deflect the heat under the body of array packages are mandatory to remove this component type. Tool choice depends on operator dexterity, the type of component being removed, and the proximity of surrounding components. Removing a 216-pin Quad Flat Pack (QFP) requires more care than removing a 16-pin Small Outline Integrated Circuit (SOIC).

Higher product quality results from the consistency of automated placement, improved process control and the use of smaller components. Tighter process control is inherent because the complex mixed SMT/FPT/ASM/TH process demands a higher degree of control than the process for TH products alone. Tape and reel, tube cassette, or tray component packaging used with SMT permits large quantities of components to be issued to the production area without the need to sequence or repackage components, thus providing an additional benefit.

As the complexity of IC's forces the adoption of Surface Mounting, the printed board will also change. With more of the circuit customization going into silicon and with the component package size increasing, the printed board size may also change. However, the higher I/O demand will require multi-layer or high density interconnection (micro-via) designs to support the wiring needs for closely spaced devices, or to provide the escape routing from internal connections of array component patterns. Both sides of the printed board may be needed to place all the components; power dissipation on the printed board will also increase.

**Complexity Matrix**

With the advent of new IC package styles, such as the ball grid array (BGA), electronic equipment designers are carefully reviewing their options. BGA immaturity has given way to data that indicates high yield assembly processes and good field reliability reports. Positioning tolerances are more liberal, however quality is achieved
through process control as opposed to visual inspection. In addition, flip chip and chip scale packages offer added density advantages for those products that need the smaller, lighter form factor.

The following is a complexity matrix that could help establish the parameters for definition of high pin count and fine pitch. Developed by the J-STD-013 Subcommittee complexity is judged on a scale of 1 to 10, with 10 being the most difficult. The first number reflects design complexity. Some designs are simple, others are more difficult because of the number of IOs that require interconnection, and constraints limiting available interconnect area.

The second number in each matrix cell reflects the difficulty for manufacturing. Manufacturing includes the manufacture and testing of both the printed board or mounting structure and the completed assembly.

Figure 1-1 shows the matrix for packaged parts with leads or terminations around their perimeter. The second matrix in Figure 1-2, shows the relationship or evaluation of parts with their leads or terminations on the underside of the package in an array format.

**Figure 1-1**
Component Packages with Leads Around Perimeter

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>Pitch</th>
<th>2.54mm</th>
<th>1.0mm</th>
<th>.63/.5mm</th>
<th>.4/.3mm</th>
<th>.25 &amp; Less mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 68</td>
<td>1-1</td>
<td>1-3</td>
<td>1-6</td>
<td>3-8</td>
<td>4-10</td>
<td></td>
</tr>
<tr>
<td>70-136</td>
<td>1-1</td>
<td>1-4</td>
<td>1-7</td>
<td>3-9</td>
<td>5-10</td>
<td></td>
</tr>
<tr>
<td>138-408</td>
<td>7-1</td>
<td>7-4</td>
<td>6-7</td>
<td>6-9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>410-720</td>
<td>10-3</td>
<td>10-4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>720-1000</td>
<td></td>
<td></td>
<td></td>
<td>Not Practical</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 1-2**
Component Packages with Leads Underneath in Array Format

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>Pitch</th>
<th>2.54mm</th>
<th>1.0mm</th>
<th>.63/.5mm</th>
<th>.4/.3mm</th>
<th>.25 &amp; Less mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 68</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
</tr>
<tr>
<td>70-136</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
<td>1-1</td>
</tr>
<tr>
<td>138-408</td>
<td>2-1</td>
<td>2-1</td>
<td>2-1</td>
<td>2-1</td>
<td>2-1</td>
<td>2-1</td>
</tr>
<tr>
<td>410-720</td>
<td>4-4</td>
<td>4-4</td>
<td>4-4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>720-1000</td>
<td>7-7</td>
<td>7-7</td>
<td>7-7</td>
<td></td>
<td></td>
<td>Not Practical</td>
</tr>
</tbody>
</table>
Product Types

The SMC has categorized the various end use applications for electronic products into nine different product type classifications. These are:

1. **Consumer products** including games, toys, audio and video electronics. In general, convenient size and maximum functionality are important here, but product cost is also extremely important.

2. **General purpose** computers as used in small businesses and personal applications. Compared to consumer products, customers expect longer life and more consistent service.

3. **Telecom products** including telephone, switching systems, PBXs, and exchanges. These products are used in applications requiring long service life and enduring relatively harsh environments.

4. **Commercial aircraft** requiring small size, light weight and high reliability.

5. **Industrial products and passenger compartment automotive applications**. Size and function is a byword of these products. Cost is very important, provided that reducing product cost doesn't forfeit the highest achievable product quality, performance, and function.

6. **High performance products** consisting of ground-based and shipboard military products, high speed, high capacity computers, test equipment, critical process controllers, and life supporting medical systems. Quality, reliability and performance are paramount, closely followed by size and function. Cost is optimized based on alternatives for meeting these requirements, but is a secondary importance issue.

7. **Space products** include all of the products above that are built to meet harsh outer space conditions. This implies high quality and performance over a wide range of environmental and physical extremes.

8. **Military avionics products** built to meet demanding mechanical and thermal changes. Size, weight, performance and reliability are paramount considerations.

9. **Under-the-hood automotive electronic products** endure the harshest of all use environments. These products face extreme temperatures and mechanical variations. Added to this is the pressure to achieve the lowest cost and optimum manufacturability in high volume.

For ease of reference and for categorizing process applications, these nine classifications have been further bundled into three general classes of product. These are:

**CLASS 1 General Electronic Products**: Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.

**CLASS 2 Dedicated Service Electronic Products**: Includes communications equipment, sophisticated business machines and instruments where high performance and extended life are required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

**CLASS 3 High Performance Electronic Products**: Includes equipment of commercial and military products where continued performance or performance-on-demand is critical. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support systems and critical weapons systems.
In addition the IPC National Technology Roadmap recognizes Eight basic markets into which products fall. That report takes the eight basic markets tracked by most forecasters to determine industry size and compares them to various technology drivers. The eight basic markets include:

<table>
<thead>
<tr>
<th>Automotive</th>
<th>Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Business/Retail</td>
<td>Instrumentation</td>
</tr>
<tr>
<td>Computer</td>
<td>Military/Aerospace</td>
</tr>
<tr>
<td>Consumer</td>
<td>Telecommunications</td>
</tr>
</tbody>
</table>

The market analysis recognizes that much of the equipment produced by the OEMs within various market segments differs dramatically. The OEMs have identified, through the National Electronics Manufacturing Initiative (NEMI) roadmap, that the products that they design can be further segmented into five basic technology drivers. These technology drivers are:

- Harsh environment - automotive under the hood, military, avionics electronics
- Cost performance - personal computers, servers, high-end games
- High performance - supercomputers, high-end workstations
- Low cost/high volume - camera, entertainment, mini-cam
- Handheld portable - cellular phones, sub-notebooks, PDAs

Figure 1-3 shows the relationship of the eight basic markets and their counter-coordinates reflecting the five technology sectors. It can be stated that every market has at least one product that fits into one of the technology sectors.

![Figure 1-3](image_url)

**Figure 1-3**

*Industry Markets/Technology Sectors*
Assembly Types

The SMC and IPC documentation on Printed Board Component Mounting, IPC-7070, J-STD-013, and the National Technology Roadmap for Electronic Interconnections includes the following classification scheme for surface mount assemblies:

- **Type 1** - Components (mounted) on only one side of the board or interconnecting structure
- **Type 2** - Components (mounted) on both sides of the board or interconnecting structure
- **Class A** - Through-hole component mounting only
- **Class B** - Surface mounted components only
- **Class C** - A mixture of through-hole and simplistic surface mounting
- **Class X** - Complex intermixed assembly, through-hole, surface mount, fine pitch, BGA
- **Class Y** - Complex intermixed assembly, through-hole, surface mount, Ultra fine pitch, CSP
- **Class Z** - Complex intermixed assembly, through-hole, Ultra fine pitch, COB, Flip Chip, TCP

Within the type 1 and 2 classifications there are subsets describing assemblies according to process complexity. These are subjectively listed as either simple or complex thus, a Type 2C complex assembly is one that has both through-hole and surface mount components mounted on both sides of a packaging and interconnection structure (See Figure 1-4). The assembly flow for these methods are described in section 1.

All of the classifications for performance, environments in which equipment is intended to operate, or complexity of the product are intended to facilitate communication through-out the supply chain.
Figure 2-3 Electronic Assembly Types

**Type 1** Components (mounted) on only one side of the board

Through-hole

SMT

SMT/TH

THT
SMT
FTP
BGA

**Type 2** Components (mounted) on both sides of the board

2-Sided Thru-hole (NOT RECOMMENDED)

SMT
FPT

TH/SMT

SCP
THT
UFTP
COB
TAB
Flip Chip

Legend:
- Class A = Through-hole component mounting only
- Class B = Surface mounted components only
- Class C = Simplistic through-hole and surface mounting intermixed assembly
- Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch BGA
- Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
- Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

Figure 1-4
Electronic Assembly Types
Device and Interconnect Alternatives

The electronics industry has evolved from using through-hole assembly technology in which the component leads went into the printed board substrate and were either soldered to the bottom side of the board or into a plated-through hole. Surface mounting technology (SMT) has advanced to a stage where the majority of electronic components manufactured today are only available in SMT form. Manufacturing products with SMT in any significant volume requires automation. For low volume, a manually operated machine or a single placement machine may be sufficient. High volume SMT manufacturing requires special solder paste deposition systems, multiple and various placement machines, in-line solder reflow systems and cleaning systems.

The heart of surface mount manufacturing is the machine that places the components onto the printed board land areas prior to soldering. Unlike through-hole (TH) insertion machines, surface mount placement machines are usually capable of placing many different component types. As design densities have increased, new SMT package styles have evolved. Examples are fine pitch technology (FTP), ultra fine pitch technology (UPT), and array surface mount (ASM). This latter category consists of the many families of ball or column grid arrays and the chip scale packages (CSP) and Fine Pitch BGAs. These parts are all capable of being placed by machines provided that the equipment has the required positioning accuracy.

Surface mount packages, particularly those with leads on all four sides, solved many of the problems. In addition, new computer-aided design tools made it possible to quickly design Application Specific Integrated Circuits (ASIC), providing a greater degree of circuit integration, however driving lead count up. At the same time the market forces for miniaturization kept the maximum device package size from increasing. The result has been a steady decrease in lead pitch for SMT devices from 1.27 mm (0.050 inch) to 0.63 mm (0.025 inch) to 0.5 mm (0.020 inch). The trend towards lead pitch reduction has continued to 0.4mm and 0.3mm, often referred to as ultra fine pitch.

Increased device complexity has been a primary driving factor for SMT. In order to keep the component package size down, component lead spacing was decreased. (e.g. 1.27 mm to 0.65 mm). Further increases in semiconductor integration requiring more than 196 I/Os, can drive packages to even closer perimeter lead spacings such as 0.5 mm, 0.4 mm, 0.3 mm, and 0.25 mm. However, the array package format has become the favorite for high I/O count devices. Area array component package styles have a pitch that is much larger than the equivalent peripherally leaded device and is therefore more forgiving during the assembly processes.

Ball and column grid arrays were standardized in 1992 with 1.5, 1.27 and 1.0 mm pitch. Fine Pitch BGA array packages standards have established pitches of 1.0 mm, 0.8, 0.75, 0.65, and 0.5 mm and there are proposals to go to 0.4, 0.3 and 0.25 mm. The via pattern for the board requires much tighter feature control as the pitch for BGA, FBGA and CSP becomes smaller.

JEDEC has developed industry standards for BGA mechanical outlines. The component packages are available in a plastic or ceramic configuration as well as some that have been thermally enhanced. The Chip Scale Packages can also be thought of as miniature BGAs. The package size is smaller and the I/O pitch is less, but the same principals for interconnecting the IOs and the assembly issues apply.

There is a question as to how many lead pitches are required between 1.0 mm and 0.5 mm. Some indicate that a 60% rule is of value where the ball is 60% of the pitch diameter. This results in a 0.5 mm ball diameter for a .08 mm pitch. FBGA would use a 0.4 mm ball diameter for a 0.65 mm pitch. On the other hand, some feel that it
would be better to standardize a 0.3 mm diameter ball for all FBGA packages. The motive is to facilitate PWB routing and help standardize socket contact design.

**Figure 1-5 Area Array I/O Position Comparisons**

Area array packaging has the intrinsic value of making coherent designs. This is exemplified on the right side of Figure 1-5, where a single pitch may be depopulated to meet the requirements of the design. The trend illustrated on the left side of Figure 1-5 will force the creation of many different test sockets. Wireability is affected both by ball pitch and ball diameter. The standard ball diameter as specified by the US JEDEC Committee alleviates pressure on the substrate design. The selection process for an electronic assembly should attempt to minimize the variation in component package types and the I/O pitch condition.

The conductor routing stresses imposed by BGAs, place additional demands on the printed board or P/I structure routability and require higher wiring density to allow the leads from inner land rows to escape. Typical array spacings are 1.5mm (.060in.), 1.25mm (.050in), 1.0mm (.040 in.) for standard BGAs and 0.8mm (.032 in.), 0.75mm (.030 in.), 0.65 mm (.026 in.), 0.5 (.020 in.) for miniature BGAs or Chip Scale Packages.

As pitch decreases, so does the wiring space between vias, and additional layers may be required for conductors to escape from inner rows. This demand has lead to the development on High Density Interconnecting (HDI) structures. Similar to standard printed boards the HDI structures have additional surface layers that incorporate very fine holes called micro-vias. These added layers become part of the multilayer structure and provide the additional needed high density conductor routing and interconnection capability. Holes are produced using chemical etching, plasma etching, or lasers to produce holes as small as 50 µm (0.002 in.) Micro-vias are produced using non-mechanical means and have been defined as any hole (prior to plating) that is equal to, or less than 150 µm (0.006 in.)

The large I/O count devices and problems with assembly of finer pitch peripheral packages has caused rethinking of the packaging style vs. the assembly complexity relationship, and the printed board interconnection and surface characteristics. The concern in using these very complex parts relates to board design and assembly issues. Assembly is concerned about attaching all the leads to the mounting structure without bridging (shorts) or missing solder joints (opens). Design is concerned with interconnecting all the leads and having sufficient room for routing conductors.

Array packages permit a variety of ball configurations, e.g., staggered positions or partially populated parts, to provide the room required for adequate conductor routing. With a common base array pitch significant advantages could be gained in terms of providing a coherent standard for all of the elements of the electronic manufacturing infrastructure for components, sockets, substrates and test systems. See Figure 1-6.
As the complexity of IC's forces the adoption of surface mounting, the printed board design will need to change. With more of the circuit customization going into silicon and with the component package size increasing, the printed board size will also need to change. The higher I/O demand will require multilayer or high-density interconnection (microvia) designs to support the required wiring and to provide escape routing from the internal connections of array component patterns to the printed board. Both sides of the printed board may be required to place all the components required by the design. There will also be an increased demand on the printed board to handle the required power dissipation. Table 1-1 shows routing escape capability. As the pitch changes it becomes more difficult to produce the board, and high-density boards become mandatory.

### Table 1-1 Number of escapes vs. array size on two layers of circuitry

<table>
<thead>
<tr>
<th>Array Size</th>
<th>Total Leads</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 X 14</td>
<td>196</td>
<td>O O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>16 X 16</td>
<td>256</td>
<td>192</td>
<td>196</td>
<td>196</td>
</tr>
<tr>
<td>19 X 19</td>
<td>361</td>
<td>236</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>21 X 21</td>
<td>441</td>
<td>272</td>
<td>316</td>
<td>352</td>
</tr>
<tr>
<td>25 X 25</td>
<td>625</td>
<td>304</td>
<td>356</td>
<td>400</td>
</tr>
<tr>
<td>31 X 31</td>
<td>961</td>
<td>368</td>
<td>436</td>
<td>496</td>
</tr>
<tr>
<td>35 X 35</td>
<td>1225</td>
<td>528</td>
<td>638</td>
<td>736</td>
</tr>
</tbody>
</table>
Table 1-1 indicates the number of "escapes" possible versus the array size on two layers of circuitry and the routability of conductors between I/O. It should be noted that as the quantity of I/O increases, the ability to escape diminishes and thus more layers are required.

Using high I/O components like BGAs and Fine Pitch BGAs creates the challenge of routing all the required signal, power, and ground I/O pins to the PWB without increasing PWB complexity and therefore cost. Thoughtful package pin assignments and the package configuration considerations (pitch, ball size, ball count, and depopulation) can go a long way in making the board routing easier.

For example, signal pin assignments should be kept on the outer rows of an array package, using no more than four rows deep to facilitate routing of the printed wiring board (also known as “escapes”). A 25 mm square BGA with a 1.27 mm pitch has a 19x19 ball matrix that has the possibility to provide 361 I/Os. The outer 4 rows contain 240 pins; if a designer can use 0.5 mm lands, board routing can easily be accomplished by one conductor between lands for the 3 outer rows. Rows 4 and 5 can be routed on a second signal layer with a 150 µm conductor.

Routing one conductor between lands is very cost effective, using 150 µm conductor width and 200 µm conductor spaces. Two conductors between lands can be achieved on 1.25 mm grid using 150 µm lines and spaces at virtually no premium in cost. However, the total amount of real estate used may be higher and the performance may suffer slightly.

Using an organic interconnecting substrate to mount the bare die within a plastic BGA requires that the mounting lands on the substrate match the bonding lands on the die. The bonding lands are typically positioned for wire bonding, since this is the most popular technique. Flip chip with underfill is one of the methods used to attach the back of the die to the substrate. See Figures 1-7. Depending on the number of I/O and the lead pitch, multilayer substrate fabrication techniques may be used to translate a peripheral bonding land die, to an area array matrix of bumps, balls, or columns. The transition of chip bonding lands in an array format requires mounting the die in a flip chip configuration. This creates new challenges for the routing requirements for the organic high-density microcircuit board manufacturer.

![Image](image.png)

**Figure 1-7 Plastic ball grid array, chip wire bonded**

Flip chip and chip scale packaging is the new entry into surface mount technology. Flip chip technology (FCT) has been practiced for many years by IBM and Delco. Other companies such as Motorola are using the technology on organic printed boards as opposed to the ceramic substrates required for the original flip chip process. Identified as direct chip attach (DCA), the assembly uses an encapsulant to “underfill” the space between the mounting substrate and the underside of the chip. Using chip underfill provides added protection of the solder ball joints and increases reliability due to the reduced stress of the CTE mismatch. The IPC and EIA have developed a joint standard ANSI (J-STD-030) which identifies the properties and performance characteristics of the underfill materials. See Figure 1-8.
To accommodate a flip chip with area array I/O lands at 0.25 mm pitch, the BGA package substrate will need bonding lands at 0.25 mm pitch on the top side, and solder balls at 1.27 or 1.00 mm pitch on the bottom side. These opposing sets of lands must be connected by the BGA package substrate (High-Density Microcircuit Board) wiring and interlevel vias or PTHs. It may be necessary to have one or more interconnecting lines between two adjacent bonding lands on the topside of the BGA substrate. This is done in order to access multiple rows of the interior I/O lands for connection to the vias or PTHs for eventual connection to the solder balls on the bottom side. Very aggressive layout rules must be used, even when designing with surface redistribution layers.

**Interconnect Density Evaluations**

A wide variety of materials and processes have been used to create substrates for electronics interconnections. They all share a common attribute in that they must route signals through conductors and there are limits to their abilities in terms of how much routing each can accomplish. There are several factors that define the limits of their wiring-ability as a substrate. These are:

- The pitch or distance between the vias or holes in the substrate
- The number of conductors that can be routed between those vias
- The number of signal layers required

In addition, there is need to account for the methods of producing the vias between layers. Blind and buried vias can facilitate routing by selectively occupying routing channels whereas via which are routed completely through the printed board preclude any use of that space on all conductor layers.

Conductor and via factors can be combined to create an equation which defines the wire routing ability of a technology. Historically most components have had their leads on the periphery either on two or four sides, however newer technologies based on area array interconnection of component I/O are much more space conservative while allowing courser I/O pitches to be used. Thus, very high I/O devices will require very dense substrate routing in order to interconnect the devices.

Conductor Density Capacity (CDC) is the most common definition of printed board interconnection capability. This connectivity definition describes the total signal interconnect capacity (conductors per channel) provided by a given substrate type. It is established by counting the number of conductors located in a centimeter length on a single level (layer) of substrate. Since these conductors could come on various levels from different directions, the number of 1-cm segments of these wiring channels (channel width) are multiplied by the number of levels (layers) to finally obtain the total connective capacity of a given system. It is measured in units of centimeters of conductor length, per square centimeter of substrate.
Channel width and conductors per channel are design layout terms that refer to the distance between vias and/or component lands (channel width), and the maximum number of conductors that can be routed through each channel (number of tracks per channel). Design system capability and electrical performance requirements may influence these parameters. Examples of various channel width and track per channel combinations are shown in Figure 1-9.

![Figure 1-9](image)

**Figure 1-9**

Conductors (tracks) per channel variation

Component packaging technology, lead pitch, number of I/Os and mechanical and electrical performance all impact the design of active circuit elements and the difficulty of their interconnection to a packaging/interconnect (P/I) structure. Any analysis must estimate the amount of wiring that an active component requires (wiring demand) and how this relates to the available wiring on the P/I structure (wiring capacity). The estimate of required wiring may be based on empirical analyses, such as those by Dr. D. Seraphim of IBM, who showed that the required wiring length to interconnect multiple devices is directly proportional to the number of component terminals and the pitch between the terminals. Assuming a 50% efficiency of actual wiring length to ideal wiring length, the equation is:

\[ L = 2.25 \times D \times Ns \]  

(Eq. 1)

where
- \( L \) = Required wiring length per chip site
- \( D \) = Distance between chip sites
- \( Ns \) = Number of signal terminals on the chip

The chip site distance "\( D \)" is equal to the sum of the chip or package body size plus the spacing between chips or device packages. The equation applies to both bare and packaged devices.

Adding the simplifying assumption that the distance between devices is constant, then the required wiring per unit area becomes:
\[
\frac{L}{D \times D} = \frac{2.25 \times D \times N_s}{D \times D} \quad \text{(Eq. 2)}
\]

\[
L = \frac{2.25 \times N_s}{A \times D}
\]

where \( A = \) area needed to mount and interconnect a single chip or package

\( N_s \) is estimated at 80% of the total I/O with the other 20% being used for ground and power.

Table 1-2 shows the wiring per unit area required for three chip carrier packaging technologies as a function of I/O count. The value for \( D \) was estimated as:

\[
D = \text{Body Size (rounded up)} + 2\text{mm}
\]

The data shows increasing demand for wiring density as I/O increases and lead pitch decreases. This increase in wiring length per unit area translates into a need for a higher density P/I structure. A simple set of metrics has also been developed to estimate the conductor routing capability of the P/I structure.

A universal technique for measuring conductor routing density of P/I structures has been developed that relates the number of conductors which can be placed between plated through hole lands. George Messner of AMP/AKZO described this in 1987. His simple definition of connectivity is:

\[
\text{Connectivity} = \frac{\text{conductors/centimeter per unit length}}{\text{Centimeters of conductor/centimeter}^2} \quad \text{(Eq. 3)}
\]

This connectivity definition describes the total signal conductor channel capacity that is provided by a given P/I structure. It only requires that one count the number of conductors between PTH lands on a single internal layer located in a 1-centimeter length. The number of conductors is usually stated as one track, two tracks, or "n" tracks (conductors) between lands. For a PWB with 4 tracks per 2.54 mm (0.100in) there are 15.7 tracks/cm (40 Tracks/in.). the tracks are assumed to have unit length. Therefore, a 1, 2, or 3 track per 2.54 mm packaging interconnect structure would have a wiring density in metric and English units of:

<table>
<thead>
<tr>
<th>Tracks/2.54mm</th>
<th>Wiring Density</th>
<th>Wiring Density</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>cm/cm²</td>
<td>in²/ft²</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
<td>30</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>40</td>
</tr>
</tbody>
</table>
TABLE 1-2
REQUIRED CONDUCTOR WIRING LENGTH IN CENTIMETERS PER
SQUARE CENTIMETER OF SUBSTRATE

<table>
<thead>
<tr>
<th>Component I/O</th>
<th>1.27 mm Pitch PLCC</th>
<th>0.63 mm Pitch PQFP</th>
<th>0.5 mm Pitch FQFP</th>
<th>0.4 mm Pitch FQFP</th>
<th>0.3 mm TAB</th>
<th>0.25 mm TAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>39</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td></td>
<td>85</td>
<td>96</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>46</td>
<td>69</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>47</td>
<td>72</td>
<td>106</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>132</td>
<td></td>
<td>82</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>160</td>
<td></td>
<td></td>
<td></td>
<td>137</td>
<td></td>
<td></td>
</tr>
<tr>
<td>164</td>
<td></td>
<td>84</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>176</td>
<td></td>
<td>109</td>
<td>127</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>208</td>
<td></td>
<td></td>
<td>113</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>240</td>
<td></td>
<td>117</td>
<td>160</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>244</td>
<td></td>
<td>98</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256</td>
<td></td>
<td>140</td>
<td>171</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>272</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>296</td>
<td></td>
<td></td>
<td></td>
<td>172</td>
<td></td>
<td></td>
</tr>
<tr>
<td>304</td>
<td></td>
<td></td>
<td>122</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>336</td>
<td></td>
<td></td>
<td>148</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>376</td>
<td></td>
<td></td>
<td>151</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>432</td>
<td></td>
<td></td>
<td></td>
<td>166</td>
<td>166</td>
<td></td>
</tr>
</tbody>
</table>

The total connectivity is the connectivity per square centimeter times the number of signal layers. Using this simple logic, Table 1-3 was constructed to show the ideal connectivity for various P/I structures. This table used the term “channel” to provide the relationship between conductors (tracks) and clearances (space) requirements.

1. If Eq. 2 is used, the required wiring per unit area has already accounted for the fact that only 50% of the wiring channels are utilized. The connectivity used must be the ideal connectivity.
2. This analysis applies to internal signal layers only. Top and bottom layers are assumed to have no wiring.
Table 1-3

SUBSTRATE INTERCONNECT CAPABILITY

<table>
<thead>
<tr>
<th>P/I Substrate Type</th>
<th>Provided Connectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Centimeters/Sq Centimeter/Level</td>
</tr>
<tr>
<td>MLB glass laminate through hole PWB</td>
<td>8</td>
</tr>
<tr>
<td>(2 channel per 2.54mm 0.2mm conductor &amp; space)</td>
<td></td>
</tr>
<tr>
<td>MLB glass laminate SMT PWB</td>
<td>16</td>
</tr>
<tr>
<td>(4 channel per 2.54mm, 0.15mm conductor &amp; space)</td>
<td></td>
</tr>
<tr>
<td>Thick Film Ceramic Hybrid</td>
<td>32</td>
</tr>
<tr>
<td>(4 channel per 1.27mm, 0.125mm conductor &amp; space)</td>
<td></td>
</tr>
<tr>
<td>Discrete Wiring Board</td>
<td>63</td>
</tr>
<tr>
<td>Thin film on polyimide</td>
<td>79</td>
</tr>
<tr>
<td>(MCM-D, 50 micron conductor/75 micron spacing)</td>
<td></td>
</tr>
<tr>
<td>Thin film MCM-D on Silicon</td>
<td>130</td>
</tr>
<tr>
<td>(12 micron conductor 25 Spacing) via in Land design</td>
<td></td>
</tr>
</tbody>
</table>

Today MLB and DWB technology is being used in products to support FPT. For a 0.5mm pitch, 208 I/O QFP the required wiring length is 113 cm/cm². For a 4 conductor/channel design rule, 7 signal layers or 2 DWB wiring layers would be needed. In fact since only a few FPT devices are used the average wiring demand is less than the 113 cm/cm² from Table 1-3. The localized conductor routing demand is met by using more P/I structure surface.

It should be noted that all the previous examples are for peripheral leaded packages using standard multilayer boards or discrete wiring boards. The rules will change dramatically when one is trying to develop a redistribution layer for moving bonding sites on a bare die to an array pattern position. In addition, the routing density for escapes from the inside land pattern of array devices may not provide the traditional 1,2,3, or 4 conductor routing opportunity. (see Figure 1-10). HDI technology will play a dramatic role in changing the wiring demand capability.

Figure 1-10 Conductor routing methodology for BGA component land patterns
The diameter of the solder land can affect both the reliability of the solder joints and also the routing of conductors. Several studies have shown that larger solder lands (up to 0.8 mm in diameter) increase the fatigue life of PBGA packages. However, the larger the lands, the less room for routing between lands.

For example, a 1.27 mm pitch BGA package with 0.63 mm diameter solder lands will be able to fit 2 conductors between the lands using 125/125 µm conductors and spacing. If a 0.8 mm diameter solder land is used, only one conductor can fit between the solder lands using 125/125 µm conductors and spaces.

Tables 1-4 and 1-5 show the number of conductors that can be routed between lands for various land diameters and conductor/space widths.

### Table 1-4 Number of conductors between solder lands for 1.27 mm pitch BGAs

<table>
<thead>
<tr>
<th>Solder Land Diameter (micron)</th>
<th>750</th>
<th>700</th>
<th>625</th>
<th>500</th>
<th>400</th>
<th>350</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor Width (micron)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>150</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>125</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>100</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>75</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

### Table 1-5 Number of conductors between solder lands for 1.0mm pitch BGAs

<table>
<thead>
<tr>
<th>Solder Land Diameter (micron)</th>
<th>625</th>
<th>500</th>
<th>400</th>
<th>350</th>
<th>300</th>
<th>250</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor Width (micron)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>150</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>125</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>75</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

The following equation can be used to determine the number of conductors that can routed between lands depending on package pitch (P), solder land diameter (D), number of conductors between lands (n) and conductor/space width (x):

\[ P - D \geq (2n + 1) \times x \]

Recommended solder land diameter sizes for PBGA packages range from 0.6 to 0.8 mm. A general rule is to design the solder land on the circuit board with the same diameter as the solder land on the PBGA substrate.

Solder land sizes for CBGA should be designed such that the stencil aperture will deposit a minimum of 4800 cubic mils of solder paste. This generally equates to a solder land diameter of between 0.7 and 0.8 mm. This minimum requirement is necessary to ensure reliability as all melted solder, during reflow, comes from the paste deposit.

As the size of the array increases, more and more traces from the solder balls inside the array have to be routed in between the solder balls to connect to the outside world. It is important for the substrate designers to know how many conductors they may expect to accommodate in the spacing between the adjacent solder balls so that they may determine the widths of the conductors and the spacing between the conductors. This information will help to model the signal integrity to assure the success of their application.
The number of conductors per outlet, \( C \), for a simple \( r \times c \) array can be determined by substituting \( r \) and \( c \) in the following relationship with the number of rows and columns of the given array, and by substituting \( d \) with the number of depopulated sites in the array.

\[
C = \frac{[(r-2)(c-2)]-d}{2(r+c-2)}
\]

In case the above equation provides a whole number for \( C \), every array outlet between adjacent solder balls will need to accommodate \( C \) conductors. If \( C \) is a fractional number then some outlets will have to accommodate a number of conductors obtained by rounding down the value of \( C \) and others will have to accommodate a number of conductors obtained by rounding up the value of \( C \). The fraction is the proportion of the lower and higher number of conductors per outlet.

The balls in an array can also be interspersed, as in a diagonal array. An example of a \( 5 \times 5 \) interspersed array is shown in Figure 1-10.

![Figure 1-10 Interspersed Array](image)

The following relationship can be used to determine the number of conductors per outlet for an interspersed array.

\[
C = \frac{[(r-2)(c-2)+(r-1)(c-1)]-d}{2(r+c-2)}
\]

If \( C \) turns out to be a fraction, then rounding it down will give the lower number of conductors to be accommodated between some adjacent balls, and rounding it up will provide the number of maximum conductors needed to be accommodated between other adjacent balls. The fraction gives the proportion of the two numbers.

**When To Select SMT**

At present, most products are best designed using SMT. There is a strong supplier infrastructure and many skilled users. In general, a product is a good candidate for SMT if it needs to be:

- Small in size.
- Able to accommodate large amounts of memory.
- Light in weight.
- Able to accommodate several large, high lead-count complex ICs (such as ASICs and silicon arrays).
- Able to function at high frequencies and speeds.
- Able to transmit little or no noise, EMI or RFI.
Able to be built in large quantities using automation.

If a product does not have to meet the criteria above, then a more detailed examination of size, cost and performance projections may be in order. This involves simply comparing the SMT version of the product with the other alternatives. Fortunately, this can often be done without physically designing and building the SMT and the alternate versions.

Currently, most SMT boards that have 50 or more components use a combination of SMT and through-hole technologies. The mix is a function of component availability, multiplicity of suppliers, and cost. A mix of 85 percent SMT and 15 percent TH parts is very common, even for boards containing up to 1,000 components. As a result, most companies install a combination of SMT (placement and reflow) and through-hole (insert and wave) assembly capabilities.

**Impact of Fine Pitch Technology (FPT) 0.5mm Pitch**

Fine Pitch Technology (FPT) is really a process rather than a packaging technique, since the package to board assembly steps are different than standard SMT. For example, several of the commercially available FPT and TCP parts require lead excise and forming prior to placement; also most packages are encapsulated or molded with plastic and delivered to users as a separate packaged device. FPT packages are available under package names such as PQFP (Plastic Quad Flat Pack), CQFP (Ceramic Quad Flat Pack), QFP (Quad Flat Pack), VSOIC (Very Small Outline Integrated Circuits), and TCP (Tape carrier Package). in a molded ring that is used by the placement machine to deliver the part to the board.

Any handling of the components or leads, such as during component burn-in or testing, tends to aggravate the coplanarity or lead straightness problem. The leads are in the ideal position immediately after they are trimmed and formed. Because of this, it is best to do the lead forming operation as the devices are placed on the interconnecting substrate for soldering.

Fine pitch devices are also attached to the interconnecting substrate using hot bar, hot gas, laser or focused IR reflow, or thermocompression welding. The assembly equipment must also prepare some of the component types by excising the device out of its carrier and forming the leads for the outer lead bond area. Currently, the trend is to do direct attach, where the leads are soldered or welded to the substrate during the placement cycle. Hot bar soldering, where entire rows of components are attached simultaneously, is most often used.

During the reflow process using Hot Bar, the bar tends to push the component leads downward thus minimizing coplanarity problems. Plastic packages with soft copper leads can be deformed in this manner with no reliability impact. Stiff leads such as Kovar can cause plastic deformation of the solder due to residual stress in the soldered leads that can lead to open circuits. Convection reflow utilizing pre-fused soldered boards is a candidate for the future to accomplish high volume outer lead bonding of several components simultaneously.

Mass reflow of FPT along with the BGA and SMT parts is also possible, but requires greater control of solder paste volume, placement accuracy, and reflow thermal energy. Generally, less solder paste is deposited on FPT and BGA lands than on SMT lands to avoid solder shorts.

Convection reflow utilizing Solid Solder Deposited (SSD) interconnecting substrates (Para. 1.2.11.3) is another candidate for accomplishing high volume bonding of FPT, BGA and SMT components simultaneously. Much work is presently in progress to make the concept of “Solder-Bumped Boards” (the jargon for SSD technology), a production reality.

With the proliferation of packages, solutions are evolving to overcome problems commonly experienced with high lead count/fine pitch part combinations. One of the solutions is to move toward array type packages, such as the BGA, or miniature BGA packages. The industry is starting to provide cash memory devices in the miniature BGA
package. There are not many I/Os so the location of the balls are sometimes provided at in-line locations, never-the-less the routing and assembly challenges prevail for these parts as they do for fully populated arrays.

**Impact of Chip Mounting Technology (CMT)**

Although used for many years in hybrid assembly, direct mounting of Integrated Circuits devices on a variety of substrate materials is an emerging technology in many products. CMT is an alternative to conventional fine pitch technology; its main purpose is to increase the chip interconnect density to the substrate. CMT is most often combined with other assembly technologies (THT/SMT/FPT/ASM) to achieve the product manufacturer's packaging goals.

CMT also requires extra substrate processing to accommodate either the wire bond or other direct chip attachment process without intermediate leads between the chip pad sites and substrate land pattern. Some of these include selective plating of gold, fine conductor substrate processing with 0.1 mm conductors and 0.1 mm spacings at the interconnect site, and depositing micro amounts of solder and flux.

Wire Bonding is used in hybrid assembly and in printed board attachment (Chip-on-board - COB) - This process attaches the bare IC die directly to the substrate, circuit side up, usually with a thermally conductive adhesive. The IC pad sites are then wire-bonded to the substrate land pattern using the same conventional technique as used in "packaged" IC components where the IC pads are connected to a component lead frame. For COB a gel coat of high purity resin is normally applied over the bare die and wire bonds for protection; hybrids are normally sealed with a lid over the package.

Flip Chip technology, often referred to as C4, (Controlled Collapse Chip Connection) usually requires the IC die pad sites to be prepared for solder metallurgy. The sites can be either on the periphery of the die or internally to form an area array for higher density interconnects. The IC die is placed on the substrate, bumps down, and then heated to allow the solder bumps to reflow with the substrate land pattern. A column of solder is formed between the IC die and land pattern. The process must be precisely controlled to form the correct column shape and to prevent opens and shorts among the closely spaced connections. The differences in the Coefficient of Thermal Expansion (CTE) characteristics of the IC die and substrate material must also be taken into consideration.

A major obstacle to CMT in the form of mounting bare chips is the availability of bare tested IC chips in a wide range of device types. Most component suppliers are reluctant to ship bare die in wafer format or some other protective package such as matrix tray. The question of who takes responsibility for die that fail testing after assembly still needs resolution. In the case of the COB, Flip Chip or unique TAB, the product manufacturer is doing the "final packaging of the IC". Any component supplier will admit that there is fallout during this manufacturing step. Is it the die or the attachment process that was bad? Currently these technologies are often the domain of the vertically oriented companies both producing and using the bare IC die.

Several new approaches have been developed that provide redistribution patterns and make these interconnections under the die. These packages come in a variety of configurations and are known as chip scale packages. The interposer fans in to a pattern of solder bumped flexible material. Similar to tape automated bonding, this concept attaches the flexible membrane to the chip bonding sites providing a package that can be tested or "Burned-in" prior to assembly. Other techniques for chip scale packages are evolving, such as fanning out to columns or other ball configurations. The new document on flip chip and chip scale technology is J-STD-012, which highlights the design and assembly issues related to these technologies. The J-STD-012 also recommended new design and performance standards that need to be developed for the infrastructure to take hold. Committees of IPC and EIA are working to provide the needed new standards, some of them to be released in 1998.

The assembly process for chip scale is similar to the BGA attachment technique, just more precise with better process control. One major benefit is that the chip scale packages can be fully tested prior to assembly, eliminating the problems associated with known good die (KGD).
Multi-chip and Single-chip Modules (MCMs and SCMs)

Since electronic packaging reflects the increasing need for high speed/high density interconnections, many companies are turning to multichip modules to increase the performance of their packaging method.

Multichip modules have sometimes been identified as a level 1.5 packaging, which indicates that they fall somewhere between the bare IC chip (level 1) and the board packaging (level 2). Multichip modules have been a viable packaging technology since the early 1980s, especially for high performance computer companies. Many major companies that require the high performance characteristics use multichip modules as their primary packaging method.

A generic definition for a multichip module is that the MCM represents "a set of logical functional blocks grouped to maximize interconnect within a compact assembly, yet minimize interconnect to the next level".

In an effort to determine the characteristics of multichip modules and the need for standardization, the IPC Multichip Module Committee has attempted to establish definitions that coincide with the IEEE Computer Packaging Committee concepts. This liaison is most appropriate since most of the need for the performance requirements comes from the computer industry. System performance requires data processing capability in millions of instructions per second (MIPs) for general purpose machines, and millions of floating point operations per second (MFLOPs) for scientific machines.

There are two density metrics pertaining to SCMs or MCMs. The first, substrate efficiency, is measured as a percentage that the total semiconductor die occupies of substrate area. Thus, a multichip module or single die chip carrier with a substrate efficiency of 65% is one where the area of integrated circuitry equals 65% of the available substrate area of the module. Component density, the second metric, is slightly different, in that total useable component area is counted. These metrics differ in cases where: (1) inactive die are present for purposes of functional redundancy, and (2) three-dimensional components (stacked ICs) are used. In the first case, the component density is less than the substrate efficiency for the same assembly. In the second case, the component density is greater than the substrate efficiency. While it is possible by this definition to have component density > 100%, the substrate efficiency of any packaging approach can never exceed 100%.

Multichip modules use CMT and some SMT as the prime assembly methods. Several obstacles hinder the use of MCMs, the prime being CMT. CMT needs high yield ICs that are readily available from multiple sources. Currently, suppliers of unpackaged ICs are on the increase as confidence is being gained in this packaged technology.

There are several types of multichip modules. In an attempt to characterize these, three different module types have been defined to by the IPC Multichip Module Committee. These concepts are described in detail in publication IPC-MC-790 "Guidelines for Multichip Module Technology Utilization", which reflects agreement that multichip module technology cannot be defined on complexity alone.

The three categories of multichip modules that have been identified are:

- Multichip Module C
- Multichip Module D
- Multichip Module L

The definitions for these multichip modules are as follows:

**Multichip Module C**
MCM-C's are normally constructed with ceramic or glass ceramic alternative base materials with a dielectric constant of greater than 5 between signal planes or between signal planes and ground planes. These materials act as both the dielectric and supporting structure for the components.

Conductors are usually a fireable metal material, such as tungsten, molybdenum, and the screenable frit metal thick conductors of gold, silver, palladium and copper. When these materials are used to form the conductors, the conductor width is usually greater than 0.125 mm (0.005 inches).

Vias, necessary to provide the interconnection between layers, are formed during the conductor screen printing process. The vias are usually the same material as the conductor.

For most multichip module C applications the number of active elements (semiconductor I/C's) is greater than the number of passive components.

**Multichip Module D**

MCM-D's are normally constructed using deposited dielectric materials to separate the signal planes. The dimensional stability of MCM-D's is determined by the underlying substrate that is usually made of ceramic, silicon, copper, or other metals or composites. The deposited dielectric material normally has a dielectric constant less than 5 and may be deposited directly on the selected substrate, or be deposited on a metal platen and peeled off to be reapplied elsewhere. Openings for vias may be formed in the deposited dielectric layers by reactive ion etching. They may also be formed by using a photosensitive dielectric material.

Conductors and vias are sputtered or plated. The materials may be aluminum, copper, or gold. Definitions of the patterns use photolithography to provide the imaging of the conductors for etching or pattern plating. Vias are usually formed in a stair-step manner, unless a metallic fill is employed to allow stacked vias. Copper or nickel are the most common via fill materials.

**Multichip Module L**

MCM-L's are laminated modules using printed board fabrication technology. Laminated layers may be reinforced or unreinforced and consist of such resin materials as epoxies, polyimides, acrylics which may be reinforced with woven fiberglass, quartz, Kevlar, etc. The resin and reinforcement materials determine the dielectric constant.

The conductors are almost always copper. These are either additively deposited or are part of the printed board subtractive process.

Vias are copper, electroless plated initially, followed by electrolytic copper plating. When control of the coefficient of thermal expansion is required, laminate techniques use materials such as copper-invar-copper or copper-molybdenum copper or other low CTE substrates are laminated in the MCM-L to provide control of the substrate expansions.

With new HDI technology evolving the organic substrates are becoming an important element of the module development approach. The laminated concept is not only being employed for multi-chip applications, it is also being used to provide the redistribution layer for single chip or chip carrier applications. The benefit of this approach is that with proper planning in the design the packaging redistribution can accommodate several die shrink processes without changing the output pattern that the designer must consider for mounting to the next level of interconnection.

**New Standards Evolving**

Many new standards are being delivered to address the need for information on the requirements of MCMs and SCMs. IPC-2225 covers design of MCM-L, while the performance of the mounting substance is being addressed in IPC-6015. For printed boards that use High Density Interconnecting Structures the design standard is IPC-2226.
and the performance standard for the unpopulated printed board is IPC-6016. Both sets of standards will select their materials from the HDIS material standard IPC-4104. Another new document is the IPC-7095, Design and Assembly Process Implementation for BGAs. That document focuses on the critical inspection, repair and reliability issues associated with BGAs

1.2 CONSIDERATIONS FOR USING SMT

Paths For Entering SMT

There are several available paths to utilizing SMT effectively. The length of each path depends on what design and assembly facilities a company presently has, and how quickly they can be made ready for production.

Company has existing CAD or equivalent precision design capability and assembly facilities or has committed to acquire them.

[Note: It may be possible to design some simple SMT products without a CAD system, but it is not recommended.]

1. Select a list of candidate products for SMT. Most of the products will be new but a few existing TH products should be converted to benchmark the effects of converting.

2. Develop an equipment list based on the projected volume needs. If sufficient in-house expertise does not exist, it may be desirable to use a reputable training center or consultant to save cost and time.

3. Organize a team representing design, production, test, quality, and purchasing. This team is responsible for component and equipment selections and review.

4. Develop a comprehensive SMT design guide that stresses manufacturability. Use existing standards where possible.

5. Design the candidate products starting with the conversions of existing TH products.

6. Conduct rigorous assembly and test reviews. Carefully monitor component purchasing to assure components have the specified package, shipping method, metallization, solderability, and orientation in the shipping containers.

7. Develop comprehensive workmanship standards and a process control system that is statistically sound.

8. Design the remaining candidate products.

Company has existing CAD or equivalent precision design capability, but no SMT assembly facilities.

1. Select a list of candidate products for SMT. Most of the products will be new but a few existing TH products should be converted to benchmark the effects of converting.

2. Organize a team representing design, production, test, quality and purchasing. This team is responsible for the selection of components and the subcontract assembly facility.
3. Using in-house CAD or a qualified external design center, design the candidate products starting with the conversions of existing TH products. If designing on an in-house system, insure that the design rules are compatible with the capability of the subcontract assembler.

4. Conduct rigorous assembly and test reviews relying on the design for manufacturability and guidance of the subcontract assembler. If the subcontractor isn’t purchasing the components, then carefully monitor component purchasing to assure that components have the specified package, shipping method, metallization, and orientation in the shipping containers so that they are compatible with assembler's methods. Until purchasing becomes completely familiar with purchasing SMT components, it is better to let the custom assembler specify and buy components that meet his assembly methods.

5. Develop comprehensive workmanship standards and a process control system. This is important even if there are no plans to assemble internally.

6. Design the remaining candidate products.

**Design Considerations**

In general, product design is cost, size, and/or performance driven; however, other considerations may be important. The product must also meet the thermal and environmental reliability requirements.

These requirements can be met by various packaging options such as through-hole technology (TH), surface mount technology (SMT), fine pitch technology (FPT), array surface mount (ASM), chip scale packaging (CSP), chip mounting technology (CMT) or a combination of all these.

The designer faces a broad task. He or she must consider form, fit, function, cost, reliability, and time to market before choosing a particular course. A primary issue is the reliability of the final product. The product must function as intended in the working environment over the predicted life span of the equipment. Reliability depends on several factors, which will be reviewed in various sections of this report.

**Thermal Considerations**

Since surface mount component packages are smaller, they generally (not always) have higher thermal dissipation requirements, because they contain the same die as in the larger DIP packages. In addition, because of increased interconnecting substrate package density due to the smaller components, the power density per unit area of the substrate increases. In other words, SMT may compound the thermal problems for both component package and assembly. Both suppliers and users must evaluate each application for potential problems.

It is not enough to reduce the internal temperature of the electronic equipment. Rather, heat must be removed from the interconnecting substrate so that the components can operate more reliably.

Unfortunately, the thermal simulation tools for accurate modeling of thermal problems are only now becoming available. In the past, designers had to rely on empirical experience to determine the spacing between heat sensitive and heat generating components. If extra space was not available, then forced air or heat sinks were used to remove the heat.

Now, some of the new thermal analysis computer tools allow the user to build a computer model that will help identify hot spots and recommend possible solutions. Several commercial CAD systems offer excellent thermal analysis models that predict the temperature profile of a board during design of conductor routing and component placement.
Land Pattern Considerations

Components are soldered to the printed board on the surface mount lands. Lands are areas of copper approximately the shape and size of the lead or termination footprint. The land pattern design is critical for manufacturability, because it affects the solder defect rate, cleanability, testability, repair/rework and the solder joint's reliability.

In the past, component tolerances were too liberal (some still are). Additionally, since surface mount packages were not standardized, land pattern design could not be standardized. As a result, users had to develop in-house land pattern dimensions and qualify a limited number of suppliers who met those specifications. Reducing the number of suppliers reduced the range of sizes and associated tolerances required of land pattern design.

Organizations such as IPC, EIA and the Surface Mount Council worked hard in the past few years to promote standardization and tolerancing. As an example, IPC published IPC-SM-782, "Surface Mount Land Patterns (Configurations and Design Rules).” The EIA published EIA-PDP-100 and EIA-JEP-95 to provide the tolerances and dimensions for registered outlines of components. Today these two organizations are working together to provide the user with a systems concept for both components and land patterns whose tolerance conditions have been analyzed for manufacturability.

The EIA and IPC have also worked together to provide dimensioning and tolerancing criteria that considers geometric tolerancing to match the component and the land pattern. These are coupled with the tolerances for placement machines, as well as the amount of room needed for a reliable solder fillet. These data can be used by vision systems to establish criteria for acceptability of components, land patterns, placement criteria, and finally the physical solder fillet size.

In order to facilitate the use of the new land pattern analysis technique a land pattern registration system has been devised that correlates a special pattern to a specific component. Identified as registered land pattern (RLP) numbers the concept is documented in Revision "A" of IPC-SM-782. The RLP number consists of three digits, followed by a letter (if applicable) in order to facilitate revisions to a specific RLP. The revision letters X, Y, and Z have been designated for user modified land patterns for the same part; "W" is for a wave soldered process land pattern modifier, should the user feel this is necessary. In addition, the letter “V” is also a user option to identify those land patterns that have incorporated a via as a part of the land pattern design, either within the mounting land or extended as a “fan-out/fan-in” configuration.

Ball Grid Arrays have their own land pattern considerations. The patterns are considered as being related to the "True Position of the array location and the size of the ball. BGAs are divided up into two groups of pitches. The first group is regular which is 1.50, 1.27, and 1.00 mm. The second group is the fine pitch, which has the following pitches 0.80, 0.75, 0.65, 0.50, 0.40 and 0.30 mm. The present usage shows that the 1.27 as being the most popular followed by the 0.80, 1.00, 0.75, and 0.50 mm. The 1.50, 0.40, and 0.30 mm are not presently widely in use.

Pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 1-6 shows the characteristics of those balls that are used with pitches of 1.5 mm through 1.0 mm.

Table 1-6 Ball diameter sizes

<table>
<thead>
<tr>
<th>Nominal ball diameter (mm)</th>
<th>Tolerance variation (mm)</th>
<th>Pitch (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>0.90 - 0.65</td>
<td>1.5, 1.27</td>
</tr>
<tr>
<td>0.60</td>
<td>0.70 - 0.50</td>
<td>1.0</td>
</tr>
</tbody>
</table>
In each instance, component manufacturers and board designers are encouraged to reduce the land size by some percentage of the nominal ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined to be 0.1mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC). Table 1-7 shows the reduction characteristics, the nominal land size, and the target land dimensions.

<table>
<thead>
<tr>
<th>Nominal ball diameter (mm)</th>
<th>Reduction</th>
<th>Nominal land diameter (mm)</th>
<th>Land variation (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>25%</td>
<td>0.55</td>
<td>0.60 - 0.50</td>
</tr>
<tr>
<td>0.60</td>
<td>25%</td>
<td>0.45</td>
<td>0.50 - 0.40</td>
</tr>
<tr>
<td>0.50</td>
<td>20%</td>
<td>0.40</td>
<td>0.45 - 0.35</td>
</tr>
<tr>
<td>0.45</td>
<td>20%</td>
<td>0.35</td>
<td>0.40 - 0.30</td>
</tr>
</tbody>
</table>

The information shown in Table 1-7 provides data on land patterns and their variation to accommodate four ball diameters. Many component manufacturers use soldermask-defined lands. When this technique is employed, the nominal land diameter should be increased by the amount of solder mask encroachment on the land (usually about 0.1 mm). The opening in the solder mask window then represents the diameter to which the ball will become attached, while the actual land is slightly larger to accommodate the soldermask-defined land concepts. It should be noted that routing density is decreased, since the land is larger.

### Interconnect Considerations

Surface mounting has forced the industry to use fine line printed circuit boards with conductor widths down to 0.1 mm (0.004 inch) or less. As conductor spacing decreases and circuit speeds increase, the potential for circuit malfunction increases due to crosstalk or coupling of electrical energies from adjacent traces. So, now the designer must consider signal integrity issues.

As in thermal modeling tools, the interconnect simulation tools for accurate modeling of cross-coupling problems are still evolving, but an adequate variety are available to the specialist for an intelligent evaluation of signal integrity issues. First and foremost, the analysis of signal integrity issues requires an adequate appreciation of the system functionality. It is usually pointless to design a digital saturating logic system at 20 MHz in a multi-chip module with impedance control. Some rules of thumb for similar cases exist. For example, in many designs involving sub-100 MHz saturating digital logic, active circuits may be spaced at 0.15 mm (0.006 inch) or even 0.1 mm (0.004 inch) apart with no significant problems due to cross-coupling energies, provided the signal to ground plane spacing is within 0.2 mm (0.008 inch) and adjacent conductors run parallel for less than 75 mm (3 inches). When impedance control is important, then so is the careful consideration of a printed wiring board or MCM as a complex, multi-conductor transmission line system. It is important to note that many convenient “cookbook” analytic expressions and rules of thumb exist for the evaluation of signal delay, conductor capacitance, characteristic impedance, etc., but that these may lead to incorrect assessments when applied carelessly.
Multilayer structures are an important part of solving the interconnection problems of SMT, FPT and ASM. Not only do the concepts provide the electrical performance capability with impedance control possibilities and cross talk protection due to proper conductor routing, the multilayer board also allows for the fine-line conductors to be buried inside the laminated structure and thus reduce the chance of mechanical damage. Through-hole vias provide interconnection between and among the various layers; Blind and Buried vias, that only connect those layers that they traverse, allow for additional conductor routing room.

The use of microvias adds a new dimension for providing interconnectability. Using Built Up Multilayer (BUM) principles outer layers are added to the interconnecting structure. These provide the redistribution for interconnecting high density packages in order to escape from a field of highly packed mounting lands and through the use of very small plated holes (microvias) make connections to the layer below.

**Testability Considerations**

Testing of surface mount assemblies has become more difficult than conventional through-hole assemblies for a number of reasons.

1. Passive components are smaller in size and generally leadless.

2. The peripheral leaded semiconductor packages have a large number of leads on 0.5 mm, 0.4mm, and 0.3mm lead centers instead of 2.5 mm and 1.27mm centers as in past designs.

3. The increased use of array packages, both BGA and mini-BGAs require fan-out of the vias in order to obtain test point access that avoids high probe point pressure areas.

4. The increased component densities result in components placed closer together and mounted on both sides of the printed board.

5. Lack of test access (through-hole assemblies automatically provide test access on the solder side of the board).

It is for these reasons that testability must be considered at the early stages of product development, while the board is being designed, NOT after the design is complete!

Design for testability is one of the most important duties confronting a product designer. The conscious commitment for a testable design can be engaged at the board, component, circuit design, partially assembled and fully assembled level (not necessarily in that order). It can be as simple as introducing additional test access points or jumpers on the board, or it can be as complex as utilizing IEEE 1149.1 or equivalent boundary scan design methodologies at the board level. As in the case of through-hole designs but, as expected, achieving higher fault coverage comes at a price -- literally. The investment clearly pays off, however, particularly for complex designs in volume production.

There are a number of issues that arise when considering the test inspection and measurement of increasingly complex substrate interconnections especially when involved with the electrical evaluation of the substrate. In order for the manufacturer to be able to reduce cost while adequately assuring the electrical function of the substrate interconnection, the customer will have to provide definitive test data, with the preference being 100% netlist testing.

Compatibility of the data is currently an issue as well. It is hoped that industry standardization efforts will help to solve this issue in the foreseeable future. One item which could prove key to achieving this is likely to be
acceptance of a standard base grid pitch, which would allow test equipment and socket manufactures to examine and focus on creation of a universal solution.

The use of fixtures and bed of nails testing for opens and shorts testing is quickly losing the ability to meet test requirements as feature size decreases, coupled with increased densities. Double density, or 1.77 mm pitch, test beds seem to be adequate for 400 µm pitch and up. As the density of the substrate increases beyond 400 µm pitch, alternative techniques must be considered. Quad density fixturing is a possibility, with 62 test probes per square centimeter, but concern increases about potential feature damage due to the contact by the probes. In addition, the cost of double and quad density fixtures, as well as the cost of test equipment, make it difficult to justify total test coverage within cost expectations based on current understanding of electrical testing and a linear projection of present testing concepts.

Regarding the I/O density of 200 to 1000 at various grid segmentation, it becomes apparent that double and quad density is capable for bare board continuity testing the average I/O requirements. However, if components are stacked "edge-to-edge" the testing becomes impossible with this test approach. This is because a BGA on 1.0 mm pitch contains 96 lands per cm², and the quad density test fixture is only able to accommodate 62 probes per cm².

Spreading components on the mounting structure relieves some of that complexity but also consumes more space and reduces performance. It should also be noted that, using presently available testing concepts, maximum component I/O creates a condition that drives testing cost of the bare board dramatically higher due to multi-pass or dual fixture testing in order to have full test coverage. Figure 1-12 shows the relationship of part land requirements compared to fixture capability.

Flying probe testing eliminates the need for costly fixtures, and depending on the volume of substrates being manufactured can provide a cost-effective alternative to bed of nails testing. Unfortunately, the test is relatively slow, depending on the equipment used, and the equipment can be expensive. The problem is compounded by the increased density requirements and the need for additional net testing. Most of this equipment/test technique has evolved from the semiconductor industry and has experienced some difficulty in scaling to meet the mechanical challenges associated with larger panel sizes. In addition, the small feature size in some instances defeat the detection system due to the difficulties in charging the feature with the probe. Additional equipment development will have to take place if technologies such as this are going to be useful for the complex substrates of the future.

As via size continues to decrease, the limits of conventional evaluation with metallographic microsection will become less viable. 150 µm vias seem to be the practical limit for microsection labs of average competence. An alternative test method will be required if companies want to know more about the plating in the via than just continuity. An electrical Interconnect Stress Test is presently being used by some companies to determining hole integrity and reliability.
Reliability Considerations

When one talks about surface mount reliability, one is essentially talking about package and solder joint reliability. These two items affect SMT reliability in ways different from through-hole technology. The main reliability problem, component electrical failure, is package independent and needs to be minimized using the same methods as with Through-hole mounting of packaged components.

Solder joint reliability is an issue in surface mounting because solder joints must provide both the mechanical and electrical connections. In through-hole assemblies, solder joint reliability has not been as much of an issue because the plated through holes add mechanical strength to the joints. Does this mean that surface mount solder joints are less reliable?

The answer to that question involves two parts: joint reliability and package reliability. For commercial applications where plastic packages with "J"-lead, "I"-lead or gullwing lead forms are used and where ceramic components are limited to small resistors and capacitors, solder joint failure has not been a major factor. The leads of the large pin count packages are compliant and absorb stress, provided they are not over soldered (excess solder that fills the stress relief bends in the leads). The small ceramic chip resistors and capacitors do not usually experience enough differential expansion with changing temperature to cause significant stress. Nevertheless, if a printed board assembly is subjected to mechanical flexure (bow or twist) during its service life, the possibility of solder joint fatigue failures (cracking) will increase.

Solder joint reliability is more important in applications experiencing large changes in temperature and using large leadless ceramic chip carriers and large, very fine pitch, packages (0.5 mm spacing or less). Solder joint reliability is more important in applications experiencing large changes in temperature and using large leadless ceramic chip carriers and large, very fine pitch, packages (0.5 mm spacing or less). Users of ceramic leadless packages in severe environments usually limit ceramic package size to 1.5 mm (0.6 inch) i.e. 44 pin 1.27 mm pitch. Leadless ceramic packages with "J" or gull wing leads are typically used for high reliability in harsh environments above 44 pin and 104 pin (0.63 mm pitch). These uses require substrates with matched coefficients of expansion (CTE). One
solution is to use leaded packages with standard organic printed board materials whenever possible and to minimize the temperature swings during operation.

Leaded packages are not free of CTE problems, especially the very fine pitch packages with more than 100 leads on spacing of 0.5 mm or less. If the leads are over soldered, the packages may act as large ceramic non-compliant packages, prone to fatigue failure. If the leads are soldered while under stress, a solder joint failure may occur due to solder creep as the lead slowly moves back to an unstrained position.

The reliability of array type packages, such as the BGA, mini-BGAs and direct chip attachment in array formats depends on the amount of solder volume that exists in the ball or column. No problems have been experienced in relatively benign environments (laptop computers). However, testing is still being done to see what combinations of mounting structure, solder ball array and pitch will survive operation in under the hood applications. The combination of solder volumes, attachment platform (both chip and mounting structure), the use of under-fill materials, and the environment in which the equipment must operate will form part of the equations that access assembly reliability.

Component package reliability has also been a concern in commercial applications. This is primarily due to possible plastic package degradation when exposed to excessive soldering temperatures or high moisture environments.

**Component Considerations**

Surface mounting exposes the boards and the packages to higher soldering temperatures than typical through-hole mounting and the packages must be designed accordingly. Some through-hole mount components are being used as surface mount components by modifying the leads as gullwing or “I” beam leads, but these through-hole mount components may not withstand the higher temperatures of reflow soldering. To minimize this concern, some assemblers are using a lower melting temperature solder, approximately 130° C to 160° C on the secondary side, i.e., the last side to be mass soldered, and placing the modified and other sensitive components on this side. The primary side generally uses 63/67 Sn/Pb with a melting temperature of around 183° C.

While the plastic packages commonly used in commercial applications are generally safe from solder joint cracking, the packages themselves may crack, especially when the package is much larger than the die. Data indicates that moisture contributes to package cracking. A joint IPC/JEDEC report (J-STD-020) and test method have been released to describe the phenomenon and provide recommendations such as baking the components before soldering to prevent cracking. This document is being revised to reflect new test and handling procedures.

In addition to technical issues, cost is also important. The full benefits of surface mounting are difficult to achieve if many of the components in surface mount configurations are not available or not standardized. Today, many SMT boards are actually mixed assemblies made up of both surface mount and through-hole components.

If some components are not available in surface mount configurations, this increases both assembly cost and SMT component cost. In addition, variations in package types make automated assembly or interchanging component vendor parts on an existing land pattern difficult. Many surface mount components have been standardized, but not all. In time, more parts will be standardized, and as the industry develops greater production capability for a particular package or lead configuration these concepts will be the choice used by the component manufacturer for any new parts.

**Substrate Considerations**

Many types of substrates are available. These include the organic types, such as epoxy fiberglass as used in printed boards, ceramics used in hybrids, and special combinations used to enhance the physical or electrical properties of the interconnection substrate. Substrate selection depends upon the component packages and the end-use...
environment. Each substrate has advantages and disadvantages; the designer must analyze cost, reliability and performance needs.

There are essentially four ways to overcome the stress on the solder joint. First, develop substrates with a CTE that matches that of the component. Second, add leads to the surface mount packages to absorb the stress. Third, increase the solder volume and fillet size. Fourth add an "underfill" material that attaches the underside of the component to the mounting substrate, thus neutralizing the differences in CTE mismatch.

The substrate affects the electrical, thermal, and mechanical reliability of electronic assemblies. Today, interconnection substrates are evaluated and classified by their expansion characteristics for the X and Y axes of the substrate using change definition in parts per million per degree centigrade (PPM°C).

**Design for Manufacturability**

The rapid growth of technology increases the potential of conflict between design requirements and the manufacturability of a design. Almost by definition, as technology progresses, the manufacturer of a new design will have no experience upon which to predict the yield and reliability of the new product. Coupled with the decreasing life cycle of products today, there is a minimal amount of time for a manufacturer to develop the process capabilities needed for reliable production of products with new design requirements.

SMT design and PB manufacture/assembly is an excellent example of a process that needs a close relationship between the individual groups that make up the product manufacturing system. While SMT PBs are made with almost all of the same processes used in fabricating standard through-hole printed boards, most of the process tolerances and capabilities have had to change. For example, SMT designs have dramatically decreased the sizes of the via interconnect holes, conductor width and spacing have decreased, most SMT uses photoimageable soldermask, and solder coating operations have had to change capabilities to produce more uniform surface finishes. The variety of alternative finishes to that of reflowed tin/lead or Hot Air Solder Level (HASL) coatings has increased due to the requirement for flat land patterns. Almost all PB operations have had to change to improve the product capabilities needed for reliable assembly.

With the "globalization" and specialization of the electronics business, developing the communications and "team" interactions needed for manufacturability assessment and improvement has become more important than ever. Frequently, several different companies are involved in the design/production cycle. However, to ensure reliable production of new designs and technology, an integrated effort is required throughout the entire design/production operation, so that problems are communicated and fixed quickly.

**Assembly Considerations**

Surface mount assembly refers to the processes involved in producing a printed circuit assembly from the electrical components and printed wiring board. For mixed assembly technology these processes include:

1. Incoming material inspection
2. Kitting of material
3. Baking of PBs and plastic packaged components
4. Screen printing of solder paste onto the PB
5. Component placement (top side)
6. Inspection
7. Reflow
8. Assembly cleaning
9. Inspection
10. Adhesive dispensing
11. Component placement (bottom side)
12. Inspection
13. Curing of adhesive
14. Auto-insertion of through-hole components
15. Hand insertion of odd-shaped through-hole components
16. Wave solder
17. Cleaning
18. Inspection
19. Test

To assure the highest quality assembly process, the PBs should have fiducial marks so that fine pitch components can be properly placed. Fiducial marks not covered by solder or solder mask result in the maximum accuracy of reading by the vision system on the placement equipment. A pair of fiducials are required on the board. One or two local marks are required for fine pitch components. Tooling holes in the PB should match the placement equipment tooling pins, thus reducing the need for transfer plates.

If an adhesive is used to glue bottom side components to the PB, it must be applied with a controlled process producing a repeatable size of glue dots. A glue check area (55 mm x 6 mm) should be designed into the PB where sample dots can be placed and characterized. The amount of solder on the PB lands must not be so thick as to prevent contact of the component to the adhesive! No vias should be placed between component lands on the bottom side, in order to prevent solder from bleeding into the hole.

Oddly shaped PBs need to be designed to meet the standard sizes of the assembly placement equipment. In order to provide enough support on the outer edge of the PB, a frame area around the desired shape should be designed into the fabricated panel. Routing slots and breakaway tabs are required for depanelization to the final shape. The minimum routing width should be 2.3 mm.

Screened legends are used on the printed board to identify polarity of components, as well as component position. Some companies are questioning the need for this additional process step since alternate techniques for assembly and troubleshooting are available that do not rely on the legend markings. Cost pressures cause every element of the assembly to be evaluated.

Components for surface mounting must be properly packaged in tapes and reels for SOICs and passive components, in sticks for PLCCs molded carrier ring and TAB carriers and in matrix trays for quad flat packs (QFP), ball grid arrays (BGAs), mini BGAs, and even un-packed dice. For tape and reel, follow Electronic Industries Association Standards: EIA-481-1A, EIA-481-2, and EIA-481-3.

The assembly should be designed so components are not placed closer than 3 mm to the edge of the PB. No component should be placed any closer than 15 mm to a tooling hole in the fabrication panel; and component-to-component spacing needs to be large enough to allow for inspection and rework, if required.

For ease of rework SOJs should be spaced a minimum of 0.1 mm land-to-land or component-to-component, whichever is larger. To prevent open wave solder joints on backside surface mount chip components, the lands should be no closer than 1.75 mm. For backside SOICs to be wave soldered, the minimum spacing between component lands parallel to the direction of motion is 2.5 mm. In addition, for backside wave soldered SOICs, some systems require that an extra trailing land is added on both land rows. This land will pull excess solder away from the last active solder connection and thus reduce the incidence of solder bridging.

To minimize solder defects and to ease the task of inspection, all like components on both top and bottom sides of the PB should be oriented in the same direction. For wave soldered components the long axis of the lands should be aligned perpendicular to the direction of PB motion. This will help to prevent open solder joints. For IR reflow processes, the PB should be laid out in such a way as to achieve a high degree of uniformity in the heat absorption. This will minimize the maximum temperature seen by any portion of the board. For example, QFPs should not be
clustered but spaced evenly about the board. Again, for ease of rework, exposed vias should be a minimum of 0.25 mm from lands. If vias are closer than 0.25 mm, they should be covered by soldermask.

A key to high printed board assembly (PBA) yields and reliable solder joints is the solderability of the board and components. Assemblers must qualify and monitor the processes used by their suppliers to assure solderability of incoming material entering the assembly house. Joint industry standards ANSI/J-STD-002 (Component Solderability) and ANSI/J-STD-003 (PB Solderability) provide agreed to test procedures and requirements for solderability evaluation.

**Designing for the Assembly Process**

Manufacturability means designing products that fall within the manufacturing process capability. The benefits of a manufacturable design are better quality, quicker time to market, lower labor and material costs, shorter through-put time, fewer design revisions, and higher profits. Most companies planning surface mount products create manufacturable designs by trial and error, often at considerable expense. One quick way to waste thousands of dollars is to produce an SMT design that cannot be assembled, repaired, or tested. Design for manufacturability guidelines and rules (standards) can help the designer plan a manufacturable product; however, it is important to distinguish between standards and guidelines.

Standards are necessary for compatibility with the planned manufacturing equipment and processes. If standards are not followed, the product cannot be manufactured. Guidelines may make manufacturing easier but they are not critical in getting the product out the door.

For example, one general guideline is to leave sufficient space under the component, if cleaning is required, (approximately 0.13 mm). If the assembly process could result in less space being left under the part, the guideline should become a requirement to insure that assemblies can be properly cleaned and that no contamination or flux residue remains under the part. This requirement is not critical if no-clean or low residue solder fluxes are used, eliminating post-solder cleaning.

Since manufacturability is process dependent, guidelines and standards must be validated. Each process site should establish the process capability related to consistently manufacturing the same product in the same manner.

Finally, specifying guidelines and standards is not enough if people don't adhere to them. The company's management and work force must actively work to promote adherence. Table 1-8 provides a subjective process comparison of TH, SMT, and FPT. This table was originated to assist the committee developing the framework and standards for FPT and upgraded to include bare chip mounting technology (CMT).

**Table 1-8**

<table>
<thead>
<tr>
<th>Process Characteristics</th>
<th>Through-Hole Technology</th>
<th>Surface Mount Technology</th>
<th>Fine-Pitch Technology</th>
<th>Chip Mounting Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lands with Lead Mounting Holes</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Lands with External Vias</td>
<td>-</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Lands with Internal Vias</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Component Insertion</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Component Placement</td>
<td>-</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Component Lead Excise, Form &amp;</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Use of Solder Paste</td>
<td>-</td>
<td>5</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>
General Attachment and Process Flows

The principal surface mount attachment technologies used today are the adhesive/wave solder or the reflow soldering methods. The former attaches surface mount components (SMC) to the secondary side of the board using special adhesives. Ledged though-hole components are inserted on the primary side of the board. The whole assembly is then sent through a wave or drag solder machine to complete the connections. In this approach, the SMCs are actually immersed in the molten solder during the process.

The reflow method derives its origins from traditional hybrid circuit techniques which place SMCs into solder bearing paste on the primary side of the board. The first step is to dispense a solder paste onto the bare board using either a silk screen or stencil (for prototypes and small volume production, the paste may be applied one dot at a time, either automatically or manually). Components are placed into the tacky paste, which is then dried or preheated. No additional adhesive is necessary since the paste holds the components in place.

The solder is reflowed by one of several common methods, including infrared (IR), vapor phase or thermal convection using hot air. Many of today’s reflow ovens contain nitrogen blankets to reduce oxidation and improve soldering-ability. The boards then go through a cleaning operation to remove residual flux and any solder balls. Finally, if leaded through-hole components are needed, they are inserted and the board is sent through a wave solder operation. Normally, the primary side of the board does not get hot enough during the wave soldering to melt the previously reflowed solder holding the Surface Mount Components.

A new process currently being used is "Direct Attach of Fine Pitch Components." In this process, TAB, molded carrier ring, or similar type components with a lead pitch of 0.5mm (.020") or smaller are placed with the aid of automated vision systems. Because of the need for high accuracy alignment with respect to the printed board land pattern - no further handling is desired. Therefore, as the component is held in place during the placement cycle, the leads are reflow soldered or welded to their corresponding lands before the placement head retracts. The attachment processes in use include hot bar reflow, focused IR reflow, hot gas reflow, laser reflow, and thermocompression welding.

Common assembly process flow is shown in Figures 1-13. Solder paste is applied, components are placed, and then the assembly is reflow soldered and cleaned. Some users try to avoid cleaning after reflow; however, other users must clean immediately after reflow in order to meet final cleanliness specifications.

The newest process being developed is that for attachment of array packages to the substrates. BGA, PGA and LGA all require strict process control and an understanding of the variables that produce high quality, defect free solder connections. Techniques are being developed to provide adequate assurance that all joints are properly connected and that there are no shorts or solder bridges.
A simple Type 2C (THT/SMT simple) assembly has secondary side attachment in which surface mount passive devices and small active devices are wave-soldered to the secondary side of a mostly through hole component assembly. The leaded through-hole components may be automatically or manually inserted and clinched. Components are placed by a "pick-and-place" machine or robot: the adhesive is cured; the assembly is turned over; and the wave soldering process is used to solder both leaded through-hole and surface mount components in a single operation. Finally, the assembly is cleaned, inspected, repaired (if necessary), and tested.

To convert from a combination/complex THT/SMT assembly where the assembly contains only a few through-hole parts, users might consider modifying or cutting the component leads to make them surface mountable.

Probably the most complex assembly flow is the Type 2 THT/SMT/FPT/CMT Ultra Complex Assembly. This assembly uses wave soldering, mass reflow soldering, selective reflow soldering, and wire/lead bonding attachment techniques.

**Solid Solder Deposit Technology**

In recent years, developments have taken place intended to simplify the previously defined soldering attachment processes. This new technology, being developed in Europe, Asia, and the Americas, consists of having the printed board contain the correct amount of solder for mounting all the surface mount parts.

There are several advantages to solid soldering deposit (SSD) technology. These include:

- Preparing the printed board before it has been exposed to high temperature assembly processes.
- Eliminating the concern of printed board solderability.
- Simplifying the assembly line which can be made shorter.
- Reducing the registration problem at assembly for solder paste deposition.
- Permitting a single pass attachment process.

Although this technology has been in the experimentation stages for several years, with the advent of using more fine pitch components, the need at the assembly level for SSD has increased.

There are a variety of processes in the development stage. One process uses a special machine, to add the molten solder to the lands; another process uses solder paste which has been reflowed, and coined to achieve the flat surface necessary for placing the surface mount parts. Selective tin/lead plating followed by reflow, has also been used successfully; this process is also followed by a flattening of the land area.

Most of these processes are still in the prototype stage. Because of the preliminary successes and the investments being made by major original equipment manufacturers it is likely that the assembly process will achieve successes in those companies that have not as yet made a major commitment to solder paste application equipment. If the assembly has components on both sides, adhesives are used to hold components in place on the under-side during the single pass soldering operation.

**Assembly Equipment Considerations**

Most of the electronic assembly types employ component mounting, soldering, and cleaning process steps. If no-clean fluxes are used in the soldering process some of the cleaning steps may be eliminated, however, flux residues are not the only contaminant; finger prints, air borne particles, hand creams and other items need to be controlled or adequately removed.

The equipment required for each process step is shown in Figure 1-14. Twelve basic equipment types are needed to process the variety of printed board assemblies being designed today. Figure 1-14 also shows the combinations of equipment that might be used to produce the electronic assembly categories shown in Figure 1-4.
### Part Mounting Equipment

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Paste Application</td>
<td>Adhesive Application</td>
<td>Thru-hole Component Insertion</td>
<td>Surface Mount Component Placement</td>
<td>Adhesive and/or Paste Curing</td>
</tr>
</tbody>
</table>

### Soldering and Cleaning Equipment

<table>
<thead>
<tr>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reflow</td>
<td>Wave Soldering</td>
<td>Aqueous Cleaning*</td>
<td>Solvent Cleaning*</td>
<td>Cleanliness Testing*</td>
</tr>
</tbody>
</table>

### Application of Equipment to Assembly Types

#### Type 1

- **A** - $3 + 7 + 8 + 10$
- **B** - $1 + 4 + 5 + 6 + 8$ or $9 + 10$
- **C** - $1 + 4 + 5 + 6 + 8$ or $9 + 3 + 7 + 8 + 10$

#### Type 2

- **A** - Not Recommended
- **B** - $1 + 4 + 5 + 6 + 8$ or $9 + 1 + 4 + 5 + 6 + 8$ or $9 + 10$
- **C** - (Simple) $2 + 4 + 5 + 3 + 7 + 8 + 10$
- (Complex) $1 + 4 + 5 + 6 + 8$ or $9 + 2 + 4 + 5 + 3 + 7 + 8 + 9$

* Optional depending on final cleanliness specifications and solder flux used.

---

**Figure 1-14**

Major Equipment Required to Produce All Types of Printed Board Electronic Assemblies
SECTION 2
Status Report on the Visions 2010 Roadmap Analysis

In 1998 a cross-industry roadmap analysis, sponsored by the Surface Mount Council was held to explore the predictions of the specific industry segments' roadmap and identify similarities and differences between those roadmaps. The intent was to set the focus for a comprehensive discussion of approaches to problems associated with the interfaces between segments and identify common challenges within the electronics industry as a whole.

A complete overview of this project, called Visions 2010 Roadmap Analysis, was presented last year in the Surface Mount Council's 1998 Status and Action Plan. A review of the analysis was also presented at the 1999 Surface Mount Technology Association Conference in San Jose, CA.

A full review of the 2010 project will not be repeated here. Rather, this section will briefly summarize the 2010 project and then present a status report on what actions the Surface Mount Council is undertaking in support of the 2010 effort. (The complete 2010 report can be found on the Surface Mount Council's web site at www.surfacemountcouncil.org)

2.1 SUMMARY OF THE 2010 PROJECT

Vision 2010 is based on the existing electronics industry roadmaps. A brief description of the roadmaps considered in the 2010 analysis is provided here for reference. (The current chair of the roadmap activity is listed)

- The 1997 National Technology Roadmap for Semiconductors. It is published by the SIA (Semiconductors Industries Association), but receives considerable support from Sematech, and SRC. This roadmap is a 15-year projection of CMOS integrated circuit technology. It identifies research needs and provides some potential solutions. The chairman of this roadmap is Paolo Gargini from Intel.

- The 1996 National Electronics Manufacturing Roadmap. This roadmap takes a system view, utilizing five product emulators as its basis. The chairman of the NEMI National Electronic Manufacturing Initiative roadmap is Irwin Asher of Lucent Technologies. Leo Feinstein of NEMI is the co-chair.

- The 1997 National Technology for Electronic Interconnections. The IPC roadmap is based on 18 product emulators and covers the areas of printed wiring board assembly, device packaging, board assembly, and environmental issues. The chairman is Jack Fisher, from ITRI.

- The 1996 Electronic Design Automation Roadmap. This roadmap is a cooperation between EDAC (Electronic Design Automation Companies), CFI and Sematech. John Teets from Silicon Integrated Initiatives, is chairman.

- The 1996 Optoelectronics Technology Roadmap Series Conclusions & Recommendations Sensors, Multimedia, Parallel Optical Interconnects, and Military and Aerospace. Since 1992, OIDA has conducted both market and technology-oriented workshops, which serve to identify critical issues for suppliers and users, develop statistical estimates, and provide recommendations to industry and government. In addition to assistance from the Defense Advanced Research Projects Agency (DARPA), OIDA's workshops are supported by the active participation of the National Institute of Standards and Technology (NIST) and the National Science Foundation (NSF) which provide valuable expertise and insight to the process.

The roadmaps developed by various segments of the electronics industry are subject to internal review within each segment. Industry experts within a particular technology area chart each roadmap. The maps represent the best
The judgment of experts in that field. However, the needs identified by one industry segment are not generally known to other segments nor do these the individual segment needs have the same priority in another segment's roadmap.

The idea for Technology Vision Analysis 2010 was first proposed at the Surface Mount Council meeting in September 1997. Given the broad experience base of the Council members it had become apparent that roadmapping was a major industry trend. It was also apparent to the Council, given that many of its members actively participate in these industry wide roadmap activities, that these individual roadmaps were very "segment focused". Even with the efforts of a national committee to coordinate roadmap timetables, the focus of the segments was often significantly different.

The Council discussed the variety of scope and focus of the published electronics industry roadmap and voted to invite all affiliate members of the Council (and any interested industry representatives) to a cross roadmap analysis. This team of industry members, including many of the representatives from the leading industry roadmap groups, met at Georgia Institute of Technology in February of 1998. The team addressed issues of management, design, components, assembly, and substrate interconnections. Each team covering these issues reviewed the scope of the existing roadmaps, their similarities, gaps and issues that cut across the industry.

Based on the work of the team a series of actions items were identified and prioritized. Of the action items prioritized some were referred to the national roadmap committees and the Surface Mount Council took some. The list of Council action items as identified by the 2010 team was:

Roadmap Coordination: the National Roadmap Coordinating Committee is already working the issue of coordination between the publication of the various roadmaps. The Surface Mount Council will work to provide on going input to that committee based on a yearly cross roadmap analysis.

Emulators: The concept of product emulator is common for IPC, NEMI, and SIA. IPC uses 20 product emulators. NEMI uses 5 product emulators. SIA uses product emulators. The Surface Mount Council will work to encourage adoption of a core group of product emulators. These emulators will serve as a direct cross roadmap comparison and allow a user of any roadmap to immediately and easily compare the predictions in technology evolution from one roadmap to another.

Commonality of Terms and Definitions: Each roadmap uses a different set of terms and definitions. In some cases even when words are used in common, the meaning of those words is not the same from one roadmap to another. The Surface Mount Council will work to facilitate the adoption of a common glossary of terms and definitions for all roadmaps.

Date of First Use/Revenue Center of Gravity: Beyond the differences in definitions of terms used in the roadmaps is the issue of economic impact of a particular technology. Each roadmap has a different approach to its description of when a technology is first introduced, when it becomes generally available and when that technology is in common use. The Surface Mount Council will work to encourage the adoption of a common metric to describe technology introduction based on that technologies economic impact.

Scaling with Silicon: The semiconductor industry has had great success in tracking its technology evolution using Moore’s Law. Although various “laws” have been proposed for translating silicon feature density into wiring density on PWBs, there has been no general acceptance of a PWB equivalent to Moore’s Law. The Surface Mount Council will work to support development of a common metric that can use the data of the semiconductor industry in an algorithm that provides a meaningful description of wiring and interconnection density for the PWB and board assembly industries.

Development of a Technology Tracking Matrix: The Surface Mount Council publishes an annual status report on the electronics industry called the “Status and Action Plan”.

1999 Status and Action Plan

Section 2

Page 2
2.2 SURFACE MOUNT COUNCIL ACTIVITIES BASED ON 2010

The Surface Mount Council has undertaken the following actions in response to the items listed above.

Roadmap Coordination: the National Roadmap Coordinating Committee has two members of the Surface Mount Council as participating members. These members provide on-going reports on the activities of the National Roadmap Committee and in turn bring Council feedback to the Committee.

Commonality of Terms and Definitions/Date of First Use/Revenue Center of Gravity: The Surface Mount Council has requested the National Roadmap Coordinating Committee accept IEC6154 as their official list of terms and definitions. The Council has also requested that for items not covered in IEC6154, e.g. "revenue center of gravity", the IPC roadmaps list of terms be adopted by all National Roadmap teams.

Emulators/Development of a Technology Tracking Matrix: Better coordination between the emulators of the roadmaps is occurring now through the efforts of the National Roadmap Coordinating Committee. The Surface Mount Council has taken as an action item a review of past emulator predictions. This review would benchmark where the industry has gone relative to roadmap predictions. The Council is approaching this issue in two ways. First, a review sources of information on industry trends such as the TMRC is being conducted to determine how technology actually changed over the years of the roadmap predictions. Secondly, with data available, a review of relative costs of the emulators is being tested using the MACH-SPAN model in the IPC roadmap.

Scaling with Silicon: This item remains open at this time. At present the challenge from the SIA roadmap to "scale with silicon" in the printed wiring board world remains unanswered. The Council will continue to look for ways to respond to this challenge.

2.3 SUMMARY

The Technology Vision Analysis 2010 is an attempt to analyze the industry roadmap efforts now underway in the United States and to use that analysis to develop ways to make those efforts more successful. Vision 2010 represents the first effort of this type within the road-mapping activities of the United States Electronics industry. The Surface Mount Council is committed to insuring that this work is not a “one time” activity. The Council has committed itself to furthering the development of electronics industry roadmaps. Updates on Council activities in support of this goal will be released on a regular basis.
SECTION 3
Design for Manufacturability

Design for manufacturability is the practice of designing board products that can be produced in a cost-effective manner using existing manufacturing processes and equipment. The benefits of a manufacturable design are better quality, quicker time to market, lower labor and material costs, shorter throughput time and fewer design iterations. The quickest way to waste thousands of dollars is to produce an SMT design that cannot be assembled, repaired or tested using the existing equipment. Design for manufacturability is essentially a yield issue, hence a cost issue. It plays a critical role in reducing defects in printed circuit assemblies.

Design for manufacturability (DFM) is gaining more recognition, as it becomes clear that manufacturing engineers alone cannot control cost reduction of printed circuit assemblies. The printed circuit board designer also plays a critical role in cost reduction. The days of throwing the design over the fence to the manufacturing engineer are gone—if indeed they ever really existed.

Every company needs its own unique DFM. Certain guidelines are equipment and process dependent and do not apply equally to all manufacturing facilities. The issues dealing with component selection, an integral part of DFM is also unique to each company. There are some guidelines that are generic, and hence will apply to every company. IPC-SM-782 is a good place to start for incorporating generic guidelines. It should be noted however, that IPC-SM-782 is primarily a land pattern document - a subset of DFM.

It is very common to hear from SMT assembly subcontractors that since the design is done by OEMs, they really do not have much control over the design. While this is mostly true, it does not have to be so. For example, generally the quotes for products that meet DFM requirements should be higher than those products that do not. This certainly should get attention of OEMs. Also, how about providing free training to OEMs on DFM. Unfortunately, not every subcontractor has in-house DFM and hence is really not prepared to provide any DFM help to OEMs.

3.1 DFM Organizational Structure

The traditional approach of doing design serially, where the design proceeds from the logic or circuit designer to physical designer (CAD layout) to manufacturing and finally to the test engineer for review, is not appropriate because each engineer is making decisions independently in evaluating and selecting alternatives. This results in sub-optimized designs. What is worse is where the manufacturing engineer sees the design only in a physical form on a PCB. This is generally the case when subcontract assembly houses build products.

A parallel or concurrent design approach where the logic designer, CAD layout designer, the manufacturing, test, and process engineers and purchasing and marketing representatives sit in one room to review the design and discuss the alternatives to meet thermal, electrical, real estate, cost and time to market requirements is highly recommended. This should be done in the early phases of the design to evaluate various alternatives within the boundaries of the company’s in-house DFM document created by them.

The DFM team should consist of members from various organizations such as logic design, CAD layout, Manufacturing, Test and Component Engineering and Purchasing and Marketing. A Program Manager with good technical and people skills who has the full support of the team members and their managers should head this team. It is critical that the team has good understanding of the SMT design and process issues in order to establish meaningful DFM that can improve yield and reduce cost. Putting the designers onto the shop floor to assist manufacturing engineering in developing and implementing the manufacturing process should also be seriously considered. This will prevent the designer from “throwing the design over the fence” to manufacturing.

If the team does not create a DFM document, enforcement will be a problem due to lack of ownership and misunderstanding of the issues. Many times DFM violations happen because parties involved are not aware of
the consequences of their decisions. This is why reasons should be provided for DFM rule. With passage of
time, if the reasons change, the team can change the rules accordingly.

The design team plays a critical role in the success and financial viability of any product using SMT. This has
been true in the through-hole mount design as well, but not to the same degree. There is only one way to
assemble a through-hole mount board: stuff and wave solder it. In SMT, however, the designer has many
options, depending on the type of assembly. For example, in SMT, the same component can be placed on either
the topside or the bottom side, with different manufacturing consequences in each case. Clearly the design
team needs to be thoroughly familiar with the surface mount manufacturing processes in order to understand
the impact of their decision.

This is not to belittle the importance of DFM in through-hole assemblies, because DFM for autoinsertion is
important. But unlike through-hole mount, SMT does not have the option of manual placement, and the rules
for testability are very different because in SMT we no longer have the ends of the devices that also served as
the test nodes. In a nutshell, DFM and the role of the design team in the success of SMT cannot be
overemphasized.

3.2 Design Rules Versus Guidelines

For the design team to be able to design a manufacturable product, it is important to establish guidelines and
rules. The distinction between guidelines and rules is very important. Rules are necessary for compatibility with
the planned manufacturing equipment and processes. If the design rules are not followed, the product either
cannot be manufactured or must be built manually. In the case of SMT, having to build manually is tantamount
to not being able to build at all. Guidelines, on the other hand, are nice to have and may make life easier for the
manufacturing engineer, but they are not critical in getting the product out the door. This means that rules
cannot be violated, but guidelines may be overruled if there are good and sufficient reasons.

Depending on the product and on marketing constraints, even the rules can be violated as long as the members
of the product team understand and agree on the consequences of each violation. In general, the guidelines can
be violated by the DFM team but violating the rules requires, in addition to the team’s approval, the signature of
a higher level manager who has been designated by the company as its DFM authority.

In order to lend some weight to DFM guidelines and rules, it is important that such a policy be in place. In
addition, there should also be a procedure in the DFM requiring the team to provide reasons for each violation,
alternatives attempted and the impact of the violation on product cost and schedule. Also, violating either the
guidelines or rules once must not set precedence for subsequent violation on other products. Such a policy will
generally not be viewed as a bureaucratic hurdle since it is created by the team members who have to live by it.
This implies that they are diligent in creating the DFM document in the first place and since it is their policy,
they can abide by it. This is another reason for creating in-house DFM guidelines and rules guidelines and
updating it on a regular basis.

It is not enough, however, to establish design rules and guidelines for manufacturability. Everyone must be
fully trained on the content of the DFM. And most importantly, a corporate culture must exist to support
adherence to DFM, as is the case with other important company policies and procedures.

3.3 Surface Mount Component Land Patterns

Surface mount land patterns, commonly referred to as footprints or pads, define the sites at which components
are to be soldered to a printed circuit board. The design of land patterns is critical because it not only
determines solder joint strength, hence reliability, but it also influences the areas of solder defects, cleanability,
testability, and repair/rework. In other words, the very producibility of surface mount assemblies depends on
land pattern design. However, the producibility of surface mount assembly is not determined by pad design
alone. Materials, processes, components, and board solderability also play very important roles.
Poor component tolerances and the lack of standardization of surface mount packages have compounded the problem of standardizing the land pattern design. Numerous package types are being offered by the industry, and the variations in a given package type can be numerous, as well. More important, the tolerance on components varies significantly, causing real problems for land pattern design and adding to the manufacturing problems for SMT users.

Consider the component tolerance found in “standard” 1206 resistors and capacitors. These items are anything but standard: the tolerance of the most important dimensions—the termination width—varies from a minimum of 10 mils to a maximum of 30 mils (nominal dimension is 20 mil). With a tolerance variation of this magnitude, the design of land patterns is challenging indeed.

The technical societies, such as the Institute of Interconnecting and Packaging Electronic Circuits, the Electronics Industries Association, and the Surface Mount Council, are doing everything they can to improve the current situation as far as component standardization and tolerances are concerned.

Through the efforts of the Surface Mount Council, now there is a significant amount of coordination between the EIA and the IPC to ensure compatibility between component outlines (established by the EIA) and their land patterns (established by the IPC). For example, IPC-SM-782 document is a good example of the industry's effort to promote standardization in surface mount technology. IPC-SM-782 also discusses the basic concepts of land pattern design for different package types, including the formulas that serve as the basis for the land patterns. The formulas can be used for developing land patterns for newer components as they become available or when the dimensions of the existing components change.

Many people consider IPC-SM-782 also as a DFM document as well. While it sheds some light on DFM related issues; it should be kept in mind that it is primarily a land pattern document and not a DFM document. The land patterns are a subset of DFM, which should also encompass issues in components, bare board, solder mask, placement, soldering, rework and test. Every company should have in-house company specific DFM document to take advantage of its unique processes, component, solder mask, board and assembly requirements.

One will benefit greatly if the land pattern designs are also customized for the manufacturing process being used. For example, there are companies who solder bottom side components twice (both by reflow and wave solder). In this process, paste is printed, adhesive is dispensed, and components are placed and then reflowed. All these devices should have been soldered either by reflow or wave but at times they are not. Hence the company resorted to two step soldering where single step should have sufficed. Most likely the cause of the problem here is poor component or board solderability. Such problems should be corrected at the source by asking the supplier to provide solderable parts and not be taking unnecessary added step, which adds to product cost.

### 3.4 Different Land Pattern for Wave and Reflow?

Given the process and thermal profile differences among soldering methods, should the land pattern designs for each be different? From the standpoint of optimizing the land pattern design, it is advantageous to have different land patterns for different soldering processes. But from a systems standpoint, having different land patterns for different processes poses some problems. For example, some CAD systems limit the total number of land pattern sizes that can be supported.

Even if the CAD capability is not a concern, it would be very confusing for a CAD designer to have to maintain different sets of land patterns for different soldering processes for the same part in the CAD library. In many cases this approach could be very restrictive if the company uses different soldering processes for various applications because no one process meets all requirements.

The primary reason for having different land patterns for reflow and wave soldering is the susceptibility of components to moving or standing up during soldering. During wave soldering, since the components are
glued, part movement is not a concern. Thus a land pattern design that is optimum for reflow soldering will work also for wave soldering. Obviously, then, it is desirable for the land pattern design for components to be transparent to both wave and reflow processes. It should be kept in mind that this issue of common land patterns is applicable only to discrete devices, such as resistors, capacitors, small outline transistors (SOTs), and sometimes small outline integrated circuits (SOICs). Active devices such as plastic leaded chip carriers (PLCCs) and fine pitch are not wave soldered, so for them this issue does not arise.

Whether using the same or different land pattern designs for different soldering processes, the land patterns must be validated for reliability and manufacturability before being used on products.

### 3.5 Conclusions and Recommendations

The benefits of a manufacturable design are better quality, quicker time to market, lower labor and material costs, shorter throughput time and fewer design iterations. Every company needs its own unique DFM that is developed by a team. The design team plays a critical role in the success and financial viability of any product using SMT. For the design team to be able to design a manufacturable product, it is important to establish guidelines and rules and controlled procedures for DFM revisions. In order to lend some weight to DFM guidelines and rules, it is important that such a policy be in place.

IPC-SM-782 is a good place to start for incorporating generic guidelines. It should be noted however, that IPC-SM-782 is primarily a land pattern document - a subset of DFM. It is not enough, however, to establish design rules and guidelines for manufacturability. Everyone must be fully trained on the content of the DFM. And most importantly, a corporate culture must exist to support adherence to DFM, as is the case with other important company policies and procedures.

While DFM is very important, we must also keep in mind that design for manufacturability alone cannot eliminate all defects in surface mount assemblies. Defects fall into three major categories: design-related problems, incoming material related problems such as PCB, adhesive, solder paste etc. and problems related to manufacturing processes and equipment. Each defect should be analyzed for its source, to permit appropriate corrective action to be taken. Simply put, all major issues in design, materials, and process must be fine-tuned to achieve zero defects. What this means is that in addition to DFM, every company also needs internal “recipe” for materials and processes as well.
SECTION 4
SMT COMPONENTS

4.1 Component Packaging Issues

The continued emphasis on faster, smaller, lighter, and lower cost electronics systems is making component, board and system packaging more complex each year. The increase in complexity is due to wider use of finer pitch, thinner array surface mount packages, which are the key to miniaturization of electronics products in the new Millennium. Most of the components on a typical systems motherboard for desk top computer systems remain at 1.27 and 1.00 mm pitch surface mount components with increasing use of finer pitch (0.80, 0.65, 0.50 & 0.40 mm) array styled packages. Portable systems are moving to the finer pitches at a faster rate.

The component pitch and overall profile height plays a critical role in the complexity of manufacturing process. The use of finer pitch low profile components demands assembly equipment and processes operate tighter specification limits. The assembly processes that demand a higher precision are as follows: pick-and-place, solder paste-printing applications, reflow, inspection, and rework. The use of finer pitch low profile components increases the complexity, which could negatively effect yield and rework making assemblies more difficult and costly. Let us examine the driving forces for component packaging and some major issues in high pin count fine pitch component packages.

The Drivers for Component Packaging

Since memory and microprocessor packaging generally drives the component packaging technology, let’s look into the forces that drive this technology. The driving forces for component packaging are thermal performance, electrical performance and overall profile / foot print of the package (length, width, and thickness). These forces must be accomplished at the lowest possible cost to meet the high volume commodity markets. The component packaging requirement varies for different types of systems. For example, the high-end microprocessors run at high frequencies require thermally and electrically-enhanced package designs. Examples of thermal enhancements are heat slugs, heat spreaders, heat sinks and fin-fan (fan mounted on heat sink) etc. Examples of electrical enhancements are multilayer and higher pin-count packages and in-package capacitance. In the past hermetic ceramic packages were generally used for the in-package capacitance application put now plastic package solutions are appearing. With the fine line disappearing between mid-range and commercial/industrial systems, performance and cost are running hand in hand. Thermally enhanced multilayer packages (Plastic PGA, QFP, BGA & FBGA) may be appropriate for this application. For low-end entry level and portable systems cost and overall profile factors are critical and surface mount packages such as LQFP, TQFP, TSOP, TSSOP, TAB are generally used for this application. The CSPs (Chip Size Packages) and Flip Chips are making their presence known in these areas and the volumes are increasing rapidly. As the overall price of finished electronic devices decrease, the pressure to use packages widely used in the commodity market increases in area that were not as cost sensitive in the past.

The Thermal Drivers

Thermal enhancements have become essential with introduction of faster and faster microprocessors. With introduction of new generations of microprocessors, power dissipation has continually moved upward. This trend does not show any sign in change of direction in the future. As the device clocking speed increases and the silicon geometries decreases, the power issues become more challenging. Packaging is becoming the critical issue in these new microprocessors. The ceramic PGA (CPGA) has been commonly used for higher wattage packages but is being replace by non hermetic versions because of cost. An example would be the Intel 400, 500 and 600 MHz microprocessors (Pentium III™). Use of thermally enhanced plastic packages used to be limited to 6 - 8 watts maximum. Now thermally enhanced plastic packages can accommodate up to 30-50 watts.
The Electrical Drivers

Electrical performance drivers include signal fidelity, operating frequency, power, and pin-count. With increasing frequency, the need for improved board impedance control and minimal package insertion loss are concerned. With impedance control comes the need for terminations to prevent or damp reflections. These terminations, if performed in parallel to source and/or load points on critical signals, will increase power consumption.

High frequency operation itself, all other things being equal, drives power consumption upward as the square of frequency. As such, low power semiconductor research is increasing, in an attempt to reduce the average power consumption of complex digital ICs. The desire for longer operation of consumer products further accelerates the drive to reduce power consumption. Fortunately, as IC processes mature, the power per logic operation decreases by virtue of smaller device feature sizes. Shrinking transistors alone, however, are not the answer, since the power density of devices with smaller feature sizes is higher, due to the sheer number of devices packed in a given area on an integrated circuit.

In addition to power, IC pin counts are on the rise, as projected by Rent’s rule, which postulates that the number of signal pins required for a device increase as a function of the number of logic building blocks. Since the number of gates on typical devices have grown at a geometric rate for the last three decades, then it is not uncommon to see pin counts above 300 in contemporary integrated circuits. As devices increase in complexity, the number of pins required for power distribution also increase. In the case of ceramic packages, even with increase in bond pads for high speed devices, the pin count growth required for power and ground distribution is kept to a minimum by exploiting the intrinsically high package capacitance and employing package-mounted bypass capacitors. For example, the Intel Pentium III™ microprocessor has 370 pins in an organic (laminate) Pin Grid Array (PGA), while an Intel Pentium III™ for notebooks may require as many as 544 pins in an organic (laminate) Land Grid Array.

Packages are being built using both conventional wire bonding and flip chip for the interconnection to the organic substrates.

It is unlikely that Rent’s rule will soon be broken in high-end electronics system without some compromise. The most common form of compromise is occurs in digital designs when different signals use common pins. In doing this, pin count reduction is obtained at the expense of reduced performance, due to the need to time-share a common set of pins for multiple functions. The practice is inconsistent with the nearly continuous demand for improved performance, which places pressure on complex systems designers to increase pin count to maximize electrical bandwidth. As such, leading edge components, such as the Compaq’s Alpha can have in excess of 400 pins, while IBM and NEC mainframe MCMs have in excess of 1600 pins. Since yesterday’s mainframes are becoming tomorrow’s laptops, the trend of increasing pin count is important to consider, as it drives package and assembly technologies.

In addition to an increase in pin count, the need for shorter leads is also becoming evident. Higher pin counts are commonly used in faster systems, which need lower pin inductance, capacitance and resistance. This is one of the reasons for intense interest in packages such as BGAs and LGAs, which not only accommodate larger pin counts but also provide lower package parasitics.

The Real Estate Drivers

The real estate constraint is also one of the important driving forces in component packaging. This has contributed to the widespread usage of surface mount devices, which are not only smaller in size, but enable component mounting on both sides of the board. As pin counts increase, however, even with surface mount, the conductor-to-conductor pitch must decrease to keep the size of the package within a practical range for manufacturing. For example, when the pin count increases beyond 84 pins, decreasing pitch from 1.27 or 1.00 mm to 0.80 or 0.50 mm allows higher pin-count packages without a corresponding package size increase. However, even this measure is not enough for pin-counts beyond 200, and finer pitches, such as 0.4/0.3 mm in a TAB or FQFP format, become
necessary for peripherally leaded devices. Another obvious solution to the package size problem is to move to area distributed conductor package approaches, such as pin grid arrays (PGAs), ball grid arrays (BGAs), land grid arrays (LGAs), and chip size packages (CSPs).

There is another unwritten rule about real estate constraint for surface mount packages. The package size needs to be around 40 mm (1.50 inch) maximum per side. The Fine Pitch BGAs (FBGAs) and other Chip Size Packages (CSPs) are topping out at 21 mm (0.83 inch). The main factors for this is as follows:

1. Most pick and place machines have field of view limited to about 40 mm maximum, although there is a limited number of models that can handle larger packages.
2. As the peripheral leaded package increase in pin count above 200, the corresponding packages sizes are approaching the 40 mm per side maximum which creates a plastic package overmolding warpage problem that translates to a harder time in maintaining the tight 1.0 mm (4 mils) maximum coplanarity allowed. Plastic packages above 40 x 40 mm are not practical if the coplanarity is 1.0 mm.
3. As the package body size increase larger on peripherally finer (0.50 & 0.40 mm) pitch packages, the lead skew (bend) as well as coplanarity become equally critical issues. This is why the popularity of 0.40 mm pitch packages has not risen in the last few years. Pitches below 0.40 mm have been abandoned except in unique custom applications.
4. If the package is thermally enhanced, the coplanarity and standoff problems gets more sensitive because of the weight of the heat slug or heat spreader.
5. If the package happens to be a laminate based structure, such as BGA, the flatness of the laminate becomes a critical factor in meeting the tight coplanarity. The larger the package the greater the laminate warpage. This is major reason why the coplanarity requirement is 0.20 mm (8 mil) for BGA packages. The majority of suppliers would like the BGA coplanarity to be greater 0.20 mm (8 mils) while users would prefer 0.10 mm (4 mils). The BGA laminate issue continues so the final coplanarity is 0.15 mm (6 mils) because the balls used are high temperature melt ball and do not collapse like the eutectic ball on the plastic styles.

As discussed earlier, there are generic package drivers such as cost, thermal/electrical enhancements and real estate constraints. Now let us examine some of the driving factors for some specific packages.

**PGA Drivers**

With the infrastructure for surface mount in place, why do we still need a PGA? There are two main reasons: disadvantages of surface mount and advantages of PGA. Let us look at the disadvantage of surface mount packages. Surface mount ceramic packages such as Ceramic Leadless Chip Carrier (CLCC) or Ceramic Land Grid Array (CLGA) direct soldering to a PC Board may experience solder joint cracking due to the mismatch of the package and board materials. The same two package types could be socketed but may have reliability problems due to mechanical nature of connection. In addition, by requiring a selective gold plating process for the board, CLCCs and CLGAs will drive up the standard board cost.

Now let us look at some of the advantages of a PGA. It can either be socketed or directly soldered without some of the reliability concerns that afflict surface mount packages. Many OEM’s directly solder PGAs to board assemblies in order to reduce cost, except during development where socketed components are more desirable. PGAs are socketed in computer applications to allow easy customizing and upgrading motherboards.

In through-hole, the PGA is most widely used for microprocessor packaging. The main disadvantage of the PGA is its larger size. However, for larger wattage devices, board or system space requirement is determined by the heat sink size. In addition, a ceramic PGA easily incorporates electrical (in-package capacitance) and thermal enhancements required by high performance devices. In-package capacitance is difficult to incorporate in a surface mount package. The industry in order to reduce cost is using Laminates (organic) rather than Ceramic PGAs in most applications. This has created a shift from ceramic to laminates as the main stream packages.
Unlike ultra-fine pitch and BGA packages, PGA has been used for over 20 years. Also, PGA can be reliably socketed (and soldered). For various reasons, OEMs and users prefer socketing. There is a strong need for socketing the most expensive component in a typical system. For example, socketing allows OEMs to design a common motherboard that will accept all different frequencies of a given microprocessor with common pin out. Socketing allows upgrades by end users that do not have to buy a whole new system in order to take advantage of higher performance of future processors.

All this adds up to a strong case for continued use of PGAs along with predominately surface mount packages on the same board. The continued use of PGAs, through-hole sockets and connectors means that the industry will have to wrestle with mix-and-match assemblies for the foreseeable future.

**Fine Pitch Plastic Drivers**

The primary driver for fine pitch is real estate reduction. In addition, there is significant cost saving, in some cases over the PGA. Fine pitch plastic package is a common package for high pin count (over 100) ASIC (application specific integrated circuit) devices. In many cases, ASICs are used for reducing thermal load by combining 10 to 20 programmable logic array devices that would consume 5 to 10 watts into a 2 to 4 watts single ASIC device. These packages allow thermal and electrical enhancements by use of heat slugs and multilayer boards while significantly reducing cost. Package reliability and moisture susceptibility used to some of the major concerns preventing their widespread use. However, these issues have been resolved by the industry now. For example, J-STD-020 provides guidelines for classification and handling of moisture sensitive packages.

**Ball Grid Array (BGA) Drivers**

High pin count peripherally leaded devices (200-300 lead) with 0.50-mm (20-mil) pitch have become commonplace in the industry. However, this package cannot accommodate 300 pins or higher without issues with lead skew, package flatness, coplanarity and physical size. The larger pin devices greater than 300 requires finer peripherally lead pitches of 0.50 (20 mil), 0.40 (16 mil) or 0.30 (12 mil) mm. Although pitches below 0.50 mm on paper are wonderful for reducing package size, these pitches present many problems for most SMT manufacturers.

At these fine-pitches, leads are very fragile and susceptible to damage such as lead coplanarity, lead bending, and lead skew (bend). The problems with fine-pitch packages do not end here. The finer particle solder pastes needed for these fine-pitch packages tend to increase viscosity and lower print speed. Also, design guidelines must change to allow added inter-package spacing between the fine-pitch devices and neighboring conventional packages when using dual thickness printing for solder paste.
With the exception of no-clean fluxes, horrendous cleaning problems arise when using EIAJ (Japanese) fine-pitch peripherally leaded devices that sit almost flush (0 to 0.25 mm) to the board. For proper cleaning, a 0.35 to 0.50-mm standoffs is required for the larger high lead count packages.

Now compare the features of BGAs. Because BGAs use solder bump interconnections instead of leads, problems associated with lead damage and coplanarity are eliminated. The BGA are array type packages like the PGA so they are on longer peripherally leaded so they can distribute the balls in a higher pitch patterns on the on the package. The BGA pitches are 1.50 (60 mil), 1.27 (50mil), and 1.00 (40mil)and the minimum standoff is 0.50 mm, therefore the peripherally fine pitch problems with paste printing, placement and cleaning significantly reduced. BGAs also provide much shorter signal paths compared to fine-pitch devices and results in electrical enhancements for high speed applications.

BGAs have higher assembly yields than the fine-pitch peripherally leaded packages and the conversion is occurring at any accelerated rate. The cost difference between BGA packages and leaded packages has decreased making the BGAs more attractive. Finer the BGA pitches, more dramatic the impact on layer count and hence board cost.

BGAs are being back by the entire industry and becoming a widely accepted package option.

Even though the BGA has obtained industry and customer backing, the suppliers still are addressing some fundamental technical problems. These problems include warpage in large BGA packages, higher coplanarity 0.20(8-mil) mm, and thermal enhancements in plastic packages for higher wattage devices. Although BGAs can be packaged in ceramic for higher wattage devices, CTE mismatch problems associated with ceramic packages on commonly used glass epoxy circuit boards is a major solder joint reliability concern.

The future of BGA, however, looks very bright. One can expect this package to continue its used in the future but be thinner and have finer pitches that the present packages.

**Chip Size Packaging (CSP)**

A CSP is loosely defined as a package that takes no more than 20% additional area (Length & Width) than the bare silicon. What is the driving force for CSP? It provides higher packaging density than BGA but not quite the density that is possible with flip chip. However, the CSP assembly process is not as complex as the flip chip process either. For example, it does not pose the handling problems of the bare die used in flip chip. The assembly processes are not only much easier than those are for flip chips are; they are even compatible with SMT processes. CSPs can be pretested like SMT and reworked like SMT. Their pin count, size, and thermal and electrical performance are close to those of flip chip without the known good die concern of flip chip. Their disadvantages in comparison to flip chip is that they are slightly larger in size and their electrical performance may not as good. The CSP can have many different structures, processes, and materials while still meeting the customer’s requirements. CSPs are going to be a very flexible package technology. At last count there are more than 150 different styles of CSP. Some of the common names for CSPs are Fine Pitch Ball Grid Array (FBGA), Fine Pitch Land Grid Array (LGA), Small Outline No Lead (SON), and Quad Fine Pitch No Lead (QFN). We have include on example of a popular CSP for reference.

Tessera Micro BGA is one example of a CSP structure, process, and set of materials. It has the traces on a flex circuit fanning inward to the array of bumps underneath the die. This is the reverse of a TAB device, where the traces fan outward. The package is assembled using modified wire bonding equipment where gold wires are bonded to the chip's pads.
The package has an array of 85 to 90 micron electroplated nickel bumps plated with 0.3-micron gold flash on 25-micron thick polyamide film on a single- or two-layer tape. The second layer, when used, acts as the ground plane. A 150-micron thick high temperature silicone elastomer filled with 50% pure silica between die and polyamide film is used for X-Y-Z compliance.

Tessera Micro BGA has excellent electrical performance (0.5-0.7 NH) and a good thermal path through the backside of the die to a heat sink. The main issue with this package is that the paste printing and placement problems are somewhat like those for fine pitch packages since its pitch is very small. There are numerous other micro BGA packages by various US (e.g. micro SMT by Chip Scale) and Japanese companies.

**Issues In Component Packaging**

There are many types of packages but only four types of leads. Every lead configuration has advantages and disadvantages. Nevertheless, all lead configurations are generally found on most boards. The most common lead configurations used today are “J” and “Gull Wing”. The up and coming configuration consists of packages with balls (i.e., BGAs). The butt lead is merely an interim solution for a package that is not available in surface mount. Devices are normally available in one or more of the lead styles. Although each designer and manufacturer has its favorite lead configuration, for all practical purposes, these assemblers have to accommodate all lead types on most boards.

The gull wing lead is the most commonly used lead type today, especially for fine-pitch packages. As pin count increases, their use becomes increasingly more prevalent in peripherally leaded packages, as is evident in TAB and ultra-fine-pitch (0.50, 0.40, and 0.30 mm) packages. The low profiles of gull wing leaded packages are critical in applications such as notebook computers. These leads are compatible with almost any reflow soldering process, including IR, convection, vapor phase, hot gas and hot bar. Their ability to self-align during reflow when they are slightly misplaced is fairly good. Contrary to popular belief, lead inspection is more difficult with this configuration because of hidden heel fillets, which are very important for solder joint reliability. Their easily visible toe fillets are not required or even achievable all the time. Creating toe fillets on a consistent basis is difficult because the lead frame material (normally copper) is exposed when leads are cut after plating which makes it difficult to solder.

One of the biggest problems with gull wing leads is they are fragile and, consequently, susceptibility to lead damage such as coplanarity, lead bending and skew. Lead damage is the leading cause of defects in gull wing leaded packages. These packages generally have very low standoff height, causing flux entrapment, which results in cleaning difficulties. This problem is especially true with Japanese fine-pitch packages, which allow zero standoffs. The gull wing packages have lower profiles but have larger footprints than other surface mount options. Gull wing packages are cost effective at the board level because they require no additional layers to be added for routing.

Although gull wing devices are the most commonly used lead forms for high pin count packages, because of the aforementioned problems, there is much interest in ball grid array (BGA) packages. Instead of leads, this package uses robust balls, which are not susceptible to lead damage. With fragile leads replaced by rugged bumps, problems related to bent leads disappear. Also, BGA signal paths, much shorter than those of fine-pitch, prove advantageous in high-speed applications. Because balls accommodate high I/O in a small form factor, BGA may be the solution to the high pin count packaging trend.

Balls are very good at self-aligning during reflow. This benefit is partly responsible for higher yield. Undoubtedly helping improve yield is BGAs increased lead pitch to the familiar 1.00 to 1.50 mm pitch range from the problematic 0.50 mm pitch and below range common in gull wing packages. Also, since the package thickness maybe thinner than gull wing packages, BGAs have become popular in hand-held consumer applications like pagers.
Although a lead type may have many good points, no form is an SMT cure-all. For example, BGA requires less PCB real estate than gull wing components; however, balls increase board layer count requirements. Other BGA disadvantages include incompatibility with different reflow processes, cleaning problems, and hidden solder joints that cannot be inspected and are difficult to repair.

J lead packages have been the real workhorse of SMT. This package, an American invention, is more popular in the U.S. than Japan. They start at about 20 pins and are commonly used up to 84 pins. The J leaded packages come in Dual Inline and Quad formats. For pin counts higher than 84, different lead configurations such as gull wing or BGA must be used. J lead packages are more rigid than gull wing because of work hardening of leads during forming.

For pin counts above 84, J lead style is not used because of the difficulty in forming these leads. Like BGA, J lead devices are not compatible with all types of reflow processes (i.e., hot bar). And like BGA and gull wing, they also self-align well during reflow when slightly misplaced. However, one should never count on self-alignment as a substitute for accurate placement. J lead packages are excellent for cleaning because of higher standoff height. They take up less real estate on a board than other types of packages such as gull wing or butt leads. J lead inspection accessibility is excellent since the outer fillet is the major fillet for solder joint reliability.

Butt lead or I lead is not a commonly used configuration. However, it is sometimes used by cutting off the leads of through-hole devices such as DIPs to convert them to surface mount by brute force. This method is not always desirable but is an option especially when there are only a few through-hole packages in an almost completely surface mount board. Conversion to surface mount helps reduce the number of process steps during assembly.

These packages have high body thickness since they are essentially through-hole. They are not compatible with all soldering processes and creating good solder fillets with these leads is difficult. These leads are not used for very high pin count packages since DIPs are essentially low pin count packages. They generally do not self-align during reflow because of their higher mass. They are suitable for inspection, poor for real estate efficiency and excellent for cleaning because of their high standoff.

Where do we go from here? We have a mature infrastructure in place for dealing with PGA and QFP (0.5 mm pitch and above) packages. They do not address all our needs. So we have to explore high pin count CPGAs, enhanced plastics, BGAs, TAB and FQFPs.

As the performance and speed of microprocessor's increase, pin counts will increase. This trend will continue despite the fact that using multilayer packages with in-package capacitance for decoupling will electrically enhance these packages. For cost reduction, thermally and electrically enhanced packages will become common. For this to happen, however, the reliability concerns in such packages must be addressed first by the industry. The complexity of board assemblies will increase because packages of varying lead pitches including through hole will be used. To reduce board complexity and to increase manufacturing yield, ball grid array packages will become common since they reduce process complexity for the user. And, of course, the suppliers and users both will feel the complexity. Despite complexity in packaging and assembly, the primary driver will be cost. So the winners will be those suppliers who not only meet the technical challenge to provide a solution, but do so at a continuously decreasing price.

4.2 SMT Component Status

This section describes the current packaging status of the major surface mount product families. It includes a discussion of current standards and identifies areas for future development. It also displays the significant wealth of standards and documents that have been introduced in the past 12 months to define component package criteria.

Passive and Electromechanical Products
Passive Surface Mount products have become readily available as the market has continued to expand. High volume usage parts are being supplied by both domestic and foreign sources. Earlier SMT process incompatibilities have been overcome for the most part. Challenges for the future continue to involve size compression and value extension. Since these products are often the most numerous on the PB, they sometimes are the limiting factor in the end product size. This led to investigation of passive component arrays. This investigation is still in the early stages. Standardization of package types, terminations and pin outs, and costs are detriments to implementation at this time. Concerns for compatibility with circuit and layout needs must also be overcome.

Standards for passive parts have been published and are under continuous review to ensure they meet new needs as these needs develop. EIA has published a catalog of registered Surface Mount Passive Part Outlines as EIA PDP-100. This book provides detailed drawings of SM parts, which have been reviewed and approved by the EIA P-4 committee. This publication serves the same purpose for passive parts as JEDEC Publication 95 serves for Semiconductor Outlines.

EIA/IPC coordination will provide the recommended registered land patterns for all of the EIA published outlines. These land patterns are documented in IPC-SM-782.

Detailed component standards, which provide performance specifications and standardized test methods for all of the published outlines, are shown in Table 3-1.

### Table 4-1
Summary of Passive Surface Mount Component Standards

<table>
<thead>
<tr>
<th>PRODUCT FAMILY</th>
<th>REFERENCE DOCUMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed Resistors</td>
<td>EIA-575</td>
</tr>
<tr>
<td></td>
<td>EIA-576</td>
</tr>
<tr>
<td>Resistor Networks</td>
<td>EIA/IS-34</td>
</tr>
<tr>
<td>Variable Resistors (Potentiometers)</td>
<td>VRCI-SMT-300</td>
</tr>
<tr>
<td>Ceramic Chip Capacitors</td>
<td>EIA/198D</td>
</tr>
<tr>
<td></td>
<td>CB-11 Ceramic Chip Mounting Bulletin</td>
</tr>
<tr>
<td>Tantalum Capacitors</td>
<td>EIA-535 BAAC (Molded Case)</td>
</tr>
<tr>
<td></td>
<td>EIA-535 BAAD (Conformal Coated Case)</td>
</tr>
<tr>
<td></td>
<td>Pending (Molded Case-Fused)</td>
</tr>
<tr>
<td></td>
<td>Pending (Molded Case-Low ESR)</td>
</tr>
<tr>
<td></td>
<td>Pending (Application Bulletin)</td>
</tr>
<tr>
<td>Inductors</td>
<td>EIA/IS-XX (proposed)</td>
</tr>
<tr>
<td>Switches</td>
<td>EIA-520 EAAA (SM DIP SWS)</td>
</tr>
<tr>
<td></td>
<td>EIA/PN-2186 (Proposed SM Toggle)</td>
</tr>
<tr>
<td></td>
<td>EIA-PN-2251 (Proposed SM Push button)</td>
</tr>
<tr>
<td>Connectors</td>
<td>EIA/IS-XX (proposed)</td>
</tr>
<tr>
<td>Crystals</td>
<td>EIA-IS-XX (proposed)</td>
</tr>
</tbody>
</table>

**Resistors**

1999 Status and Action Plan

Section 4

Page 8
Flat chip resistors (thick and thin film), cylindrical resistors (MELF), resistor networks, and power resistors (film and wire wound) in surface mount configurations are now readily available from both domestic and foreign sources. Part sizes have been standardized. The parts are robust and withstand the traditional surface mount process stresses. When assembly process stresses are beyond the normal, care should be taken to insure the parts selected could withstand the stresses. Along with surface mount capacitors, resistors are amongst the highest part count on most boards. High-speed placement equipment minimize this impact by lowering the per piece assembly cost.

Surface real estate may also be more effectively utilized by minimizing surface mount resistors. Chip resistor arrays are being investigated. These are similar to networks, however the total package size is much smaller.

The EIA P1 committee, consisting of representatives from the manufacturers and major users oversees resistors. Their latest efforts are centered on upgrading the standards. EIA-575 for general purpose resistor chips, EIA-576 for precision resistor chips, and EIA/IS-34 for resistor networks provide performance requirements and test methods for solderability, effect of mounting, etc., along with environmental and life tests. VRCl-SMT-300, Published by the Variable Resistive Components Institute (VRCI) details the outlines, dimensions and land patterns for a 5mm square surface mount trimming in either gull wing or "J" lead configuration. EIA-575 and EIA-576 have replaced EIA/IS-30A and work continues on refining and updating EIA/IS-34.

**Capacitors**

Ceramic and tantalum surface mount capacitors are available in a wide variety of values and recognized standard sizes. Film and aluminum surface mount capacitors are also available, but up to this time have not attained the level of usage as have ceramic and tantalum.

Ceramic surface mount capacitors come in nine standard sizes (0402, 0603, 0805, 1206, 1210, 1812, 1825, 2220, and 2225) with the two largest (1812 and 1825) recommended only for reflow soldering. The EIA P2.1 Committee, consisting of representatives from the manufacturers and major users oversees ceramic capacitors. Their latest efforts are centered on establishing standards for low voltage ratings and performance criteria, physical standards, and accelerated test programs. The trend in ceramic capacitor offerings is two folds. Smaller sizes are becoming more predominant, and higher capacitance values are being offered in each case size. Ceramic capacitors are also being used in applications more traditionally employing electrolytic capacitors. Ceramic surface mount capacitors are robust and withstand the traditional surface mount process stresses. When assembly process stresses are beyond the normal, care should be taken to insure the parts selected could withstand the stresses.

Tantalum surface mount capacitors come in seven sizes (3216, 3528, 6032, 7343, the low profile 3216L and 3528L, and the high profile 7343H). The EIA P2.5 committee, consisting of representatives from the manufacturers and major users oversees tantalum capacitors. Their latest efforts are centered on establishing standards for low ESR tantalum capacitors, fused tantalum capacitors, physical standards, and application guidelines for the use of tantalum chip capacitors. (Drafts of these are in circulation for comment.) Like ceramic capacitors, smaller sizes are becoming more predominant and higher capacitance values are being offered in each of the case sizes. The new very high operating speeds of microprocessors have resulted in a high demand for extra high capacitance tantalum chips to be used as in decoupling applications.

The EIA P2.2 committee oversees film dielectric capacitors. Standards and guidelines are not yet available. At the beginning of the migration to surface mount, film capacitors were suffering from rise in temperature created from the reflow attach processes. The development of heat resistant films has made film capacitors better able to withstand the reflow attach processes. However, care must still be taken to insure the parts are not damaged. There are applications where film dielectric performance characteristics are important. When this is the case, either the solder process is controlled to allow the use of a surface mount film capacitor, or a leaded film capacitor is used.

Aluminum surface mount capacitors are not presently overseen by an EIA "P" committee. Surface mount aluminum capacitors are available. They should be soldered with care, as the surface mount process may be
detrimental to the performance of these parts. The manufacturers present recommendations regarding the soldering process parameters for using these parts.

**Inductors**

The EIA P2.3 committee oversees inductors. Standards and guidelines for surface mount parts are not yet available.

RF inductors have been available in surface mount configurations for several years but standardization has been slow. Registered outlines of three sizes of chokes have now been published in EIA-PDP-100. The 4.5-mm x 3.2-mm size (EIA SOPM-4532) has become the most widely used. Multilayer inductors of various sizes (similar to surface mount capacitors) are also widely used.

Large high current inductors and transformers have not been standardized and are often specially designed for individual applications. Because of the low quantity usage, through-hole inductive components are often added to SMT boards.

**Switches**

Switches for surface mount are available in several configurations and sizes. The Dual-In-line-Package (DIP) configurations are presently the most popular followed by some miniature toggle switches and a few push buttons. Two DIP types are registered in EIA PD-100 along with a programmable shunt. Surface mount DIP switches exist in the IECQ system. PQC41/USD0003, and in the NECQ System, EIA-520EAAA.

Similar specifications are in process for release by EIA. In addition, international committees for inclusion into the IECQ system are discussing new switches. While there are presently no existing known switches employing fine pitch FPT (<0.63-mm spacing), specifications may require alteration to the extent that the FPT assembly processes may differ from the SMT assembly process.

Since switches are not encapsulated as are SM resistors or capacitors, and since they require manual actuation, making them capable of withstanding the surface mount manufacturing environment is a very difficult proposition. SMT processes vary widely, so it is sometimes necessary to match switch capability with a given process.

The EIA P-13 Switch Committee has defined a typical vapor phase manufacturing environment in EIA 448-19 and a typical IR process in EIA-448-21. It has also developed a qualification test for SM switches, EIA-448-23, which incorporates IR or vapor phase reflow, plus cleaning, a long bake, and/or humidity cycling, to induce corrosion or hardening of any contaminants which may have entered the switch.

**Connectors/Sockets**

Few standards exist for connectors and sockets. Even the through-hole versions remain largely under-organized, due to the nature of unique user requirements and readiness of vendors to meet custom needs. The European community has supported the Eurocard concept using the German DIN standard connector. Now that the new international grid (IEC 97) is approved, it is probable that connectors with spacing of multiples of the 0.5-mm grid will become standardized for new designs. As apparent standard SMT connectors develop, the EIA P4 Committee will seek registration of connector outlines.

A series of connectors has been developed for the Standard Hardware Acquisition and Reliability Program (SHARP) at the Naval Air Warfare Center in Indianapolis, IN. These connectors are surface mounted to the edge of a double-sided module that plugs into a back plane, and are designated Standard Electronic Module (SEM) connectors. Several module card sizes are available, designated with letters, with B, D, and E the most popular. These standardized connectors utilize blade and tuning fork contact systems, with contacts on a 2.54 mm (0.100 in) positions in the standard 140 mm (5.44 in) overall length.
Recently a number of higher contact systems have been, or are being, developed to provide nearly 400 contact positions in the same length as the SEM connectors and for similar interconnection use. These "higher density" connectors are available with varied types of contact systems, with very limited inter-mating capability.

Various committees within the EIA are responsible for the definition of surface mount connectors and sockets. These committees include the CE-2.0 Committee on Connectors, the CE-3.0 Committee on Sockets, and the P-4 Committee on Electronic Part Mechanical Outlines. Documents authored by these committees include National Industry Standards, Interim Standards and Outline Drawings. Surface Mount configurations are shown in these documents as variations of through-hole products. The following released documents are available.

EIA CE-2.0 Committee:
   o IS-64: 2 mm two-part Connectors

EIA CE-3.0 Committee:
   o EIA-540AAAA: Detail Spec. For Type A Chip Carrier Sockets
   o EIA-540ABAA: Detail Spec. For PQFP Sockets
   o EIA-540ACAA: Detail Spec. For PLCC Sockets

EIA P-4 Committee:
   o SOEN-0001: SM Header
   o SOEN-0002: SM Module Board Connector
   o SOEN-0003: SM Header
   o SOEN-0004: SM Female Socket
   o SOEN-0005: SM Unshrouded Header
   o SOEN-0006: SM Female Socket

   NOTE: The above drawings are part of EIA-PDP-100

The IPC has a new document on design and application of SMT connectors. The new publication (IPC-C-406) discusses connector material, mounting characteristics, land patterns, solder joint, and assembly techniques.

There is an initiative supported by the IPC to generate a specification on Reliability Testing for Connectors based on a specification written by Hewlett-Packard. Berg Electronics has generated a similar specification. The cost to test a connector family exceeds $30,000. Connector standards will be the first step in getting the designer to consider the connector as part of the initial design for manufacturing (DFM) rather than waiting to the end of the design before determining what space and how many lines are needed.

Crystals

Surface mount crystals have been specialty items produced in configurations requested by users. The EIA P-11 committee is actively handling the standardization process. Because of the fragile, temperature and cleaning solvent sensitivity of crystals, they are sometimes hand placed and hand soldered on the interconnecting substrate. Alternately they may remain one of the few TH parts on the assembly.

Delay Lines

Delay lines are a specialty item and little, if any, standardization has or will take place. A few manufacturers offer surface mount versions of delay line components.

Indicators
LEDs (light emitting diodes) intended for surface mounting are of the subminiature fractional inch (0.100" square) or SOT23 configuration. They are designed to withstand 215°C vapor phase and 230-235°C convection / IR reflow environments. Cool down is critical and should be limited to 3-5°C/sec. maximum down to 100°C or lower.

There are no specific dimensional standards for LEDs but, in general, the manufacturers try to follow the chip capacitor outlines.

A new surface mount configuration released in early 1991 is a high intensity, low profile package, which conforms to the EIA IS28 size B tantalum capacitor outline. Its flat top and sides have been designed for automatic placement and it will be available in 12-mm tape for automatic component handling.

**Fuses**

Surface mountable fuses are just beginning to be readily available. As there is a trend toward circuit board replacement when trouble occurs, the use of fuses or other circuit protection devices mounted directly on the board serves to protect the more expensive semiconductor devices.

The standardization of SM fuse configuration is slow in taking place. Many applications of these devices are considered "special requirements" and the device is adapted from older fuse designs or a special design is made that satisfies the requirement.

There is now on the market some specific SM designs. These include:

- Fuse configurations in the outline packages nearly identical to the tantalum capacitor outlines. These are chips with fold-under terminations.
- Chip configurations similar to the tantalum capacitor outline with gull wing terminations.
- Special SM cylindrical fuses similar to the "MELF" configuration can be surface mounted.
- Surface mountable fuse clips are designed to hold subminiature standard glass fuses. These allow easy fuse replacement on the printed board. The fuse clips, however, are difficult to handle and the use of automated equipment for placement is usually impractical.

At the present time, there is no work for standardization of these devices by any US standardizing activity. Because of the limited number of manufacturers and users, the SM fuse standardization has had a lower priority that the work on other SM electronic parts.

Standardization work has been done at the international level in IEC Technical Committee 32C. A "Technical Trend" document, IEC Publication 127-4 TTD has been published which covers the general performance of fuses. Work is continuing in Working Group 6 of TC32C to develop more detailed requirements, including SM outlines and dimensions. Scheduled for 1992, the results of this work will produce a standard part 4 of IEC Publication 127 entitled, "Universal Modular Fuses", which will include SM parts. A draft of that document, REF. 32C/WG6 (Secretariat) 30, can be obtained from the U.S. fuse manufacturers.

**Active Devices**

Progress continues in registering and standardizing surface mount semiconductor packages. The summary document is JEDEC Engineering Publication 95. A list of the surface mount components is summarized in Table 3-2. Please note that Publication 95 is available in both electronic and hard copy and can be downloaded from the JEDEC home page: www.jedec.org free of charge.
Discrete Semiconductors

The availability of discrete devices, particularly special types, is continuing to improve. A good example is in the use of special power devices, where emphasis is being placed on plastic encapsulation with metal inserts that improves the power dissipation. For diodes, the emphasis seems to be concentrated on improvement of electrical characteristics rather than package change: MELF diodes in the traditional glass case appear to remain most popular.

Small Outline Integrated Circuits

The majority of SOICs utilize the gull wing lead form; however, "J"-bend leads are also used. Most of the outlines published are for plastic devices, although there is some activity in registration of ceramic devices. JEDEC has recently published thermally enhanced shrink versions of the popular SOP and TSOP packages to handle additional power requirements. These are commonly known as SSOP and TSSOP. This activity was coordinated with EIAJ to reduce proliferation.

Plastic Leaded Chip Carrier (PLCC or PQFP, where Q is for Quad)

The PLCC (PQCC) is a mature product now as evidenced by the JEDEC Standards MS-016 for the rectangular and MS-018 for Square PLCCs. The lead form is typically "J". This package is popular both in the United States and abroad. This package continues to grow in volume where profile height and foot print areas are not critical.

Quad Flat Packs (QFP)

This package utilizes a gull wing lead form, which permits the uses of all of the typical solder reflow methods, including hot bar soldering. In addition, most of these packages are dimensioned using "hard" metric. The standard QFP pitches are 1.0, 0.80, and 0.65 mm. The Fine Pitch QFP (FQFP) pitches are 0.50 and 0.40 mm. Significant problems have been encountered during assembly of FQFPs. The standard MQFPs and FQFPs are being replaced by the thinner versions LQFP and TQFP to meet lower profile height requirements. The LQFP and TQFP have also undergone some transformation by adding thermal enhancements to also handle new power requirements. Defects on the order of 200 - 300 PPMS are not unusual. This is driving the strong interest in BGA packages, which have demonstrated defect ratios of 3 - 5 PPMS.
<table>
<thead>
<tr>
<th>GENERIC DESCRIPTION</th>
<th>REGISTRATION/STANDARD NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small Outline C-Bend</td>
<td>DO-214 AA-AB</td>
</tr>
<tr>
<td>Small Outline C-Bend</td>
<td>DO-215 AA-BA</td>
</tr>
<tr>
<td>Gull Wing Plastic Surface Mount</td>
<td>DO-216 AA</td>
</tr>
<tr>
<td>Power Plastic C-Bend</td>
<td>DO-218 AA</td>
</tr>
<tr>
<td>SOT-23</td>
<td>TO-236(H) AA-AB</td>
</tr>
<tr>
<td>SOT-89</td>
<td>TO-243AA-AB</td>
</tr>
<tr>
<td>SOT-223</td>
<td>TO-261(B)</td>
</tr>
<tr>
<td>SOT-143</td>
<td>TO-253(D) AA</td>
</tr>
<tr>
<td>Surface Mount Header</td>
<td>TO-268</td>
</tr>
<tr>
<td>Surface Mount Header 4 lead</td>
<td>TO-269</td>
</tr>
<tr>
<td>Surface Mount QFP 4-Lead</td>
<td>TO-271</td>
</tr>
<tr>
<td>DPAK</td>
<td>TO-252AA</td>
</tr>
<tr>
<td>SMT Header Family</td>
<td>TO-263AA-AB</td>
</tr>
<tr>
<td>MELF Diode</td>
<td>DO-213AA-AB</td>
</tr>
<tr>
<td>C-Bend Diode</td>
<td>DO-214AA-BA</td>
</tr>
<tr>
<td>Gull Wing Diode</td>
<td>DO-215AA-BA</td>
</tr>
<tr>
<td>SOP-3.75 mm Body</td>
<td>MS-012AA-AC (Standard)</td>
</tr>
<tr>
<td>SOP-7.5 mm Body</td>
<td>MS-013AA-AF (Standard)</td>
</tr>
<tr>
<td>SOIC-11.2 mm (0.440&quot;) Body</td>
<td>MO-099AA-AB</td>
</tr>
<tr>
<td>SOP, Peripheral</td>
<td>MO-046</td>
</tr>
<tr>
<td>SOP, 8.4 MM Body</td>
<td>MO-059</td>
</tr>
<tr>
<td>SOP, Gullwing Leads</td>
<td>MO-117</td>
</tr>
<tr>
<td>SOP, 9.9 MM Body</td>
<td>MO-164AA-AB</td>
</tr>
<tr>
<td>SOP, 4 Lead</td>
<td>MO-269 AA</td>
</tr>
<tr>
<td>SOP, 5 Lead</td>
<td>MO-155</td>
</tr>
<tr>
<td>SOJ-0.300&quot; Body</td>
<td>MO-065AA-AB</td>
</tr>
<tr>
<td>SOJ-0.300&quot; Body</td>
<td>MO-088AA-AF</td>
</tr>
<tr>
<td>SOJ-0.300&quot; Body</td>
<td>MO-077AA-AC</td>
</tr>
<tr>
<td>SOJ-0350&quot; Body</td>
<td>MO-091AA-BA</td>
</tr>
<tr>
<td>SOJ-26/20-0.350&quot; Body</td>
<td>MO-063</td>
</tr>
<tr>
<td>SOJ-32/28-0.400&quot; Body</td>
<td>MO-061</td>
</tr>
<tr>
<td>SOJ-0.300&quot; Body</td>
<td>MO-119</td>
</tr>
<tr>
<td>SOJ-0.350&quot; Body</td>
<td>MO-120</td>
</tr>
<tr>
<td>SOJ-0.330&quot; Body</td>
<td>MO-121</td>
</tr>
<tr>
<td>SOJ-12 mm Body</td>
<td>MO-123</td>
</tr>
<tr>
<td>SOJ-12.7 mm Body</td>
<td>MO-124AA-BA</td>
</tr>
<tr>
<td>SOJ-10.15 mm Body</td>
<td>MO-165</td>
</tr>
<tr>
<td>SOJ-11 mm Body (Heat Slug)</td>
<td>MO-166AA-AE</td>
</tr>
<tr>
<td>SOJ-.415 Body Ceramic</td>
<td>MO-147</td>
</tr>
<tr>
<td>SOJ-16 mm Wide Metric</td>
<td>MO-181 AA</td>
</tr>
<tr>
<td>SOT- 5 &amp; 6 Lead</td>
<td>MO-203 AA-AB</td>
</tr>
<tr>
<td>Low Profile SOJ</td>
<td>MO-199 AA-AJ</td>
</tr>
<tr>
<td>Stacked SOJ</td>
<td>MO-200 AA-BB</td>
</tr>
<tr>
<td>SO-Leadless-0.400 Body</td>
<td>MO-126AA-AB 0.050&quot;</td>
</tr>
<tr>
<td>Description</td>
<td>Code</td>
</tr>
<tr>
<td>-------------------------------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>SO-Leadless 7.0 mm Body</td>
<td>MO-196 AAA-VLE</td>
</tr>
<tr>
<td>Leadless Surface Mount Package</td>
<td>MO-197 AA-AC</td>
</tr>
<tr>
<td>TSOJ-0.300” Body</td>
<td>MO-105AA 0.050”</td>
</tr>
<tr>
<td>SSOP-0.300” Body</td>
<td>MO-118AA-AB 0.025”</td>
</tr>
<tr>
<td>SSOP Family .150” Body</td>
<td>MO-137AA-AF 0.025”</td>
</tr>
<tr>
<td>SSOP-5.3 mm Body</td>
<td>MO-150AA-AK</td>
</tr>
<tr>
<td>SSOP (QVSOP) 3.9 Body</td>
<td>MO-154</td>
</tr>
<tr>
<td>SSOP .4 mm, .5 mm, .65 mm Pitch</td>
<td>MO-152AA-JD</td>
</tr>
<tr>
<td>TSSOP .4 mm, .5 mm, .65 mm Pitch</td>
<td>MO-153AA-JDT-1</td>
</tr>
<tr>
<td>TSSOP 8 lead</td>
<td>MO-187</td>
</tr>
<tr>
<td>TSSOP</td>
<td>MO-194 AA-BBT</td>
</tr>
<tr>
<td>TSOP-I</td>
<td>MO-142AA-DD 0.5 mm pitch</td>
</tr>
<tr>
<td>TSOP-I</td>
<td>MO-183 AA. 0.5 mm pitch</td>
</tr>
<tr>
<td>6 Lead TSOP</td>
<td>MO-193 AA</td>
</tr>
<tr>
<td>TSOP-II 7.62 mm Body</td>
<td>MO-132AA-CA 1.27 mm</td>
</tr>
<tr>
<td>TSOP-II 10.16 mm Body</td>
<td>MO-133AA-CA</td>
</tr>
<tr>
<td>TSOP-II 12.7 mm Body</td>
<td>MO-135AA-CA</td>
</tr>
<tr>
<td>TSOP-II 10.16 mm Body</td>
<td>MS-024 AA-FB</td>
</tr>
<tr>
<td>TSOP II, 16 mm Wide</td>
<td>MO-182 AA-BA</td>
</tr>
<tr>
<td>PLCC-Square</td>
<td>MO-047AA-AH 0.050”</td>
</tr>
<tr>
<td>PLCC, Rectangular</td>
<td>MS-016</td>
</tr>
<tr>
<td>PLCC-Rectangular</td>
<td>MO-052AA-AE 0.050”</td>
</tr>
<tr>
<td>PLCC-Square</td>
<td>MS-018</td>
</tr>
<tr>
<td>PLCC-Rectangular 0.050”</td>
<td>MS-016AA-AE (Standard)</td>
</tr>
<tr>
<td>PLCC-Square, Ceramic “J” Lead</td>
<td>MO-087 0.050”</td>
</tr>
<tr>
<td>Non-hermetic Leadless CC .050Pitch</td>
<td>MO-075</td>
</tr>
<tr>
<td>Non-hermetic Leadless CC .050Pitch</td>
<td>MO-076 SO Series</td>
</tr>
<tr>
<td>Leadless Rectangular .040 Staggered Pitch</td>
<td>MO-085</td>
</tr>
<tr>
<td>Plastic Flat Pack w/Heat Slug</td>
<td>MO-162</td>
</tr>
<tr>
<td>LCC-0.050” Pitch –Leadless Type A</td>
<td>MS-002 (Standard) 0.050 Pitch</td>
</tr>
<tr>
<td>LCC-0.050” Pitch –Leadless Type B</td>
<td>MS-003 (Standard) 0.050 Pitch</td>
</tr>
<tr>
<td>LCC-0.050” Pitch –Leadless Type C</td>
<td>MS-004 (Standard) 0.050 Pitch</td>
</tr>
<tr>
<td>LCC-0.050” Pitch –Leadless Type D</td>
<td>MS-005 (Standard) 0.050 Pitch</td>
</tr>
<tr>
<td>Ceramic Leaded Chip Carrier Type B</td>
<td>MS-009 (Standard) 0.050 Pitch</td>
</tr>
<tr>
<td>Leadless Ceramic Type B</td>
<td>MS-014 (Standard) .040” Pitch</td>
</tr>
<tr>
<td>Leadless Ceramic Small Outline</td>
<td>MO-144</td>
</tr>
<tr>
<td>Plastic Quad Flat Pack Bumperered, Family (Gullwing)</td>
<td>MO-069AA-AH 0.025”</td>
</tr>
<tr>
<td>Plastic Quad Flat Pack Bumpered, Thin Lead Family (Gullwing)</td>
<td>MO-071AA-BB 0.025”</td>
</tr>
<tr>
<td>Plastic Quad Flat Pack Bumpered, Low Profile (Gullwing)</td>
<td>MO-086AA-AH 0.025”</td>
</tr>
<tr>
<td>Plastic Quad Flat Pack Bumpered (Gullwing)</td>
<td>MO-089 0.050”</td>
</tr>
<tr>
<td>TapePak/Molded Carrier Ring</td>
<td>MO-094AA-BD</td>
</tr>
<tr>
<td>TapePak/Molded Carrier Ring, Fine Pitch</td>
<td>MO-109</td>
</tr>
<tr>
<td>Power PQFP w/Heat Slug</td>
<td>MO-188 AA-BH</td>
</tr>
<tr>
<td>Power QFP w/Heat Slug</td>
<td>MO-189 AA-BC-1</td>
</tr>
<tr>
<td>Power QFP</td>
<td>MO-204 AA</td>
</tr>
</tbody>
</table>
Vertical Surface Mount MO-141
Staggered Surface Mount Package MO-213 0.4 mm pitch
Tape Ball Grid Array MO-149AA-CU-1X
Plastic Ball Grid Array (Square) MO-151AAA-CBA
Plastic Ball Grid Array (Rect.) MO-163AA-AB
Low Profile Ball Grid Array MO-192 AA-CBA
Low Profile Fine Pitch BGA 0.80 mm pitch MO-205 AA-BL
Rectangular Chip Size, FBGA Family MO-207 AAY-CAY
Die Size BGA MO-211 AA-BG
Thin BGA 1.00 and 0.80 mm pitch MO-216 AAA-BAY
Thin Fine Pitch BGA 0.50 mm pitch MO-195 AA-DB
Ceramic Ball Grid Array (Square) MO-156AA-CU
Ceramic Column Grid Array (Square) MO-158AA-CL
Thin Fine Pitch Ball Grid Array MO-195 AA-BU
Metric Quad Flat Pack (Body +3.2) MO-108AA-FA
Metric Quad Flat Pack (Body +3.2) MS-022 AA-GC
Metric Quad Flat Pack (Body + 3.9) MO-112AA-FA
Thin Quad Flat Pack Family MO-136AA-BX
Fine Pitch Quad Flat Pack, 0.4 mm/0.5 mm Pitch MS-029 AA-KA
Low and Thin Profile Quad Flat Pack MS-026 AAA-BJC
PQFP Three Tiered MO-198 AA-AF
Stacked TSOP MO-201 AA-AB
64 Lead Surface Mount ZIP MO-202 AA

TAB - English Dimension UO-017
TAB - Metric Dimension UO-018
TAB - Metric Dimension US-001

Ceramic Quad Flat Pack, 256 Leads MO-100AA 0.020"
Ceramic Quad Flat Pack, .050 Pitch MO-081
Ceramic Quad Flat Pack MO-082AA-AF 0.025"
Ceramic Quad Flat Pack, Guard Ring, 132 Leads MO-104AA 0.025"
Ceramic Quad Flat Pack, MO-090AA-AF 0.015"
Ceramic Quad Flat Pack, MO-084AA-AF 0.050"
Ceramic Leaded Chip Carrier MO-044, 0.050" Pitch
Ceramic Leaded Chip Carrier MO-107AA-AE 0.050"
Ceramic Leaded Chip Carrier MO-129AA-AB 0.015"
Ceramic Leaded Chip Carrier MO-130AA 0.015"
Ceramic Leaded Chip Carrier MO-131AA-AD 0.025"
Ceramic Leaded Chip Carrier MS-006 Type A 0.050 Pitch
Ceramic Leaded Chip Carrier MS-007 Type A 0.050 Pitch
Ceramic Quad Flat Pack MO-134AA-AE 0.5mm
Ceramic Flat Pack MO-146
Ceramic Chip Carrier, .025 Pitch MO-062
Ceramic Chip Carrier, "J" Lead. MO-087AA-AE 0.050"
Ceramic Round Lead "J" Lead
Ceramic Round Lead, "J" Lead,
Ceramic Round Lead, "Gull" Lead, MO-111 0.050"
Ceramic Quad Flat Pack, w/Tie Bar MO-113 0.025"
Cerquad Family w/Gullwing Leads MO-114
Ceramic Quad Flat Pack, 132 Lead MO-060 0.040"
Ceramic Quad Flat Pack, 196 Lead MO-125 0.025"
6.35 mm Cerpak Leaded Flat Pack MO-092AA-AD 0.025"
Braze Lead Flat Pack MO-098AA-AD 0.050"
Top Brazed 48 Pin Flat Pack MO-101AA-AB 0.050"
Flat Pack, .200" Width, .050" Pitch MO-003 AA-AK
Flat Pack, .300” Width, .050 Pitch MO-004 AA-AM
Flat Pack Family, 0.535” Long, 0.303” Pitch MO-106AA-AC 0.030”
Flat Pack, 32 Lead MO-115 0.050”
Flat Pack, 10.15 mm Width MO-018 (C) .89 mm Pitch
Flat Pack, 10.16 mm Width MO-019, AA-AF 1.27 mm Pitch
Flat Pack, 12.70 mm Width MO-020 (C), 1.27 mm Pitch
Flat Pack, 15.24 mm Width MO-021 (C), 1.27 mm Pitch
Flat Pack, 17.78 mm Width MO-022 (D), AA-AE 1.27 mm Pitch
Flat Pack, 22.86 mm Width MO-023 (C), 1.27 mm Pitch
Flat Pack, 16.64 mm Width MO-032, AA-AF 1.27 mm Pitch, 16.64 mm body
Flat Pack, Leadless MO-027, 1.27 mm Pitch
Lateral (Leadless) Ceramic CC, MO-056AA-HC 0.025”
Lateral (Leadless) Ceramic CC, MO-057AA-JC 0.020”
Ceramic Multichip Module Family MO-148

Ceramic Lateral (Leadless) Chip Carriers (LCC)

Ceramic Lateral Leadless Chip Carriers (LCC, where the L means lateral, not Leadless), entered the packaging scene as the solution for increased density. The packages offer hermetically and good electrical performance (since all conductor paths are short and essentially the same length). Early experience with small package sizes was successful. As package sizes grew larger, problems occurred with cracked solder joints when the CLCCs were mounted on laminate PC board.

This has led to the increased use of leaded ceramic packages for the larger packages and for high reliability applications.

Ceramic Leaded Chip Carriers (LDCC)

The ceramic leaded chip carrier (LDCC) is a modification of the leadless version. It has filled a much-needed void and is now one of the most dependable packages for higher lead counts reliable circuits. Where a higher level of reliability is preferred, the LDCC is used instead of the LCC. The need for higher and higher lead count circuits is resulting in the closer lead pitch approach, similar to what is being seen in the quad packs (1.0, 0.80, 0.65, & 0.50mm as well as 50 and 25 mil pitches). Along with the advantages of the fine lead pitch are the disadvantages, as listed earlier. Military programs in particular are placing very strong emphasis on the use of LDCC for surface mount systems.

Dual In-Line Packages (DIP)

Without question, the dominant integrated circuit package in the past was the dual in-line package (DIP) 70 and 100 mil pitches. Whether it was a multilayer ceramic (co-fired) side brazed package, a pressed ceramic (CERDIP) package, or a plastic encapsulated package, it has withstood the test of time and emerged as the primary packaging configuration of the microelectronics industry. Unfortunately, the needs of the industry has changed requiring lower profile, higher lead count, smaller foot print, and finer pitch surface mount packages which begun to reduce the overall volumes of DIPs used. Consequently, it is being replaced by MQFP, PLCC, and SOIC surface mount packages. The trend today appears to be that the DIP will still be used where the end customer requires low lead count through-hole packages. Some designs call for surface mounting the DIP. This can be accomplished by shortening the leads and mounting the parts in "I" beam or butt lead fashion.

Single In-Line Packages
The single in-line package (SIP) component is similar to the DIP with leads that exit the component body "in-line" 2.54-mm (0.100-inch) pitch. The lead pattern is in a single row. This component configuration is usually associated with resistor networks and smart power applications. Although intended for through-hole mounting, many SIPs have been transformed into surface mount packages by shaping the leads into the gull wing configuration. SIPs have also been used as a Multichip module configuration for mounting memory chip arrays in PLCC and SOIC packages. These are also available with leads that exit the component body "in-line" 1.27 mm (050 mil) apart.

Flat Packs

The flat pack has been commonly used in military applications over the years, and falls into the category of higher lead count surface mounted hermetic packaging. As such, it is now gaining popularity for hermetic applications and may eventually replace the DIP. Versions appear in the form of ceramic multilayer co-fired brazed leaded flat pack, pressed ceramic Cerpak flat pack, and plastic encapsulated packages. Typically, the leads are formed into a gull wing configuration, although some J-bend configurations have been built. The ceramic flat pack usage over the last few years has been decreasing while the growth of the plastic know as an SOP (Small Outline Package) is now the highest volume plastic package produced in our industry. The SOP has two lead configurations: a gull wing called A SOIC and a J bend version called SOJs

Area Array Packages

Pin Grid Arrays (PGA) have been around for over twenty years. It is only recently that they have come into prominence for high pin count circuits. The PGA is not an SMT package; its design was for the through-hole mounted board and it is still primarily being used in that manner. There have been attempts to carefully prepare the lead tips so that the package can be surface mounted in "I" butt joint fashion. These are known as Surface Mount PGAs (SMPGA) and they usually have smaller lead diameters and finer pitches. The uses of the PGA for “I” butt joint assembly causes one major problem which "I" butt joint LDCC or quad pack does not have. That is in the area of repair or rework. Since the PGA has rows of leads inside the periphery and under the body of the package, it is impossible to reach it to do any rework. They are not intended to go into the printed board assembly. They are butts soldered to the lands on the top layer of the surface.

There is work going on to develop a soldering method which would be more amenable to "I" butt joint soldering so the PGA can be used in surface mount applications with a higher level of reliability.

A new area array package is evolving. This package has lands (or pads) in a grid array and omits the pins altogether. It often has solder bumped pads on the bottom of the package, which are typically soldered directly to the plated metallization on the interconnecting substrate. The common name for this package in the industry is Ball Grid Array (BGA). This package is under investigation by several companies, because it offers high lead counts on reasonable centerline spacing and the associated higher yield potential. This also permits a smaller package to be used when compared to a fine pitch peripheral leaded QFP. Attention must be paid to routing density on the interconnecting substrate because of the fine pitch visa associated with this package design. Other critical issues with this concept are placement accuracy and having sufficient solder joint height to insure compliance. Some companies are using under package encapsulation to help alleviate the compliance problem. Of course the solder joints are not easily inspected, causing some to question assembly quality. Soon the industry will have to let go of that not-so-ancient proverb: "If your can't see it, don't solder it."

Outlines for Plastic Ball Grid Array, Ceramic Ball and Column Grid Array packages have been issued.

Fine Pitch Quad Flat Packs (FQFP), Thin Small Outline Packs, and Plastic QFPs
As higher and higher lead count packages are developed, it is necessary to develop finer pitch lead spacing in order to keep the body size from growing too large. The typical fine pitch spacing now in use is 0.80, 0.65, 0.50, and 0.40 mm. These packages are smaller, denser versions of the QFP and SOICs, in either plastic or hermetic form. Fine pitch packages are defined as any whose final encapsulated form has external lead spacing of 0.65-mm pitch or less. Some of the current package type names are SOP, TSOP, SSOP, TSSOP, FQFP, LQFP, TQFP, MQFP, CQFP, SSOP and TSSOP. Virtually all of the new fine pitch packages use the gull wing lead shape, instead of the "J" or leadless options. These fine pitches require sophisticated and very tightly controlled assembly processes.

With the drive toward higher densities, the quad flat pack is undergoing a significant reduction in package thickness. Previous packages were all greater than 2.0 mm thick. Recent package thicknesses are 1.4 and 1.0 mm.

**Bare and Minimally Packaged Solid State Devices for Direct Attach**

These packages are now commonly called “chip size”, reflecting their small size.

Flip chip
Bare chip
Micro SMT
TFBGA

**Tape Automated Bonding - TAB (Tape Carrier Package - TCP)**

The drive to higher density, faster performance, and higher lead counts has resulted in an increased interest in TAB. TAB construction consists of an integrated circuit bare die, which is attached (inner lead bonded) to a thin, etched copper lead frame, which is supported by plastic. The outer leads of the frame are subsequently attached (outer lead bonded) into either a single or Multichip package or directly to a mounting and interconnect substrate. Inner lead bond spacing is as small as 75 microns and outer lead bond spacing is as small as 150 microns. TAB remains an application specific packaging concept and is not considered a main stream technology. This technology has been limited in it success because the end user must have a lead trimming and forming operation prior to assembly.

**Flip chip**

As electronic systems become smaller and denser, the need for higher I/O IC’s in smaller packages is increasing. Flip chips (which are bare die with solder bumps on the interconnect pads) are receiving renewed interest by product and component designers. Flip chip packaging is not new, IBM, Delphi Delco Electronics Systems has used it, and others for over 30 years, primarily in ceramic substrate based applications. With advent of “underfill” which is an epoxy material which is placed between the chip and the substrate (encapsulation the solder bumps and neutralizing the shear stresses on the bumps), flip chips can now have broad application on laminate substrates. The Surface Mount Council is coordinating the activities of EIA and IPC groups working on standards required for this technology. J-STD-010 was published in January of 1995.

**Bare chip**

Increases in packaging densities for portable telecommunications and other consumer applications, have increased the use of bare die attach. In this case the bare (unpackaged) solid state device is attached directly to the mounting and interconnecting structure.

**Micro SMT**

The substrate used to make the integrated circuit is also used to construct the Micro SMT package. This is accomplished by extending the substrate area and using a combination of metallization and epoxy. The resulting package is slightly larger (>20%) than the bare unpackaged solid state device.
Thin Fine Pitch BGA (TFBGA)

Figure 4-2
Fine Pitch Ball Grid Array Package

This package consists of a bare, peripherally leaded integrated circuit die that is either connected using single layer TCP (TAB) to the top of a double sided flex circuit or a multilayer laminate. The options for FBGA are continuing to grow as new ideas are formulated. Over the next couple of years the most cost-effective options will become the clear-cut winners. The memory applications are the volume drivers for this package style. The Surface Mount Council is coordinating the activities of EIA and IPC groups working on standards required for this technology. J-STD-012 was published in January of 1995 as a guide to the standardization activities.

Multichip Modules (MCM)

Multichip modules are projected to become very popular in the near future. In December 1992 a revision to the PGA Registered Outline MO-067, adding a few larger sizes for MCM applications, was approved for publication. A perimeter leaded MCM Outline MO-148 was also published.

Dual-in-line Memory Modules

Dual-in-line Memory Modules have been manufactured for use in computers for several years. Many of the new fine pitch ball grid array and other chip size/scale packages are bring mounted on DIMM modules to permit high-density memory assemblies.

Following is a list of the DIMM module outlines contained in JEDEC Publication 95:

<table>
<thead>
<tr>
<th>MO Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MO-116</td>
<td>30 I/O Single-in-line-memory-module (SIMM)</td>
</tr>
<tr>
<td>MO-160</td>
<td>72, 84, 88 I/O 1.27 mm pitch DIMM</td>
</tr>
<tr>
<td>MO-161</td>
<td>100, 168 I/O 1.27 mm pitch DIMM</td>
</tr>
<tr>
<td>MO-167</td>
<td>128 I/O 1.27 mm pitch DIMM</td>
</tr>
<tr>
<td>MO-172</td>
<td>112, 200 I/O 1.27 mm pitch DIMM</td>
</tr>
<tr>
<td>MO-179</td>
<td>111, 200 I/O 1.00 mm pitch DIMM</td>
</tr>
</tbody>
</table>
### Component Packaging for Handling

The EIA Automated Component Handling Committee (ACH, formerly the ACPI) and JC-11 have been working on industry packaging standards. Standard RS-481-Rev A, "Taping of Surface Mount Components for Automatic Placement" was published in February 1986. The ACH has extensively reviewed 481, including its breakdown into three separate standards recognizing several handling differences between 8 and 12 mm tapes, 16 and 24 mm tapes, and 32, 44 and 56 mm tapes. EIA-481-1 (8 and 12 mm), 481-2 (16 and 24 mm) and EIA-481-3 (32, 44, and 56 mm tapes) have been issued as EIA standards.

Meetings have taken place with the ACH counterparts within EIA Japan and the IEC Europe with the purpose of bringing the European, Japanese, and American "Taping Standards" in close harmony.

The JC-11 Committee has issued registered outlines for matrix trays and TAB carriers for component handling. These can be found in JEDEC Publication No. 95. Future work of these committees will include TAB carrier and MCR (Molded Carrier Ring) tubular magazines, bulk packaging of high volume SM resistors and capacitors, and alternate taping technologies.

<table>
<thead>
<tr>
<th>MO-185</th>
<th>72 I/O 1.27 mm pitch DIMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>MO-190</td>
<td>144 I/O 0.8 mm pitch SODIMM</td>
</tr>
<tr>
<td>MO-191</td>
<td>160 I/O 1.27 mm pitch DIMM</td>
</tr>
<tr>
<td>MO-206</td>
<td>184 I/O 1.27 mm pitch DDR DIMM</td>
</tr>
<tr>
<td>MO-214</td>
<td>144 I/O 0.5 mm pitch Micro DIMM</td>
</tr>
<tr>
<td>MO-215</td>
<td>210 I/O 1.00 mm pitch SDRAM DIMM</td>
</tr>
</tbody>
</table>
Section 5
Interconnection Substrates

Packaging and Interconnect structures in the past could be divided into commercial and military categories. The major difference between the two has been associated with the military requirement for hermetic packaging and severe environmental resistance. The military market has virtually eliminated hermetic packages except in special applications and now uses mostly plastic packages. The commercial market has almost completely converted to plastic packages with the elimination of ceramic packages for microprocessors.

5.1 Commercial P/I Structures

Interconnection substrates for commercial, rigid board products are primarily glass reinforced organic laminates. The resin materials used are phenolic, epoxy, BT, polyimide, cyanate ester, Teflon, IPN resins and combinations of some of the resins. Phenolic laminates are used primarily in single sided printed board applications. The standard difunctional epoxy resin is by far the most widely used of these resins for multilayer boards. Higher temperature epoxy, BT, polyimide, IPN and cyanate ester resins are used for specialty applications. BT resins have become more widely used due to the semiconductor manufacturers selecting them for use in device packaging applications such as PBGAs. The laminate reinforcement materials used with these resins are paper, non-woven glass, woven glass, and non-woven aramid material.

Ceramic substrates are seldom used for printed board (PB) replacements in commercial applications. They are mostly used in hybrid components or in multichip modules in various component forms on standard printed wiring boards. Ceramic hybrid substrates are widely use in high temperature applications such as “under the hood” automotive. Multilayer ceramic substrates are also used in multichip modules for the central processing unit of some mainframe computers.

Flexible circuit substrates using polyimide flex tape materials and combination rigid/flexible laminated structures are also used for commercial products. These systems are used for specialized packaging requirements to make the interconnection between two or more rigid printed boards. There are two classes of these materials: 1) flex to install and 2) flexible application with large cycle to failure requirements such as a flex cable for a print head on a printer. Polyimide flex materials are also widely used in tape PBGA semiconductor packaging applications.

Printed boards molded with thermoplastic resins, can be made into two or three dimensional shapes and are generally used in low density interconnect structures utilized in high volume consumer type products.

Consumer PWB substrates primarily utilize reinforcement laminated materials made from paper, non-woven glass and woven glass products with phenolic and epoxy resin systems. These products range from single sided up to about 6 layers. Only a few years ago most consumer electronics products were one-sided paper reinforced phenolic laminate, with limited SMT utilization. Today, most new consumer electronics products use both leaded through hole and SMT components with the most advanced products using 0.5mm pitch plastic quad flat packs (PQFPs) with up to 28mm body size and 208 I/O. The 0.4mm pitch PQFPs with up to 256 I/O is also used. Plastic ball grid arrays (PBGAs) with 1.5 and 1.27mm pitch with I/O count are often used above 208 I/O. At 28mm body size the PBGAs have 324 I/O for 1.5mm pitch and 441 I/O for 1.27mm pitch. A new class of array type device package called Chip Scale has emerged with solder ball pitch below 1.0mm down to 0.5mm. The PBGA and Chip Scale packages are sometimes combined into three categories of PBGA packages. The first is for solder ball pitch of 1.5 and 1.27mm. A second category of high density PBGAs is used for solder ball pitches of 1.0 to 0.5 mm and a third category of very high density PBGAs for pitches below 0.5mm. These types of device packages have allowed the further development of high performance, lightweight consumer electronics.

Packaging and Interconnecting (P/I) substrates are going through a change driven by the introduction of these “array” packaging methods for semiconductors. The PQFP at 1.5mm and 1.27mm pitch and the peripheral leaded packages with lead pitch down to 0.5 mm have been designed with standard plated through hole printed board technology with reasonable layer counts and low cost. The PQFP solder land pitch of 0.5 mm has not been a routing
problem for standard technology PWBs with mechanically drilled holes. As the I/O count has increased the PQFP no longer supports the semiconductor need in a reasonable size package without going to a 0.4mm pitch package which has proven difficult to assemble. The PBGA package has become the package of choice above 208 I/O.

The wiring density for the PQFP package ranges from 0.28 I/O per sq mm for a 20mm square package to 0.17 for a 40mm square package. As Table 5.1 below shows the PBGA package has 2X to 3X the lead count in the same area on the P/I structure.

**Table 5-1 I/O Density for 0.5 mm pitch QFP and 1.27 mm Pitch PBGA Packages**

<table>
<thead>
<tr>
<th>PQFP Body Size</th>
<th>PQFP I/O</th>
<th>PQFP I/O Density, I/O per sq mm</th>
<th>PBGA Body Size</th>
<th>PBGA I/O (full array)</th>
<th>PBGA I/O Density, I/O per sq mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>144</td>
<td>0.28</td>
<td>21</td>
<td>256</td>
<td>0.58</td>
</tr>
<tr>
<td>28</td>
<td>208</td>
<td>0.22</td>
<td>29</td>
<td>484</td>
<td>0.56</td>
</tr>
<tr>
<td>36</td>
<td>272</td>
<td>0.18</td>
<td>35</td>
<td>729</td>
<td>0.60</td>
</tr>
<tr>
<td>40</td>
<td>304</td>
<td>0.17</td>
<td>40</td>
<td>961</td>
<td>0.60</td>
</tr>
</tbody>
</table>

For size driven applications like hand held products and high I/O applications the PBGA has become the package of choice. The impact of this change from peripheral to array package on the PWB substrate is substantial. As can be seen from Table 5-1 the I/O density must now be supported with more vias per unit area and greater wiring density to access those vias that are attached to solder lands. Table 5-2 below shows the impact on I/O for PBGA packages with three levels of wiring density.

PTH land size, PTH drill size, and the line and space size limit the I/O count. The motherboard via pitch must match the package pitch and the PWB via drill fabrication technology is usually 0.25-0.30mm. From Table 5-3 below this drill size is adequate for 1.5 and 1.27 mm solder ball pitch s. The 1.0 pitch requires a drill size of 0.2mm and will usually result in an increased PWB motherboard cost with mechanically drilled vias. Below 1.0mm solder ball pitch the standard drilled-hole technology for the PWB will be marginal for the transition to high-density PBGA packages.

**Table 5-2 Number of I/O vs. array size on two layers of circuitry with varying wiring densities**

<table>
<thead>
<tr>
<th>Array Size</th>
<th>Total Leads (full array)</th>
<th>Number of Conductors between Vias (# I #)</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 X 14</td>
<td>196</td>
<td>192 # I # 196 # II # 196 # III #</td>
</tr>
<tr>
<td>16 X 16</td>
<td>256</td>
<td>236 # I # 256 # II # 256 # III #</td>
</tr>
<tr>
<td>19 X 19</td>
<td>361</td>
<td>272 # I # 316 # II # 352 # III #</td>
</tr>
<tr>
<td>21 X 21</td>
<td>441</td>
<td>304 # I # 356 # II # 400 # III #</td>
</tr>
<tr>
<td>25 X 25</td>
<td>625</td>
<td>368 # I # 436 # II # 496 # III #</td>
</tr>
<tr>
<td>31 X 31</td>
<td>961</td>
<td>464 # I # 556 # II # 640 # III #</td>
</tr>
<tr>
<td>35 X 35</td>
<td>1225</td>
<td>528 # I # 638 # II # 736 # III #</td>
</tr>
</tbody>
</table>

Source: IPC-7095
Table 5-3 Critical PBGA Design Parameters

| Critical Design Parameters for PBGA Board Routing-Bottom Surface (Dimensions in mm) |
|---------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Solder Ball Pitch/Design Parameter | 1.5  | 1.27 | 1.0  | 0.8  | 0.65 | 0.50 |
| Solder Ball Diameter              | 0.75 | 0.75 | 0.60 | 0.50 | 0.40 | 0.30 |
| Solder Pad Diameter               | 0.50 | .050 | 0.40 | 0.35 | 0.30 | 0.25 |
| PTH Diameter *                    | 0.30 | 0.30 | 0.20 | 0.20 | 0.20 | 0.15 |
| PTH Land Diameter                 | 0.50 | 0.50 | 0.40 | 0.40 | 0.40 | 0.40 |
| Line Width** for 1 line per channel | 0.30 | 0.25 | 0.20 | 0.125 | 0.075 | 0.075 |
| Line Width for 2 line per channel | 0.20 | .015 | 0.12 | 0.075 | 0.050 | 0.050 |

Source: Hayward (AMD), Future Circuits International

* Assumes mechanically drilled holes  ** Assumes 1 conductor between via pads

Figure 5.1a shows the crosssection for a PBGA with a 1.5mm and 1.25mm pitch mounted on a standard mechanically drilled PWB. Figure 5.1b shows the one line per channel fanout required on the motherboard. Table 4.3 shows that the line size must be decreased to 0.15mm for two lines per channel for the 1.25mm pitch PBGA. For the 1.0mm pitch PBGA the drill size must decrease to 0.20mm for a 0.2mm line to fanout with one line per channel. At the 0.2mm drill size the motherboard cost will increase with mechanical drilling and thus is not acceptable to the user community.

Figure 5.1a Typical PWB Cross section for 1.5 & 1.27mm Pitch PBGA
In order to achieve smaller form factors the hand held consumer applications have been the first to move into high density interconnect structures such as built up multilayers. This HDIS type structure will be discussed in more detail later. The driving force in these applications is the use of CSP and PBGA packages with 1.0mm to 0.5-mm array pitch to achieve a smaller form factor.

**P/I Structure Materials**

Computer, telecommunications and industrial products are almost all based on epoxy resin/woven glass reinforced laminate structures of 2-14 layers. In recent years the need for higher processor operating speeds and more uniform P/I structures have led to a reevaluation of the base laminate construction materials used in making the multilayer products for these applications. Discrete wiring boards that have better control over electrical performance are also finding wide use in high-speed computer applications.

Laminators throughout the world, use different woven glass styles as the reinforcements for the single or double-sided copper clad laminate used in multilayer construction. The variations in laminate are designed to enhance the properties of the material for such characteristics as resistance to processing chemicals, resistance to measing or cracking, ease of drilling, improved dielectric constant and reduced loss tangent, machineability, availability or cost. As a result of the variations in manufacturing processes and equipment used by the world laminate community a wide variety of laminate constructions can be used to construct a particular thickness of laminate. A designer could specify a particular laminate core thickness, and when purchased from three different laminators, have the construction be significantly different with a different resin content, a different glass style, and a different dielectric constant, yet all achieving the same thickness.

Because of the need for impedance control boards, with control of dielectric constant and inter-laminate spacing, users are finding it difficult to use materials from different laminators in building their product. Manufacturers of base materials have maintained that the glass style used within their product was proprietary and that they were free to use various glass styles to meet a given thickness requirement. In 1991, a program was started where the IPC Base Material Committee has attempted to break down these barriers, and laminators throughout the world have participated in this program. Table 5-4, FR-4 Copper Clad Laminate Construction Selection Guide is intended to provide the consistency needed for computer, automotive and telecommunications products of the 1990’s. The selection guide was developed by users and manufacturers of base material, and shows 31 different thickness of glass cloth and epoxy resin (base material) used in making epoxy glass copper clad laminate. As can be seen from the table, there are times when the construction thickness are very close to one another, however the resin content
and glass styles are relatively different in an attempt to meet the needs of the users for performance or cost driven products.

In 1993, information in Table 5-4 was published in IPC-CC-110. It is expected that this new document will lead to market standardization by designers calling the document out on the drawing. This standardization and registration of the defined laminates will be of significant benefit to the industry, so that no matter who provided the material the characteristics would be identical or identical within the tolerance limits specified for the various characteristics. A companion selection guide has also been prepared for prepreg. The higher performance resin systems (BT, polyimide and cyanate ester, or blends with epoxy) are used in limited volume on 10-45+ layer multilayer structures, and/or higher performance systems for computers and telecommunications and industrial products. The BT resin is unique among the high performance materials due the application in PBGA packaging.

**P/I Structure Design Considerations**

SMT design is used on most microprocessor based computer type systems and peripherals. The common medium density SMT design utilizes 0.65 mm PQFP and 1.25 mm pitch small outline (SO) devices on one side, discrete components on the opposite side. The P/I structure uses finished line widths and spacing between 0.125 and 0.175 mm (0.005 to 0.007”) with drilled via interconnect holes from 0.33 to 0.5 mm (0.013 to 0.020”). The typical SMT board is produced on an epoxy glass, 6-8-layer substrate. BT resins are also used for substrate for COB applications using thermosonic gold wire bonding because of its high Tg, good stiffness at temperature and low moisture absorption.

Advanced, commercial volume designs are utilizing fine pitch components down to 0.25 mm (0.010”) on epoxy resin/woven glass 10 layer structures, with controlled impedance, 0.20 mm (0.008”) finished holes and line/spaces down to 0.10 mm (0.004”). Intel is delivering the Pentium II and III microprocessor in their Single Edge Contact (S.E.C.) Cartridge technology with direct chip attach processor core inside the high density interconnect module. Intel has a very large impact on PWB infrastructure. When Intel needs a particular technology they pay for the development. The promise of high volume has driven Shindo’s investment for the tape carrier package. Shinko has an Intel only Plastic Pin Grid Array factory for the Pentium package. Johnson-Matthey has also entered the PPGA market. Intel is using High Density Interconnect technology for the Pentium II and III Modules. Intel has Ibiden, Shinko and Johnson Matthey making these module packages. Intel is expected to next move to µPPGA technology and Direct Chip Attach for modules operating at speeds greater than 500 MHz on chip and greater than 100 MHz off chip. Intel is moving to the S.E.C. cartridge “plug-in” PWB daughter board technology to simplify the motherboard design and extend the applications for higher and higher microprocessor performance. The S.E.C. cartridge will hold MPU, cache SRAM’s, and power modulation and other components. The plastic ball grid array (PBGA) which has better electrical performance due to shorter line lengths with less inductance will also be used for Pentium II and III processors since the integration of “on board” cache memory on the processor chip eliminates the need for chip to chip interconnection. Many design issues today are a result of “mixed” technology, products that might have 0.25 mm (0.010”) fine pitch tape automated bond (TAB) packages (like the early mobile Pentium packages), through-hole parts, 1.27 mm pitch SMT parts and chip components. The surface finish material and thickness for each package style may be different for optimal assembly yields. Currently many P/I structures for consumer products are finished with bare copper protected with an organic surface protection (OSP) coating. Other P/I structures are solder coated by the printed board manufacturer. On both approaches, the screen printing of solder paste is used to attach the devices. For PQFP pitch at or below 0.40 mm (0.016”), alternate methods of attachment are being developed that may have different board finish requirements. The PBGA packages are much more forgiving for finish type down to at least 0.5mm pitch.

The use of SMT has had a significant impact on the hole size used for interconnect via holes. As the drilled size drops below 0.63 mm (0.025”) there is a decrease in the reliability of the finished hole (see IPC-TR-579) for severe environments. While good process control is needed to assure that smaller holes are reliable, currently holes are commonly drilled above 0.35 mm (0.0135”) in panel thickness up to about 2.0 mm (0.080”). The printed board (PB) thickness to drilled hole diameter aspect ratio should ideally be kept <5:1 with 3:1 an optimum value. However, with an office environment, these aspect ratio values can be much larger and in many cases are. The system designer should be aware of the full assembly process and end use of the product to assure that the hole
interconnect size will not cause a reliability problem. For an office environment the most severe environment the PB will ever see is the assembly process.

<table>
<thead>
<tr>
<th>Reg #</th>
<th>Thickness</th>
<th>Construction</th>
<th>% RC</th>
<th>DK</th>
<th>DK Tol.</th>
<th>DS</th>
<th>Z CTE</th>
<th>Thick Tol.</th>
<th>Chem</th>
<th>Measle</th>
<th>Avail.</th>
<th>Cost</th>
<th>Flat</th>
<th>Smooth</th>
<th>Drill</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR-4 01</td>
<td>0.07mm (0.003&quot;)</td>
<td>1080</td>
<td>60</td>
<td>4.25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 02</td>
<td>0.08mm (0.003&quot;)</td>
<td>2x106</td>
<td>64</td>
<td>4.15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 03</td>
<td>0.11mm (0.004&quot;)</td>
<td>2x106</td>
<td>72</td>
<td>4.10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 04</td>
<td>0.11mm (0.004&quot;)</td>
<td>2113</td>
<td>57</td>
<td>4.30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 05</td>
<td>0.14mm (0.005&quot;)</td>
<td>106/2113</td>
<td>56</td>
<td>4.30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 06</td>
<td>0.13mm (0.005&quot;)</td>
<td>2x1080</td>
<td>59</td>
<td>4.25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 07</td>
<td>0.13mm (0.005&quot;)</td>
<td>2116</td>
<td>53</td>
<td>4.40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 08</td>
<td>0.16mm (0.006&quot;)</td>
<td>106/2116</td>
<td>51</td>
<td>4.45</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 09</td>
<td>0.16mm (0.006&quot;)</td>
<td>1080/2113</td>
<td>54</td>
<td>4.40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 10</td>
<td>0.18mm (0.007&quot;)</td>
<td>2x2113</td>
<td>50</td>
<td>4.50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 11</td>
<td>0.18mm (0.007&quot;)</td>
<td>7628</td>
<td>40</td>
<td>4.75</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 12</td>
<td>0.21mm (0.008&quot;)</td>
<td>2113/2116</td>
<td>50</td>
<td>4.50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 13</td>
<td>0.21mm (0.008&quot;)</td>
<td>2x2116</td>
<td>47</td>
<td>4.55</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 14</td>
<td>0.25mm (0.010&quot;)</td>
<td>2x2116</td>
<td>52</td>
<td>4.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 15</td>
<td>0.26mm (0.010&quot;)</td>
<td>7628/1080</td>
<td>47</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 16</td>
<td>0.26mm (0.010&quot;)</td>
<td>2x1080/2116</td>
<td>55</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 17</td>
<td>0.31mm (0.012&quot;)</td>
<td>2x1080/7628</td>
<td>47</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 18</td>
<td>0.32mm (0.012&quot;)</td>
<td>7628/2116</td>
<td>47</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 19</td>
<td>0.37mm (0.014&quot;)</td>
<td>2x7628</td>
<td>41</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 20</td>
<td>0.37mm (0.014&quot;)</td>
<td>2x2113/7628</td>
<td>46</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 21</td>
<td>0.43mm (0.016&quot;)</td>
<td>2x2116/7628</td>
<td>48</td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 22</td>
<td>0.43mm (0.016&quot;)</td>
<td>2x7628/1080</td>
<td>43</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 23</td>
<td>0.48mm (0.018&quot;)</td>
<td>2x7628/2116</td>
<td>43</td>
<td>4.8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 24</td>
<td>0.51mm (0.021&quot;)</td>
<td>2x1080/2x7628</td>
<td>46</td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 25</td>
<td>0.53mm (0.021&quot;)</td>
<td>3x7628</td>
<td>40</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 26</td>
<td>0.64mm (0.024&quot;)</td>
<td>2x2116/2x7628</td>
<td>47</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 27</td>
<td>0.64mm (0.024&quot;)</td>
<td>3x7628/1080</td>
<td>42</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 28</td>
<td>0.74mm (0.028&quot;)</td>
<td>4x7628</td>
<td>41</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 29</td>
<td>0.74mm (0.028&quot;)</td>
<td>2x2113/3x7628</td>
<td>44</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 30</td>
<td>0.75mm (0.028&quot;)</td>
<td>4x7628/1080</td>
<td>42</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 31</td>
<td>1.52mm (0.059&quot;)</td>
<td>8x7628</td>
<td>42</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 5-4**
FR-4 Copper Clad Laminate Construction Selection Guide

### 5.2 High Density Interconnect Structure Technology

*Happy Holden of Techlead Corp. has supplied much of the technical information in this section.*

The demand to interconnect higher lead count devices at a reasonable cost has spurred the development of High Density Interconnect PWBs. The drivers are PWBs as "Chip-to-Package" interconnects (PBGA, TBGA, CSP, and Micro BGA) such as the Intel packaging efforts, high trace density (5-6 lines/channel), via pitch (0.5 mm or smaller), and micro-vias as the "enabler" for flip chip/chip scale attach. Printed Board market economics dictate that
High lead count VLSI will not drive up PWB cost except in specialized segments such as mobile computing with 8 layer fine pitch ultrathin PWBs for form factor PCMCIA cards.

**High Density Interconnect Structures (HDIS)** - The basic HDIS structure is usually a standard laminated PWB with two or more laminated layers making up the core PWB. Sequential layers are added using microvia technologies, which allow the use of very small lands. The land size is the key factor in allowing more lines to be run between vias. The next few tables and figures show the difference in tracks per channel (wiring density) achieved with standard SMT laminated PWBs versus HDIS structures.

The printed circuit design rules (trace width & spacing, annular ring, pad size, etc.) associated with a particular number of tracks per channel is determined by the channel width (via spacing), track width and track spacing. For example, each of the following designs is a 1-track design. The difference is that each has a different track width.

![HDIS Diagrams](image)

The trace width, spacing and associated design rules can only be determined after the channel width has been defined.

The tables below cover various channel widths, pad diameters and trace/spacing widths. The table shows the number of tracks for a particular channel width. You can interpolate for pad diameters and trace/space widths not listed. If you are using a gridless CAD system, then the fraction of a track is useable. If you are using a gridded CAD system, you must round down to the closest whole number. The tables were built for a gridded CAD system so only whole number of line are shown.

**SMT Design (PBGA)** - Track vs. trace width for a channel width of 1.5 mm

<table>
<thead>
<tr>
<th>Tracks</th>
<th>Trace Width</th>
<th>Pad Diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>150 micron</td>
<td>400 micron</td>
</tr>
<tr>
<td>4</td>
<td>125 micron</td>
<td>350 micron</td>
</tr>
<tr>
<td>5</td>
<td>100 micron</td>
<td>350 micron</td>
</tr>
</tbody>
</table>
NOTE: In general the use of 75 micron lines has been limited due to the number of suppliers capable of high yields on large panels. A few US and a number of Japanese suppliers are capable. The latest US Industry Data Base for conductor yield from Conductor Analysis Technology shows yields for all tested US companies are below 90% for conductor/spacing width below 125 micron or 4.5 mils when tested over a full 18X24 panel. Large panels showed yields less than 40% for 75-micron lines and spaces.

SMT Design (PQFP, PBGA, and CSP): Track vs. trace width for a channel width of 1.25 mm

<table>
<thead>
<tr>
<th>LAND DIAMETER or WIDTH (microns)</th>
<th>500</th>
<th>400</th>
<th>350</th>
<th>300</th>
<th>250</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace/Spacing Width (micron)</td>
<td>200</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>150</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>6</td>
<td>6</td>
<td>7</td>
<td>7</td>
<td>7</td>
</tr>
</tbody>
</table>

A 1.25 mm channel width is today’s SMT standard. SMT lands are typically 500 to 550 microns for through vias using drill sizes of 300 to 350 microns. For 125 micron lines and spaces the number of lines is no greater than 2. This is a wiring density of 16 cm per sq. cm.

HDIS technology with smaller microvias and smaller lands are the key to increased wiring density. The land must decrease to 350 microns in diameter to achieve 3 lines per channel with 125-micron lines (24 cm per sq. cm) and 4 lines per channel with 100-micron lines (32 cm per sq. cm.). This is double the normal SMT wiring density. The key enabler for HDIS technology is smaller blind vias.
SMT (FP-QFP, PBGA, and CSP): Track vs. Trace width, for a channel width of 1.0mm

<table>
<thead>
<tr>
<th>Trace/Spacing Width (micron)</th>
<th>500</th>
<th>400</th>
<th>350</th>
<th>300</th>
<th>250</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>150</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>125</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>100</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>75</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

Decreasing the channel width to 1.25 mm to 1.0 mm has decreased the number of lines per channel for 100-micron lines and spaces and 350 micron lands from 4 to 2. The wiring density has dropped from 32 cm per sq. cm. (4 lines per 1.25 mm = 32 lines per cm) to 20 cm per sq. cm (2 lines per 1.0 mm = 20 lines per cm). It does not help to decrease the land diameter to 300 micron since the lines per channel have not increased. The land diameter must decrease to 250 microns to get an increase in the wiring density. A tradeoff must be made when selecting a 75-micron line and taking a potential processing yield loss or using a 250-micron land and going to a smaller microvia. The yield tradeoff has to be evaluated by the fabricator and designer. It is important to recognize that while the wiring density has decreased the via density has increased greatly from 64 vias per sq. cm at a channel width of 1.25 mm to 100 vias per sq. cm at a channel width of 1.0 mm.

Example: Track vs. Trace width, for a channel width of 0.75-mm width

1 track translates to a 150 micron trace width for 300 micron land dia.

2 track translates to a 100 micron trace width for 250 micron land dia.

3 tracks is not available
### CHANNEL WIDTH OF 0.75 MM - NUMBER OF TRACKS ROUTABLE:

<table>
<thead>
<tr>
<th>LAND DIAMETER or WIDTH (microns)</th>
<th>500</th>
<th>400</th>
<th>350</th>
<th>300</th>
<th>250</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace/Spacing Width (micron)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>150 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>125 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>100 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>75 1 2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

Decreasing the channel width from 1.25 mm to 0.75 mm has changed the lines per channel from 4 to 1 for a 100-micron line and a 350-micron land. This again is a change in wiring density for the 1.25 mm channel width from 32 cm/sq. cm. to 1 line per 0.75 mm (1 line per 0.75 mm = 13 cm/sq. cm). By using a 75-micron line and a 350-micron land the wiring density is 26-cm/sq. cm. (2 lines per 0.75 mm). As in the previous, the via density has increased from 64 vias per sq. cm to 169 vias per sq. cm. Both wiring density and via density are important for routing.

Example: Track vs. Trace width, for a channel width of 0.50-mm width

![Diagram of track vs. trace width]

2 tracks is not available

1 track translates to a 75 micron trace width for 250 micron land dia.

### CHANNEL WIDTH OF 0.5 MM - NUMBER OF TRACKS ROUTABLE:

<table>
<thead>
<tr>
<th>LAND DIAMETER or WIDTH (microns)</th>
<th>500</th>
<th>400</th>
<th>350</th>
<th>300</th>
<th>250</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace/Spacing Width (micron)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>150 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>125 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>100 N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
</tr>
<tr>
<td>75 1 1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Definition for Microvia - Microvias are blind via plated-through holes that are \( \leq 150 \mu m (0.006\ in. ) \). Microvias can be grouped into three fabrication methodologies. The three groups are:

- **A** create hole; then make conductive
- **B** create conductive via; then add dielectric
- **C** create conductive via and dielectric simultaneously
The hole could be any shape, including straight wall, positive or negative taper, or cup. The following techniques are being used for producing microvias:

**Today’s Microvia Technology (courtesy Happy Holden of Techlead Corp.)**

<table>
<thead>
<tr>
<th>Hole Formation Method</th>
<th>Via size</th>
<th>Pad size</th>
<th>Via Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanically drilled [A]</td>
<td>200-300 µm</td>
<td>500-600 µm</td>
<td>Sequential</td>
</tr>
<tr>
<td>Mechanically punched [A]</td>
<td>100-200 µm</td>
<td></td>
<td>Sequential/Sp. Tooling</td>
</tr>
<tr>
<td>Laser trepanning [A]</td>
<td>75-125 µm</td>
<td>200-300 µm</td>
<td>Sequential/Sp. Tooling</td>
</tr>
<tr>
<td>Photo formed [A]</td>
<td>100 µm</td>
<td>300 µm</td>
<td>Parallel</td>
</tr>
<tr>
<td>Wet etched [A]</td>
<td>No Applications</td>
<td>No Applications</td>
<td>Parallel</td>
</tr>
<tr>
<td>Dry etched (plasma) [A]</td>
<td>150 µm</td>
<td>300 µm</td>
<td>Parallel</td>
</tr>
<tr>
<td>Abrasive blast [A]</td>
<td>No Applications</td>
<td>No Applications</td>
<td>Sequential</td>
</tr>
<tr>
<td>Post pierced [B]</td>
<td>No Applications</td>
<td>No Applications</td>
<td>Sequential</td>
</tr>
<tr>
<td>Insulation displacement [B]</td>
<td>200 µm</td>
<td>300 µm</td>
<td>Parallel</td>
</tr>
<tr>
<td>Conductive bonding sheets [C]</td>
<td>25µm</td>
<td>200 µm</td>
<td>Parallel</td>
</tr>
</tbody>
</table>

**Advanced Technology Examples for Microvias** - Brian Swiggett of Prismatic at the Dec. 1996 TMRC indicated that over thirty different built up multilayer constructions and material sets have been referenced and many developments have not been published. A list of microvia processes in production is listed in the table below.

### MICROVIAS IN PRODUCTION

<table>
<thead>
<tr>
<th>Company</th>
<th>IBM &amp; Licensees</th>
<th>JVC</th>
<th>Hitachi</th>
<th>Ibiden</th>
<th>Toshiba</th>
<th>NEC</th>
<th>Dyconex</th>
<th>Matsushita</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>SLC</td>
<td>VJ2</td>
<td>Hitavia</td>
<td>IBSS</td>
<td>B²IT</td>
<td>DV Multi</td>
<td>Dycostate</td>
<td>ALIVH</td>
</tr>
<tr>
<td>Line Width, (µm)</td>
<td>75/50</td>
<td>10/95</td>
<td>100</td>
<td>75/50</td>
<td>90</td>
<td>80/50</td>
<td>100</td>
<td>60</td>
</tr>
<tr>
<td>Line Space, (µm)</td>
<td>75/50</td>
<td>100/75</td>
<td>100</td>
<td>75/50</td>
<td>90</td>
<td>80/50</td>
<td>125</td>
<td>90</td>
</tr>
<tr>
<td>Via Dia. (µm)</td>
<td>125/90</td>
<td>200/100</td>
<td>200</td>
<td>150/100</td>
<td>200</td>
<td>100</td>
<td>75</td>
<td>150</td>
</tr>
<tr>
<td>Land Dia. (µm)</td>
<td>250/165</td>
<td>-</td>
<td>500</td>
<td>250/150</td>
<td>300</td>
<td>250</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Layers/Side</td>
<td>½</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Total Layers</td>
<td>8/10</td>
<td>4/6</td>
<td>4/6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>10</td>
<td>8</td>
</tr>
</tbody>
</table>

According to Swiggett the principal differences between the various HDI technologies center on:

- Built up dielectric layer material and application method (liquid, film, etc.)
- Via hole formation (laser, photo, plasma)
- Metallization (coated foil, electroless foil, sputtering, and conductive paste)

Minimum Design Rules for HDIS Today - (Happy Holden of Techlead Corp.)
Process Flows for Four Microvia Technologies - The process flows for the major HDI process approaches are shown below:

Laser Vias
Laser Drill is a single or multiple via generation technology that replaces existing mechanical drilling process in certain designs with a laser drilling process. Laser drilling differs from mechanical drilling in that the focused beam used to create the holes can produce smaller holes that those produced by conventional drilling. These lasers are generally categorized by the wavelength of light they use. It can be used to create both blind vias and holes. The process follows standard multilayer manufacturing and is compatible with most materials. Lasers are capable of smaller features and uses standard plating technology. In the majority of cases, laser drilling produces blind or through vias one at a time. There are processes for multiple laser via generation.

The four technologies represented below are just a few of those published in literature and being developed today. These are the most mature of the HDIS technologies employing lasers to produce microvias. Finstrate, developed in 1982 employed laser drilled microvias in a PTFE multilayer dielectric. Microwiring, a development process from Germany, has employed lasers in production since 1987.

Four typical constructions that employ lasers for via generation

Wet/Dry Process Formed Vias
Microvias can be formed by various etching techniques. The most common etching technique is to use microwave-gas plasma. This is the dry etching process. Wet etching by hot KOH has been used historically for polyimide films. Because of the chemical effects, these formation techniques are isotropic, that is they etch inward while they etch down. On the positive side, these formation techniques are mass via generation in that they form all vias at the same time without regard to number or diameter.
Sequential Bonded Film (DYCOstrate)

Sheet Build Up (micro-drilled)

Roll Sheet Build Up (chem. etched)

Four typical constructions that use a wet or dry etch to generate vias

Photodielectric Vias

The figure below describes a single layer dielectric coated over a core substrate with plated and/or plugged through holes. Microvias are formed by photoimaging. Layer Photovia Additive Copper describes a single layer dielectric with microvias formed by photoimaging. A first via layer of dielectric is coated over the base substrate. The microvias are imaged and developed. This via layer is then cured, adhesion promoted and treated with a catalyst receptor. A second circuit layer of dielectric then coated. The circuit pattern is then imaged and developed. The circuit layer is then catalyzed and cured. Either Full Build Electroless Copper is then used to plate both the microvias and circuit pattern or conductive paste is used to fill the microvias and circuit pattern.

First used in 1990, the photoimageable dielectric was a modified solder mask. Today, modern photoimageable dielectrics (PID) are optimized as a dielectric in either liquid or dry film, positive acting or negative acting.

Photo-via Redistribution Layer

Interpenetrating polymer Built-Up Structure System

Carrier Formed Circuits

Surface Laminar Circuits (SLC)

Four commercially produced PID structures
Conductive inks / Insulation Displacement

The figure below describes conductive inks through a single layer dielectric with microvias formed by photoimaging, laser or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished by either laminating copper foil onto the dielectric surface or by chemical deposition.

Four new HDIS structures that employ conductive pastes as vias

**HDIS Structure Description** - The IPC has set the structure for high-density interconnections. Type I, Type II and Type III are new product definitions to identify different type of constructions using sequential layers with microvias. The types are as follows:

- **TYPE I** \( 1 \, [C] \, 0 \) or \( 1 \, [C] \, 1 \) (a structure with one sequential layer on one or both sides)
- **TYPE II** \( \geq 2 \, [C] \, \geq 0 \) (a structure with 2 or more sequential layers on one or both sides)
- **TYPE III** \( P \, \geq \, 0 \) (where \( P \) is a passive “substrate with no electrical connecting functions”).

The core is identified as an A, B, or C type core.

- [CA] is a core with internal vias only; redistribution layers make contact to the surface.
- [CB] is core with internal and external (through microvia structures). High-density interconnecting structures make contact into the innerlayers of the core. [CC] is a passive core with no interconnections.

A new Type classification is being considered by the IPC for structures that do not require a core. The colaminated layer pair structures that use conductive pastes for the electrical connection between layer pairs would have a new code for four layers (two layer pairs) such as:

\[
2 \, [X] \, 2
\]

where \( X \geq 2 \)

\( X \) represents a coreless microvia board

The table below lists eight constructions using conductive paste and colaminated layer pairs similar to the previous figure.
Testing HDIS Structures. - According to Dieter Bergman of the IPC the one missing element is a new methodology for bare board electrical testing. As the surface topology of these microstructures gets smaller, it becomes more difficult to use existing probe point methods to ensure that the interconnecting products electrically sound (no opens or shorts). The typical electrical test bed of nails has a probe grid of 2.5-mm (100 mils). This limits the probe density for long pin fixtures to about 200 pins at any location. New array components will require much higher probe densities than this. The table below shows the 1:1 probe density requirements for various array packages.

<table>
<thead>
<tr>
<th>Array Pitch, mm</th>
<th>Probe Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>256</td>
</tr>
<tr>
<td>1.25</td>
<td>400</td>
</tr>
<tr>
<td>1.0</td>
<td>625</td>
</tr>
<tr>
<td>0.5</td>
<td>2500</td>
</tr>
</tbody>
</table>

A probe field using 1.25 mm centers is the most dense presently available. This density will be completely inadequate for bare board electrical test to support the new HDIS components.

The electrical test technology for P/I structures is driven by the semiconductor package. The general technology trends for packages from the SIA 1996 Roadmap is shown below.

### General Semiconductor Technology Trends

<table>
<thead>
<tr>
<th>Chip Level</th>
<th>1999-2001</th>
<th>2002-2004</th>
<th>2005</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature Size, nm</td>
<td>180</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>Performance (MHz)- off-chip</td>
<td>25-479</td>
<td>60-884</td>
<td>60-1037</td>
</tr>
<tr>
<td>Performance (MHz)- on-chip</td>
<td>25-958</td>
<td>60-1570</td>
<td>60-2075</td>
</tr>
<tr>
<td>Package Pin Count</td>
<td>40-2007</td>
<td>40-2820</td>
<td>40-3158</td>
</tr>
</tbody>
</table>

Source-SIA Roadmap, 6/99 (Draft)
This pin count projection is driving work being done at ITRI to develop electrical test methods to meet the future P/I structure needs of the industry. This projection is shown below.

### ITRI E-Test Project Parameters Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CONV LE SA</td>
<td>CONV LE SA</td>
<td>CONV LE SA</td>
</tr>
<tr>
<td>Global Test Point Density per cm²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Printed Board</td>
<td>&lt;16 &lt;25 &lt;30</td>
<td>&lt;25 30 40</td>
<td>30 40 45</td>
</tr>
<tr>
<td>HDIS Board</td>
<td>20 28 45</td>
<td>30 &lt;45 &gt;75</td>
<td>&lt;45 &gt;75 &lt;150</td>
</tr>
<tr>
<td>Organic Chip Carrier</td>
<td>30 75 150</td>
<td>75 150 &lt;500</td>
<td>150 225 &gt;500</td>
</tr>
<tr>
<td>Impedance %Test Accuracy</td>
<td>±15 ±10 ±10</td>
<td>±15 ±10 ±5</td>
<td>±15 ±1 ±5</td>
</tr>
<tr>
<td>Test Voltage</td>
<td>40 40 100</td>
<td>80 100 250</td>
<td>100 250 250</td>
</tr>
<tr>
<td>Short Threshold Value, ohms</td>
<td>100K 1K 2M</td>
<td>1M 2M 10M</td>
<td>2M 10M 10M</td>
</tr>
<tr>
<td>Open Threshold Value, ohms</td>
<td>100 100 20</td>
<td>50 20 10</td>
<td>15 10 5</td>
</tr>
<tr>
<td>Integral Resistors</td>
<td>None 100-1MΩ ±10%</td>
<td>100-1MΩ ±10%</td>
<td>100-1MΩ ±10%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The density for Universal Test Fixtures (UTF) is shown in the next Table. The typical UTF used in PWB construction today is on .54 mm grid with less than 10% of the available fixtures on 1.25 mm grid.

### FP-QFP, BGA, Flip Chip Vs. Universal Grid Testers’ Density Today

<table>
<thead>
<tr>
<th>Pitch, mm</th>
<th>Probe density per cm²</th>
<th>Relative Density</th>
<th>Existing Testers' %</th>
</tr>
</thead>
<tbody>
<tr>
<td>_single density grid (std)</td>
<td>2.54</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>Double density grid</td>
<td>1.78</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>Fourth density grid</td>
<td>1.25</td>
<td>64</td>
<td>4</td>
</tr>
<tr>
<td>1.5 mm pitch BGA</td>
<td>1.5</td>
<td>45</td>
<td>2.8</td>
</tr>
<tr>
<td>1.0 mm pitch BGA</td>
<td>1.0</td>
<td>100</td>
<td>6.2</td>
</tr>
<tr>
<td>0.635 mm pitch BGA</td>
<td>0.635</td>
<td>256</td>
<td>16</td>
</tr>
<tr>
<td>0.3 mm pitch Flip pitch</td>
<td>0.3</td>
<td>1111</td>
<td>69.4</td>
</tr>
<tr>
<td>0.225 mm pitch Flip Chip</td>
<td>0.225</td>
<td>1975</td>
<td>123.5</td>
</tr>
</tbody>
</table>

It is obvious that the densities of current Universal Test Grid fixtures are not compatible with the coming test requirements. The existing test methods to solve the electrical test dilemma are listed below.

1. Double Density, quad density grid
2. Flying probe, flying grid
3. Translators, membranes
4. Conductive rubber, capacitance coupling
5. Step and repeat buckling beam machines

At this time there are no cost effective electrical test solutions.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CONV</td>
<td>LE</td>
<td>SA</td>
</tr>
<tr>
<td>Global test point density per cm²</td>
<td>&lt;16</td>
<td>&lt;25</td>
<td>&lt;30</td>
</tr>
<tr>
<td>Printed board</td>
<td>20</td>
<td>28</td>
<td>45</td>
</tr>
<tr>
<td>HDI board</td>
<td>30</td>
<td>75</td>
<td>150</td>
</tr>
<tr>
<td>Organic chip carrier</td>
<td>±15%</td>
<td>±10%</td>
<td>±10%</td>
</tr>
<tr>
<td>Impedance % Test Accuracy</td>
<td>±15%</td>
<td>±10%</td>
<td>±10%</td>
</tr>
<tr>
<td>Test Voltage*</td>
<td>40</td>
<td>40</td>
<td>100</td>
</tr>
<tr>
<td>Short threshold value (ohms)</td>
<td>100K</td>
<td>100K</td>
<td>2M</td>
</tr>
<tr>
<td>Open threshold value (ohms)</td>
<td>100</td>
<td>100</td>
<td>20</td>
</tr>
<tr>
<td>Integral Resistors**</td>
<td>none</td>
<td>100-1MΩ±10%</td>
<td>100-1MΩ±10%</td>
</tr>
</tbody>
</table>

5.3 Military P/I Structures

Military hardware will be different in the future. Many systems can use commercial printed boards. However, some current military P/I structures still differ significantly from commercial P/I structures in that most devices must be in hermetic packages and the system must operate over a wide temperature range (typically from -65°C to +125°C) to meet the end product reliability requirement. The military is beginning to procure systems using plastic rather than ceramic packages in order to reduce cost. The military is still concerned about the lack of hermeticity with plastic devices. A significant amount of effort is going into developing reliability information for non-hermetic packages (Reliability without Hermeticity-RWOH). It is well known that plastic encapsulated packages perform as well as ceramic packages in many applications but little is known about severe environmental applications. The military is very concerned that weaponry can be stored for 15-20 years in all types of environmental extremes and still function without fail. Most systems fall into categories similar to Types 1 and 2 of Figure 2-3. The predominant interconnection approach involves single-chip packages mounted on multilayer-printed boards or discrete wire boards mounted on a motherboard by way of a connector. Weight and volume are key issues. Military/Aerospace products are expected (required) to work the first time and every time, in potentially life threatening environments. As providers of this hardware, the fabricator is responsible to assure product conformance over the entire life cycle requirements.
The requirement for hermeticity in military packaging means the device packages are all inorganic (ceramic, glass or metal) with both leaded and leadless formats used. Leadless ceramic packages are more available at a lower cost and easier to assemble than ceramic leaded packages due to lead planarity problems. However, the leadless packages create a special set of problems related to the mismatch of CTE between the ceramic package and the printed board. Various constraining laminate materials can solve the CTE mismatch problem and metal substrates to decrease the substrate to device package CTE to match solder joint life requirements. However, the printed board is much more expensive.

Both organic and inorganic materials are used in military P/I structures. Leadless ceramic parts can be used on organic printed boards much as they are being used in commercial products. The preferred lead shape for ceramic leaded parts with Kovar leads is the “gullwing”. The organic printed board creates a special problem when using leadless ceramic chip carriers (LCC). The LCC package and the organic P/I structure have a large mismatch in coefficient of thermal expansion (CTE). For solder joints to survive even 100 thermal cycles, the CTE of the P/I structure must be decreased to within +/- 2 PPM/°C of the LCC. This means that the composite structure should have a CTE in the 5 to 9 PPM/°C range in order to decrease the stress in the solder joint.

Various methods are used to decrease the CTE of organic printed boards. A few are listed below:
1. Multilayer printed boards bonded to both sides of a low CTE metal core such as copper-Invar-copper, copper-nickel-(carbon)-copper, copper-nickel-molybdenum-copper, silicon carbide/aluminum, Be/BeO and others.
2. Thin layers of a constraining material (typically 0.15 to 0.2-mm thick copper Invar copper) can be used in place of the normal ground and voltage planes. The total constraint with this approach is less than the metal core approach but it works well for smaller LCCs (nominal 12.5 mm package dimension) and for leaded ceramic packages.
3. Constrained core and foil thermal expansion has several manufacturing issues. First, CIC foil constructions require a higher level of manufacturing competence and radial barrel cracking will typically occur with polyimide unless custom caulk fill material is used in CIC clearances. Also, mixed expansion rate/dimensional stability materials require reproducible artwork scaling factors, CIC foils pose special lamination integrity risks (surface treatments). The CIC foil treatment to plating interfaces requires special chemistries. Plating voids are a problem with thick CIC foils and the vendor process used must demonstrate there are no voids. Also, high shear forces at the interface between polyimide MLBs and the constraining materials cause laminate cracking. If a potential vendor says ‘no problem’ to building polyimide with CIC constraining foils, you may want to look elsewhere.
4. Controlled thermal expansion core module bond integrity- Because of the stress induced by mixing materials with different expansion rates in a module, it is important to have assurance that bond integrity will remain
through assembly and the life cycle requirements of the system. The experience that your vendor has with processing constraining core and foil materials is very important. The vendor should use a quantifiable measure of bond integrity (prior to your assembly).

5. A reinforcing dielectric fiber material, which has a low CTE, such as Kevlar or quartz fiber, can also be used. The composite CTE of the printed board can be made in the 7-8.5 PPM/°C range. However, both Kevlar and quartz fibers have a relatively low modulus of elasticity; therefore, the CTE of the multilayer printed board is very sensitive to the number and thickness of internal copper voltage planes. Woven aramid fibers have a problem related to the high radial CTE of the fiber. During thermal cycling, the large CTE between the fiber and the resin will cause the resin to crack at the fiber knuckles. Studies have shown a minimal effect on the insulation resistance of the P/I structure, but it is not a desirable attribute. Tougher resins (more flexible) can nearly eliminate this problem. Complete elimination of the resin cracking has been accomplished with non-woven aramid fibers in tape or random matte form. Tough resins are preferable with this construction also since the fiber still has a high radial CTE. Like other military products, heat is removed by bonding the PWB to a thermally conducting metallic substrate. A high CTE substrate like aluminum will tend to increase the CTE of the module unless it is mechanically decoupled from the printed board with a thermally conducting, flexible material (elastomer). Even with a flexible bonding material the CTE of the assembly can be expected to increase approximately 2 PPM/°C at low temperatures due to coupling with the substrate. Lower CTE aluminum alloys like aluminum beryllium alloy (AlBe) with CTEs in the 12 PPM/°C have been substituted for aluminum to eliminate this problem but at a considerable increase in cost.

With all types of organic printed board construction, reliability of small plated through holes is a critical issue. Small PTHs are those that are drilled at 0.5 mm (.020 inch) or less. The length to diameter ratio of the PTH should be kept below 3 to 1 or 4 to 1 if the small vias are to be reliable in a severe thermal cycling environment. The printed board should also be as thin as possible.

All organic dielectrics are poor heat conductors. Since heat removal for military P/I structures occurs by conduction through the printed board and into the heat removal substrate, ways must be found to decrease the temperature difference between the device package and substrate. The most common technique is the use of thermal vias in the printed board. However, since these vias use valuable routing space and are not usually part of the electronic circuit, available routing area for the printed board decreases. Discrete wiring board technology with its higher wiring density per layer is less affected by the routing space lost by thermal vias.

A ceramic multilayer substrate minimizes the CTE mismatch problem with LCCs and the low thermal conductivity problem with organic printed boards. The ceramic P/I structure introduces some unique problems of its own. The P/I structure, which uses a co-fired ceramic substrate with thick or thin film metallization using fused glass dielectrics, represents the most widely used approach. The ceramic P/I structure is brittle and must be handled carefully. Constructions of this type are usually limited to sizes less than 15x15 mm. Larger structures are available but cost goes up sharply.

The high dielectric constant of ceramic materials places greater challenges to designs where impedance control is required. For example, the ceramic P/I structure may be designed in microstrip geometry’s to increase impedance to reasonable values. The challenges in obtaining impedance control in multi-level microstrip designs is significant, but since this technology features a high wiring density, a two signal layer approach is often adequate. Thus, the electrical design limitation has not been a severe problem.

Ceramic P/I structures has about 20X the thermal conductivity of organic P/I structures. This property allows good heat spreading through the ceramic P/I structure to the aluminum substrate from the semiconductor package. The typical electronic module using ceramic P/I structures is normally soft bonded to an aluminum thermal substrate in a single sided or double-sided construction format. Unlike the organic PWB structures, the ceramic PWB has a very high modulus and the module CTE is not affected by the aluminum heat sink.

Most small, low power LCC packages can be effectively cooled through the peripheral solder joints. However, the thermal resistance from semiconductor junction to thermal substrate is much larger for high power packages causing the need for heat sinks to be attached to the package. Thermal pads on the LCC package can be soldered to matching lands on the ceramic P/I structure to decrease the thermal resistance to acceptable values.
Both leaded and leadless hermetic ceramic semiconductor packages are used in military P/I structures. The preferred lead shape is the “gullwing”, since the profile height can be kept low. Lead pitches of 1.25 mm (0.050 inch) and 1.0 mm (0.040 inch) are standard and the dimensional tolerance standards are adequate. High pin count packages of 0.63 mm (0.025 inch); 0.5 mm (0.020 inch), 0.4 mm (0.016 inch), and 0.3-mm (0.0125-inch) pitch are being used. Lead pitch tolerances are poor on all the fine pitch packages. Tight standards are definitely needed for these device packages to be put into production. Leadless ceramic packages are being used in 1.25 mm (0.050”) pitch up to 84 leads and 0.63 mm (0.025 inch) pitch up to 164 leads. Larger package sizes have two problems.

1. Solder joint reliability for large leadless packages has not been demonstrated over the full Mil-Spec temperature cycle. Adequate data and reliability predictive methods are now available so reliability can be predicted based on package size, solder joint height and test environment.

2. Lead-to-lead and land pattern tolerance build up can create an assembly problem. Tighter tolerances are required to achieve the desired lead/land overlap required for reflow soldering and to prevent solder bridging or electrical cross talk to adjacent lands.
Section 6
Assembly Technology

The surface mount assembly processes have, for the most part, stabilized. Changes occurring in the past year can be classified as enhancements to existing technology. Some enhancements, such as the emergence of CSP’s and flip chips require additional development and refinement, but for the most part existing placement equipment can handle these devices. Suppliers continue to focus on equipment performance and reliability. Cost is a major factor; this in turn drives improvements in cycle time, for example faster placement rates. This continues the push to improve productivity and process capability.

Careful handling of the product during assembly is critical. A disorderly and uncontrolled factory environment is undesirable for building surface mount assemblies (or any other product). Environmentally controlled facilities or equipment may be required if an adequate process capability is to be achieved. For example, temperature and humidity control will enhance solder paste performance.

Material handling issues must also be addressed when manufacturing surface mount assemblies. As PCB density and component complexity increases, the physical handling of assemblies between processes becomes more critical. Improper handling can induce quality and reliability problems, such as mislocated, missing or broken components. Operator handling of assemblies during processing should be kept to a minimum and allowed only with proper tooling and procedures.

A continuous flow assembly process is the best assembly technique available, whether the operation is high volume and low mix, low volume and high mix, or somewhere in between. Processing assemblies quickly with automatic handling between processes and with minimum inventory will assure that all processing variables are kept to a minimum. If a continuous flow operation is not possible, it may be necessary to provide a stable environment for the transportation of work-in-process (WIP). With this concept, the inventory from each process step is contained in its own enclosure. These enclosures are then moved through the factory to each required process.

Today, companies have the choice of investing in captive manufacturing operations, using a contract manufacturing service, or a combination of both. There are complex issues that need to be addressed in either case. Section 2 discusses some of these issues.

6.1 Attachment and Interconnect Materials

Surface Mount Adhesives

The purpose of surface mount adhesives is to hold surface mount components in place before and during wave or reflow soldering. The adhesive may also be required to provide other functions throughout the life of the assembly, such as thermal conductivity, certain dielectric properties, and chemical inertness.

Surface mount adhesives are detailed in IPC-SM-817 "General Requirements for Surface Mount Adhesives", which classifies adhesives by grade of cure: heat only, UV or visible light, and ambient cure. This document also describes test methods for determining viscosity, working life, shear strength, peel strength, spread/slump, chemical resistance and many other characteristics. These adhesives can be thermosetting or thermoplastic.

Adhesives are applied using one of three methods: dispensing, printing or pin transfer. During the adhesive application process the quantity of adhesive and location of the pattern are important process variables. Pattern misplacement and/or excessive adhesive will contaminate the solder paste and prevent good solder joint formation during reflow or wave soldering. Too little adhesive can allow components to move during assembly, prior to the
curing process, resulting in mislocated or missing components. Too little adhesive will also allow components to fall off during wave or reflow soldering. Surface condition is important; adhesives will not adhere to dirty, contaminated surfaces.

**Conductive Adhesives**

Commercially available conductive adhesives are classified into two categories: isotropic and anisotropic.

Isotropic conductive adhesive is a highly metal-filled (typically silver), polymer. To date the electrical conductivity of non-filled intrinsically conductive polymers are still inadequate for solder replacement applications. Metal-filled types, nominally 80% silver flakes by weight, have found some use in niche applications. This unique interconnection material is designed to mechanically attach to the component leads and substrate conducting pads through the adhesive property of the polymer whereas the conductivity of the joints is determined by the particular proximity of metal flakes after curing of the polymer. Such high metal loading considerably compromises the adhesive joint strength. To date, isotropic adhesive joints, particularly with larger packages with small bond areas, are found to be mechanically significantly weaker than solder joints. Unlike the self-aligning capability of solder, this type of material is characterized by its high surface tension, thereby demanding better placement accuracy. Also adhesive printing stencils must be thinner than solder stencils to assure that adhesive is removed from stencil openings and deposited on substrate.

Low temperature processing potential, lead-free formulations, and fewer process steps are positive attributes. Formulations are vulnerable to humid environments because of moisture uptake of the material and degradation of electrical properties occur over time. The reworkability of this type material is still less than satisfactory. Special solvents or excessive heat may be required while removing a component and replacing it.

In short, the commercial materials that have been evaluated do not produce mechanical and electrical joints equivalent to comparable solder joints including long term reliability testing. The CTE of polymers is generally substantially higher than metal; therefore, the conductivity excursion is rather high. The high cost of adhesives is also an issue.

Isotropic conductive adhesives have equal electrical conductivity in all directions, whereas anisotropic conductive adhesives are designed to be conductive only in Z-direction. This unidirectional material is such because metal loading is much below percolation threshold. The conductive particles are very small in size, around 5 – 10 microns, and require planarity of the mating pads. The joints made with this type of materials suffer from inherent instability with temperature stress. This material has been widely used the LCD industry. While the isotropic adhesives are available in paste form, anisotropic material is generally available in film form. The introduction of this unique interconnection materials- a composite unlike monolithic solder – is not going to be drop-in; instead it may demand addressing some infrastructure issues.

**Soldering Fluxes**

The objective of flux in electronic assembly is to remove surface contamination and oxidation from the solderable surfaces of the printed circuit board (attachment pads & holes) and component (leads, terminations, & bumps). Flux systems are generally broken down into two categories: flux chemistries that do not require cleaning of post solder residues and flux chemistries that do require cleaning of the post solder residues. Flux residue cleaning is generally broken down into solvent-based systems and aqueous based systems. Within the no clean category flux, systems are designed for nitrogen atmosphere processing only as well as for either nitrogen or air atmosphere processing.

The major advantage of fluxes that require cleaning is the increased activity of the flux compared to most no clean systems. The major disadvantages are the added cost of cleaning and the issues that surround the insurance that all
flux residues have been removed with the cleaning process. Additional environmental concerns can be raised with regards to the disposal of the cleaning solutions. Removing flux residue under small gaps such as chip resistors and capacitors can be difficult. Reliability issues can result if cleanable flux residues are not totally removed from these areas. Fluxes are described in ANSI/J-STD-004 “Requirements for Soldering Fluxes”. This standard provides test methods for determining the corrosive or conductive properties of the flux and flux residue.

Fluxes are divided into three basic classifications. Type “L” fluxes have a low activity level, type “M” fluxes have a moderate activity level, and type “H” fluxes have a high activity level. Their chemical constituents also further classify fluxes. They are listed as RO (rosin), RE (resin), OR (organic) or IN (inorganic).

The soldering of array packages with tacky fluxes and liquid fluxes is becoming more prevalent. Bare silicon and Chip Scale packages are generally assembled by either dipping the bumps into tacky flux or by applying liquid flux to the attachment pads. Chip Scale packages are also assembled using solder paste based processes. For Chip Scale Packages the bump to bump pitch generally determines if solder paste or flux only processes are to be used. Due to the low standoff distances between the substrate and the bottom of the package, cleaning of flux residue from under CSP’s is generally difficult. For this reason no-clean fluxes are generally used.

New epoxy based flux-underfills have been introduced within the last few years enabling the flip chip or package to be assembled and bonded with one material. These so-called “Flux Encapsulants” act as flux and underfill at the same time. Most of these materials still need a final curing cycle. The dispensing of these “Flux Encapsulants” can be integrated in the placement system so that an additional dispenser is not needed. Another advantage of the “Flux Encapsulants” is that no “wait time” is needed for flow of the material once dispensed onto the substrate.

**Solder Alloys**

There is pressure to reduce lead in the environment and it is being spearheaded by pending regulations in Asia and in Europe to eliminate lead from the electronics industry by 2002 and 2004 respectively. No drop-in lead solder replacements have been developed yet. Material research is proceeding in conductive adhesives, as explained earlier. However, most development activities are centered about no lead solder alloys. Approximately 13,500 metric tons of lead is consumed worldwide for electronic assembly, so the availability of a substitute element is important. Several studies were conducted for suitable tin alloys taking into account the melting range, elemental toxicity, cost, performance and elemental availability. Five elements make suitable alloys with Tin: Bismuth, Indium, Zinc, Copper, and Silver.

Copper and Silver tin alloys have reflow temperatures of 227 to 230 degrees C (versus 180 C for Lead Tin eutectic) with temperature peaks of 245 to 257 degrees C. This substantial increase in reflow temperatures requires process modifications like bake out, improved no clean fluxes because the higher temperatures will yield more oxides, and requalification of components for Jedec moisture tests. Higher temperature is actually required for some specific automotive components; however, they will use higher temperature ceramic substrates. The use of Silver can lead to potential silver migration and some leakage tests using the Toxicity Characteristic Leaching Procedure (TCLP) have demonstrated that tin-silver alloys come dangerously close to the 0.1 mg/l EPA limit in drinking water.

Traces of Bismuth, Zinc and Indium reduce the melting point, but these elements have other issues. Bismuth and Zinc oxidize readily thus requiring very active flux. Bismuth is a by-product of lead mining. Finally, Indium is a rare trace earth metal whose price and availability will become a problem.

In summary, there are no immediate drop-in replacements for lead as a solder alloy. Several efforts are under way with minute amounts of trace elements to reduce the reflow temperature and there will be widespread use of non-lead solder alloys but the question is when and will it be soon enough for some of the regulatory efforts in Asia and Europe.
Solder Paste

Solder paste contains solder particles of a specific size (1/4 to 1/5 of the screen or stencil aperture size is recommended) and shape (spherical is recommended), combined with flux to promote wetting and other additives to control viscosity, tackiness, slump, drying rate, etc. Two types of flux systems are available: those that require cleaning and those that do not. These fluxes produce residues that can be solvent cleaned (rosin systems), aqueous cleaned (water-soluble systems), or residues that require no cleaning (no-clean systems). Solder pastes are used to provide solder for lands on printed circuit boards or solder for the land/lead interface that forms the solder fillet. Solder paste application is the most difficult surface mount process to control.

Solder paste is described in ANSI/J-STD-005 "General Requirements and Test Methods for Electronic Grade Solder Paste" (formerly IPC-SP-819). IPC-SP-819 defined four types of paste categorized by the particle size in microns and its percentage composition. ANSI/J-STD-005 adds two finer particle sizes. Test methods are used to determine viscosity, slump, tackiness, wetting, and resistance to solder ball formation and shelf life.

The selection of two different solder paste alloys, one with a high melting temperature and one with a low melting temperature, can be used for double sided surface mount assembly. This step solder approach eliminates the need for adhesives, but increases the demands on the printing, reflow and hand soldering processes. However, most double sided assembly operators use the same solder alloy for both sides and rely on surface tension to hold the components in place on the bottom side. In most cases this is an acceptable approach.

Several companies have developed a process to "solder bump" certain areas on a PB; usually the ultra fine pitch land patterns. Solder paste is applied to the PB at the fabrication stage. The solder paste is then reflowed, forming the solder bump. The PB now contains sufficient solder to produce a solder joint. A flux paste is deposited on the land patterns during assembly. The components are placed in to the flux paste, which holds the components in place on the bumped solder land patterns. The PB is then reflowed, and the solder joints are formed.

Underfill Materials

Fast curing one-component epoxy underfill materials for SMT was first introduced about 15 years ago. Since that time, surface mount underfill application techniques and materials have seen significant improvements, driven by increased board assembly speed and refined material capabilities. High yields and product reliability are directly affected by the performance characteristics of surface mount underfills. The importance of underfill adhesive strength to die passivations, solder masks, and substrates cannot be overemphasized. These materials must have low mobile ionic content, very low alpha particle generation along with electrical, mechanical, chemical, and thermal stability. The industry is now providing “snap-cure” formulations that can provide very short curing times using thermal heat or microwave radiation.

Capillary flow underfills are used to securely anchor flip chip die, flip scale and BGA packages onto printed circuit substrates. These materials have the additional challenge of quickly wicking beneath the part into spaces with as little as a 25 to 40 micron dimensions. Material selection is critical since the underfill must address the thermal stresses caused by the thermal expansion mismatch of silicon die to that of the substrate. Spherical silica fillers, comprising up to 70 % of the underfill composition, are added to the adhesive resins as a means to achieve low thermal expansion coefficients. Flow modifiers and adhesion promoters among other additives provide a desired flexural modulus and specialized properties required for capillary flow underfills. Capillary flow underfill adhesives are control dispensed at the long axis edge of the SMT package along with a fillet pass. The underfill is cured following material dispense.

A more recent underfill classification is the “no-flow” underfill. These materials are not designed to wick beneath an SMT part, but rather are dispensed prior to part placement. As the part is placed into position on the substrate it displaces the attachment adhesive. A higher placement force is required to displace the underfill and insure good contact of part solder contacts to board site contacts. The “no-flow” underfill must provide sufficient fluxing.
of the solder attachment sites in addition to securely anchoring the part to the substrate upon cure. The thermal process after underfill dispense and part placement provides both solder reflow and adhesive curing.

An industry standards document, IPC J-STD-030, “Qualification and Performance of Underfill Materials for Flip Chip and Other Micro-Packages” is available. The purpose of this standard is to establish the evaluation criterion for identifying materials whose properties reduce thermo-mechanical stress thus enhancing the final assembly’s performance.

6.2 Assembly Equipment and Processes

Adhesive and Solder Paste Application

Dispensing and printing are the common methods used to apply adhesive and solder paste. Pin transfer can be used to apply adhesives, but this is not a common method. Dispensing and printing have evolved as the preferred methods for adhesive application.

Printing has evolved as the preferred method for solder paste application. Dispensing offers flexibility and printing offers a faster cycle time. Dispensing can be done on flat and irregular surfaces while printing requires a flat surface. Factors that affect the selection of an application process include the following: volume of material, volume control, process cycle time, land size and lead pitch (for example; dispensing solder paste on a 1206 land verses onto a fine pitch land), and quantity of product being produced. The time required to fabricate a stencil verses the time required to write a dispensing program should also be considered. Adhesive printing is becoming popular due to faster chip shooters making dispensers the bottleneck, development of new type of adhesives for stenciling, and introduction of new stencil technologies.

Dispensing is accomplished with equipment that ranges from simple hand held units to fully automatic dispensing systems. The dispensing equipment may be table mounted, stand alone, or in-line. Some placement systems have an integrated dispensing capability. Most automatic dispensing systems offer vision alignment. The material is usually dispensed from a 10cc syringe.

Printing systems are available in three configurations: manual, semi-automatic, and fully automatic. The printing equipment may be table mounted, stand alone, or in-line. Many semi-automatic printers offer manual vision alignment capability, while fully automatic printers offer automatic vision alignment capability.

Pump head is a new method of solder paste transfer, which allows the material to be transferred to a PCB via an independent application force. The system consists of an enclosed print head, which contains the solder paste so that it is never exposed to the atmosphere. During the print stroke paste is pressurized from the top directly onto the stencil. The paste rolls within the head during the print stroke.

Stencils are preferred over screens because of better image accuracy, volume control and longer service life. Screens are not in common use today. Stainless steel is the most common stencil material; other choices include brass, Alloy 42, molybdenum and nickel. Chemical etching is commonly used to fabricate stencils. Laser cutting, electroforming and electropolishing have been developed to aid fine pitch applications. Stepped thickness stencils can be used to vary solder paste thickness, however this method is decreasing in popularity. Aperture micro-modification has become the preferred method for varying solder paste volume. Fine pitch printing requires very accurate alignment of the stencil apertures to the land patterns.

Fiducial targets are common at the printed circuit board (global) level. SMEMA 3.1 "Fiducial Mark Standard" describes a recommended fiducial.
**Placement Machines**

**Turret architecture:**

Typical machine throughputs average around 25,000 CPH and handle components under 20mm in package size. The basic turret style concept of operation remains consistent between all suppliers. Multiple heads are equally positioned around a horizontally rotating drum. A moving feeder carriage positions tape feeders under a single pickup point. The rotation of all heads around the drum results in the simultaneous pick up, inspection, and placement of components. A moving table positions the PCB under the corresponding part placement location. After component placement, the heads are rotated back to the feeder pickup point and the cycle is repeated.

**Gantry architecture:**

Two types of applications use the gantry style architecture. One application of gantry style of machines has been in the area of flexible fine pitch placement. Typical machine throughputs average around 5,000 CPH and handle fine pitch and odd shaped components of varying package sizes. The basic concept of gantry operation uses a fixed feeder and board design. A multi-spindle placement head is mounted to either a single or dual gantry axes. The placement head moves over the desired feeder locations where components are picked. After the components are acquired, the head scans the components over an upward looking vision station. After the components are inspected, they are sequentially placed on the fixed PCB.

**Massively Parallel Architecture:**

Another type of architecture involves the use of parallel processing to achieve high-speed chip placement. This placement style is evident in dedicated high volume applications experiencing low product changeover. Consumer, automotive and telecommunication sectors have successfully implemented the parallel processing approach to chip placement. Typical machine throughputs can exceed 60,000 CPH and handle components under 12mm in package size. The basic concept of operation relies on the cumulative operation of multiple placement modules. Each individual placement module is capable of picking, inspecting, and placing components on a portion of the PCB. The net affect of parallel module operation is high throughput. The drawbacks of this machine architecture include a limited component handling range in addition to lengthy product changeover times.

**Odd Form Placement Machines**

In electronic printed circuit board assembly, Odd-Form components are identified as those through-hole or surface mount components whose height, weight or shape traditionally would not allow them to be automatically placed using standard pick and place assembly machines.

While most of the processes in electronic printed circuit board assembly have seen great advances in automation, odd-form component placement has seen little movement toward automation. It has remained largely a manual process for many reasons, including satisfaction with current methods and a lack of suitable component packaging, feeding, and placement equipment. However several factors have combined to lead electronic manufacturers to take a new look at automating odd-form component assembly. The key factors are: the need for increased production volumes, improved product quality, reduced time to market, lower assembly cost, and increased global competitiveness.

**IC Die Feeding**
Semiconductor chips can be presented to the placement machine in several formats; i.e. pocket type tape and reel, surf tape, matrix trays or waffle packs, wafers. The use of one in particular depends on several factors.

Tape and reel has a very large infrastructure in terms of tape suppliers, feeders, storage racks, etc. It is also easier for industries that need traceability such as the medical industry (implantable pacemakers, defibrillators) or some critical automotive component (air bag sensors, etc.). It is the faster for most applications and does not require too much operator intervention because of the large volumes they contain and the multiple feeder slots or carriers that exist.

Waffle packs or matrix trays are very small, do not take up a lot of space, can be reused and can be grouped or kitted very easily for small jobs. There is more operator intervention since he has to load and unload them more frequently. An automatic waffle pack feeder with a large buffer would be beneficial for the industry. Primarily used for high-end semiconductor chips like microprocessors, ASICS, SRAM and DSP's.

Wafers can be fed directly to the placement machine thus saving the intermediate operation of picking die from wafers and placing them in another medium like tape and reel or waffle packs. They take the most space if you factor in the rings, the cassettes, and the rejected die in the wafer.

**Packaged Component Feeding**

The basic function of a feeder is to prepare/present components for the “pick” sequence of a placement machine. Feeders handle component package formats of carrier tape, tube, bulk cassette, and matrix tray. Typical feeder design is an electro-mechanical sub-assembly integral to machine function, but easily removable from the machine for set-up and component loading. However, dependent on application, in some cases “feeders” become, in effect, an actual pick and place machine.

Tape feeder products are being developed to handle wider carrier tape, (for many placement machine vendors a tape width of 88mm was the maximum). Current feeder products are also being converted/redesigned to expand the pocket depth capability. To providing for more tape inputs on the placement machine, the combination of two carrier tapes, (8mm wide) into one feeder assembly is a viable approach. This design allows for an expansion of tape inputs, while keeping the feeder at a manageable sub-assembly size.

Tube feeders continued use in the industry stems from two main reasons: an inability to purchase/obtain component types packaged in tape, (component geometry or volume related), and tubes offer an inexpensive alternative to carrier tape packaging. Tube feeders are quite often employed on PCB products with small component counts (as low as quantity of one per product in some cases). With these small counts, feeder cycle speed is not an issue, and the manufactures avoid the greater cost associated with tape and reel.

The use of bulk cassette feeders continues to increase. There are a number of benefits to bulk feeding. In some cases a single cassette contains five times more components than a reel of carrier tape. This reduces component cost, due to minimal packaging costs. Bulk cassettes also reduce the costs associated with disposal of scrap carrier tape. Manufacturers must deal with the disposal of scrap carrier tape, scrap cover tape, and in some cases, scrap reels. These waste volumes can be sizable.

Matrix “feeders” represent the greatest variation of the feeder products. On the low-end of the scale, a matrix tray feeder can be as simple as a stationary platform, which precisely locates one matrix tray. As with the tube feeder products, these units are used for small count component situations, (an example; lab environment & test applications). The high-end or sophisticated matrix tray feeders more closely resemble a version of a pick-and-place machine.
Soldering

Soldering continues to be a major concern to the industry. Solder joint evaluation criteria are still not well understood. Traditionally, specifications written by both industry and government have only helped to confuse the issue by trying to evaluate the cosmetics of a solder joint and then attempting to relate the results to solder joint reliability. See section 6.0 for information on this subject.

Surface mount solder joints are of paramount importance because the solder joint is used as a structural member. Solder joint fatigue, for both leaded and leadless components, is not well understood. Detailed experiments are being done to correlate fatigue-testing procedures. Due to lead compliance, the surface mounting of leaded components provides a significant margin of safety over leadless components.

Wave soldering equipment continues to be a viable tool for soldering through-hole and surface mount components in a single operation. Some companies have successfully used drag-soldering equipment for low volume through-hole soldering.

A single bi-direction or uni-direction solder wave is not recommended for surface mount soldering. A dual and/or vibrating wave system is the preferred method. The agitation provided by the dual or vibrating wave dislodges trapped flux gas that forms during wave contact and forces solder into areas with poor wetting angles. Proper component orientation is also very important. Ideally, the wave soldering process should be limited to soldering ceramic surface mount resistors and capacitors. Wave and foam fluxers are generally used to apply flux to the board. Spray fluxers are being used to apply very controlled amounts of flux, especially when no-clean fluxes are used

The wave or drag soldering time/temperature profile is important. There is no industry standard time/temperature profile, however, some common rules can be used: preheat at a rate of 0.5 to 2°C/second, flux active time should range from a minimum of 30 seconds to a maximum of 120 seconds, heat the bottom side components to within 100°C of the solder pot temperature and maintain a solder wave dwell time of 1 to 2 seconds. Profiling is possible, and recommended. Profiling equipment capability has improved considerably in recent years.

Vapor phase, infrared (IR) and forced gas convection are the most widely used reflow soldering methods. Some suppliers utilize IR and natural or forced gas convection in the same system. The current industry trend is towards systems that are convection dominant. In-line hot plate reflow has also been used successfully in some applications.

Due to differences in the material mass, the vapor phase process heats leads and lands non-uniformly, which may cause most of the molten solder to wick up component leads. The effects of the material mass differences are significantly reduced by the use of pre-heaters positioned in front of the vapor phase system. However, vapor phase has the advantage that all components receive the same amount of heat energy and achieve a controlled maximum temperature limit more effectively than with other processes. Although it is a less common approach, vapor phase soldering will not disappear. The process allows a variety of different assemblies to be soldered with minor changes to the setup parameters. The batch vapor phase process remains a popular lab tool due to its flexibility, low cost and small size.

Various solutions, such as preheat and dual alloy solders have been proposed to reduce the wicking problems in vapor phase soldering. These solutions are not needed for IR and forced gas convection reflow because of the slower heat transfer rate. Lamp and panel IR systems were popular for many years. The current trend is towards systems that use forced gas convection. Today there are convection dominant systems heated by IR lamps, IR panels, and strip or coil heaters. Forced gas convection has simplified the profiling process; it is possible to use the same profile for numerous assemblies. However, for IR systems, each assembly may require its own profile to optimize heating characteristics depending on layout, size and thermal mass distribution.

The reflow time/temperature profile is very important. Although no industry standard time/temperature profile has been developed some common rules can be applied: maintain a heating ramp rate of 0.5 to 2°C/second, flux active
time should range from a minimum of 30 seconds to a maximum of 120 seconds, remain above solder liquidus for 30 to 60 seconds, achieve a peak temperature of about 25°C above solder liquidus, and avoid being above the substrate TG for more than 2 minutes. Profiling equipment capability has improved considerably in recent years. Profiling should be done to ensure proper reflow.

Cleaning Alternatives

December 31, 1995 marked the deadline for halting the manufacture of chlorofluorocarbon, CFC-113, methyl chloroform and other ozone depleting substances in the major industrial countries around the world. These solvents were important cleaning materials for removing rosin flux residues during the assembly cleaning process. The primary alternative to these banned chemicals has been semi-aqueous cleaning. This is usually a two-step cleaning process where an organic solvent first dissolves the rosin residues and then an aqueous rinse emulsifies the solvent containing the rosin residues and removes the residual ionic contamination.

Recently, three solvent cleaning options have been introduced which are reported to be drop-in replacements for CFC-113 stabilized methyl alcohol azeotrope. These include a hydrochlorofluorocarbon (HCFC) from Asahi Glass, a hydrofluorocarbon (HFC) from Dupont and hydrofluoroether (HFE) from 3M.

The Asahi Glass solvent AK-225 AES is an azeotrope of HCFC-225ca and HCFC-225cb with ethyl alcohol and a stabilizer. The material has a boiling point of 52 °C as compared with the CFC alcohol azeotrope, which boils at 46.5 °C. It has an ozone depletion potential of 0.03 and an operator exposure limit (AEL) of 50-PPM 8-hour time weighted average.

Dupont’s HFC solvent is named Vertrel® XM and contains an azeotrope of the HFC with methyl alcohol. Its properties are similar to the CFC-113/alcohol azeotrope with a boiling temperature of 48 °C. Since it does not contain chlorine or bromine in the HFC the ozone depleting potential is 0.0. Both of these solvents can be used in the present vapor degreasers.

A third solvent, developed by 3M, involves a co-solvent process in which the cleaning solvent and the rinse solvent are significantly different in composition. The hydrocarbon solvent used in the cleaning step is Solvating Agent-24 (a blend of monobasic ester and glycol ether derivatives supplied by Petroferm) and it is contained as a 50% v/v with the fluoroether HF-7100 (C₄F₉OCH₃). The rinse solvent is pure HF-7100, which has a boiling temperature of 60 °C and a zero ozone depleting potential.

![Figure 6-1](Properties of Cleaning Solvents)

### Figure 6-1

Properties of Cleaning Solvents

<table>
<thead>
<tr>
<th></th>
<th>CFC-113/MeOH</th>
<th>AK225 AES</th>
<th>Vertrel XM</th>
<th>3M - HFE</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP (°C)</td>
<td>46.5</td>
<td>52</td>
<td>48</td>
<td>60</td>
</tr>
<tr>
<td>Liquid Density (g/cm³)</td>
<td>1.51</td>
<td>1.49</td>
<td>1.49</td>
<td>1.50</td>
</tr>
<tr>
<td>Surface Tension</td>
<td>18.5</td>
<td>16.8</td>
<td>14.1</td>
<td>13.6</td>
</tr>
<tr>
<td>F.P. (°C)</td>
<td>-41.8</td>
<td>-138</td>
<td>&lt;-80</td>
<td>-135</td>
</tr>
<tr>
<td>ΔH_vap (cal/g)</td>
<td>42.9</td>
<td>40.6</td>
<td>43</td>
<td>30</td>
</tr>
<tr>
<td>Viscosity (cPs)</td>
<td>0.66</td>
<td>0.61</td>
<td>0.63</td>
<td>0.61</td>
</tr>
<tr>
<td>ODP</td>
<td>0.8</td>
<td>0.03</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Underfill Dispense and Curing

Underfill dispense and curing requires a significant portion of the overall SMT assembly processing time. Recent developmental emphasis has been to reduce both the wicking time of the capillary flow underfill and the time
required for its curing. In addition, the size of flip chip die and packaged parts has increased while the attachment bump or solder site has decreased in pitch yielding a device with shorter stand-off heights yet larger surface area beneath the device.

Substrates are typically pre-baked to remove surface moisture from the substrate and underside of the SMT packages. The prebake temperature is generally equal to the curing temperature.

The capillary underfill is applied to one edge of a flip chip or packaged part using a precision dispensing system. The dispense system, using optical recognition, must be capable of placing the dispense needle at a controlled distance from the SMT device and a controlled height from the substrate. The dispense pump must be capable of providing a controlled dispense rate of material as the needle is moved along the edge of the die. Multiple passes along one edge of the device may be required for large slow wicking devices.

The underfill is then allowed sufficient time to wick into the gap between the device and the substrate by capillary action. Substrates and underfill can be heated to reduce the viscosity of the underfill and increase the flow rate. Void formation beneath the device and underfill gelling limit the wicking temperature. Caution must be exercised to reduce any incidence of underfill voiding beneath the device. A fillet dispense pass is conducted on the remaining three sides. This additional material forms a uniform concave edge fillet around the perimeter of the device.

The substrate with underfilled devices is then placed into a curing oven with a set temperature and time of cure as recommended by the underfill manufacturer. Multiple stage or controlled rate curing can be used for reducing the level of stress caused by the curing process. A nitrogen purge oven, for batch or continuous line curing, is typically employed.

**Repair**

Generally speaking, repairs are changes to an unacceptable end product to make it acceptable in accordance with the original functional requirements. Modifications, rework, and repair of the interconnecting substrate or the assembly are no substitute for proper fabrication, assembly, and quality control techniques. Nonetheless, defects do occur.

IPC-7711 "Rework of Electronic Assemblies" and IPC-7721 "Repair and Modification of Printed Boards and Electronic Assemblies" detail techniques for modification, rework, or repair of printed boards and assemblies. IPC-7711 focuses on removal and replacement of surface mount components, through-hole components, and coatings. IPC-7721 addresses repair of printed boards, including base material, lifted pads and conductors, damaged pads and lands, edge contacts, plated holes, and other board conditions such as blisters, delamination, bow and twist. The documents provide detailed procedures, tools and techniques, and evaluation criteria.

A component rework operation may consist of some or all of the following steps:

1. Reflow and removal of the component:
   Small surface mount components, e.g. discrete passives, are typically removed using manual solder tools such as soldering irons and tweezers. More complex SMT components are usually removed using automated or semi-automated repair equipment, most of which employ hot gas as the means of delivering heat to the component site. Through hole components are removed using either a solder sucker or a solder fountain.

2. Site cleaning, to remove excess solder:
   For surface mount components, site cleaning is typically performed using a soldering iron and fluxed solder wick or by using a solder sucker??. For through-hole components, excess solder blocking the holes is generally removed using a solder sucker.

3. Solder replenishment, to provide sufficient solder for the creation of new solder joints:
A variety of methods are available, including: solid solder wire, solid solder preforms, solder paste (dispensed or screened), liquid solder, e.g. in a solder fountain. In many cases, the solder is replenished during the placement and reflow of the new component.

4. Placement and reflow of the new component:
   Replacement methods and tools are usually the same as those used in removal: manual tools for small SMT components, automated or semi-automated hot gas repair machines for more complex SMT components, and manual tools or solder fountain for through-hole components.

5. Cleaning
   If the flux used requires cleaning, it can be performed using the production cleaning equipment, or using an off-line batch cleaner.

Solder joints may also be touched up without removing the original component. This is typically performed manually using a soldering iron and flux-cored solder wire, and would be used to repair exposed solder joints with bridges, opens, or other solder defects.

Substrate repairs are generally applied only when the total assembly is at stake and the economics of time, labor, material and procedure limitations are weighed against outright replacement.

Some challenges in component rework include:

1. Dense board layouts
   Increased component densities on printed boards lead to ever decreasing component spacing. The ability to successfully rework a component without damaging or reflowing neighboring components is impacted by component spacing.

2. New package types that are inherently non-standard in their thermal properties
   Traditional leadframe SMT packages can typically be set up once, and the same process and equipment settings used on any new part number that follows the same mechanical package standard. In contrast, a process set up for an array package that meets a standard mechanical outline cannot usually be applied without modification to a new part number which meets the same mechanical outline standard. This significantly increases the time required to continually set up new part numbers.

3. Rework on thick, multi-planed printed boards
   Adequately heating a localized area for repair on a high thermal mass printed board may require heating of the entire assembly prior to and during the repair operation. Long repair heating cycles may also be required in order to achieve localized reflow.

4. Increased board sizes
   Increased board sizes challenge the limitations on hot gas rework equipment. The bottom heaters on these equipment must be large enough and provide uniform heating within its area to the printed board during rework.

**Process Control**

Some level of process control is recommended for each assembly process. Process control is the strategy that relates product specifications to process capability and process repeatability. To control the process, one must understand the assembly process and how each variable contributes to product quality. Process control requires a stable process that is performed exactly the same way each time it is done.

Currently, the goal is to establish and maintain at least a 3-sigma process capability, the future goal is to establish and maintain a 6-sigma process capability. A common mistake involves the use of statistical process control (SPC). The common myth: gathering and displaying statistical data is process control. SPC is one of the tools used to help evaluate processes and keep them in control. Process control is a combination of product specifications, process capability, process standardization, and data collection (SPC) and failure analysis.
In any process control program, all members of the organization play an important role. Management must understand and support process control and continuous improvement, promoting the appropriate training at all levels.

For guidance reference IPC-PC-90 "General Requirements for Implementation of Statistical Process Control" which provides guidelines for implementing process control and takes the reader from present quality conformance techniques to process parameter techniques. Also reference section 6.

Successful products are designed to be monitored and tested. The industry still relies too much on visual inspection of solder joints to determine solder joint quality. Visual inspection is inadequate. Even the best-trained inspector can inspect the same assembly several times and note different defects each time.

Automated optical inspection (AOI) is an evolving technology. Currently, AOI suppliers are focusing on three areas: inspection after solder paste printing, inspection after component placement, and inspection after reflow soldering. Currently, automated inspection is capital intensive. Suppliers are developing improved, lower cost AOI inspection tools. AOI and electrical test equipment should be used to determine process capability and as a process control tool. They should never be used to simply inspect product.

Electrical testing is used to evaluate the functionality of the electronic assembly. There are two commonly used electrical test approaches: In-circuit Test (ICT) and Functional Test (FT). ICT is used to detect faults caused by the manufacturing process and also to isolate the majority of bad components. The fault spectrums for ICT include solder bridge, solder joint open, component misorientation, wrong component, and conductor short. FT is used to detect device faults on the assembly at speed. A new approach is to place an in-circuit tester at the end of the assembly line and use it as a manufacturing defect analyzer (MDA). Each product is tested immediately after assembly. Problems are relayed quickly back to manufacturing so corrective action can be taken while like product is being assembled.

**Systems Approach**

To achieve optimum assembly yields and quality, the capability and interaction of all surface mount manufacturing processes must be completely understood. All elements of the process and the equipment contribute to the success (or failure) of producing quality products. The manufacturing equipment, usually from multiple suppliers, must be molded into an integrated system with adequate process controls. The Surface Mount Equipment Manufacturers Association (SMEMA) has suggested standards for mechanical, electrical, and software/communication interfaces between equipment in an assembly line. However, an industry wide standard for software networking does not currently exist. This is one of our future challenges.
SECTION 7
Acceptance Criteria

Acceptance criteria is concerned with the "end point" in the assembly process. Definition of that end point is dependent on what is the intended use environment of the assembly. However, certain issues are common for any type of assembly.

This section will deal with the training, materials, and metrics of acceptance criteria, levels and methods of inspection for determination if the metrics applicable to the product are being met, and finally, how to assure long term product reliability.

7.1 Training and Acceptance Metrics

But how does one implement a process, either manual or automated, that will determine if the assemblies being produced meet the criteria for acceptance? For any inspection process the accuracy of the results of that process will depend on the level of training and commitment of the users of that process. The best place to start is training. And the training depends on the metrics used as acceptance criteria.

The most widely used metrics for assemblies are the documents ANSI/IPC-A-610, "Acceptability of Electronic Assemblies" and IPC J-STD-001, "Requirements for Soldered Electrical and Electronic Assemblies". Both these standards deal with materials, methods, and criteria for assessment of electrical and electronic assemblies. In addition both these documents provide information on process control that allows quality and acceptability issues to be moved "up-stream" from final inspection.

To make these standards working documents training is available from a large number of IPC/ANSI certified training centers. Twelve centers in the United States and Europe are available to provide training in J-STD-001. Fifteen centers in Europe, Asia, and the United States are available to provide training in ANSI/IPC-A-610. Certification of instructors in the methods of teaching the criteria contained in these documents is also available. For a complete listing of training centers, copies of the documents themselves, manual aids for shop floor use of the documents, or information on certification contact the IPC. (http://www.ipc.org)

7.2 Levels of Inspection

The proceeding section covers standards available for acceptance criteria. On the assembly floor there are several levels of inspection that can be applied. Each of these levels can be restricted in their scope to end point acceptance criteria. Or these methods can be applied within the assembly process to facilitate process control.

For trained instructors visual inspection can be used to determine the level of product conformance to the end-point requirements of the 001 and 610 documents. Visual inspection can also be used as a process control method. For example, noting product non-conformity in solder quality (through application of the 001 or 610 criteria) prior to final assembly can provide process control feedback to the placement and solder paste application. While the solder inspection is being applied other process control data such as mis-oriented or missing parts may be collected. This process control data may include information on solder paste deposition quality.

The manual operation of inspection can be supplemented with Automated Optical Inspection (AOI). AOI can provide quick checks of such things as polarity markings, misalignment of parts, or missing parts. As noted above for manual inspection this information can be used at the end of the line or during the assembly process. In the latter case the data collected can be used for process control.

In circuit test (ICT) provides the next level of measurement. Electrical test through probing can determine such problems as defective parts, incorrect parts, shorts and opens in the interconnections, and physical defects. ICT
can function as a measure of product quality and thus determine acceptability. Or, if done before final assembly, the data collected can be use for process control/corrections.

ICT can be supplemented by a complete functional test at the end of assembly. This test for product functionality can, depending on type of product and the acceptability requirements, be as simple as a "go/no-go" test or as complex as a complete exercising of all circuit functionality.

A non-visual and non-electrical test method for acceptance is X-ray analysis. X-rays can provide information on product workmanship and acceptability. Defects such as poor solder quality, solder balls, and shorts can be detected.

### 7.3 Design for Reliability

Inspection should only be part of the whole process of assuring product quality. Inspection represents a check on the quality. If misused it can be only an after thought on product acceptance. To avoid this misuse, assurance of product quality and acceptability should be have begun at the earliest stages of the products life, i.e. in the design phase.

For surface mount, fine pitch, and chip scale assemblies to meet their user expectations, adequate reliability needs to be designed into the product. This "Design for Reliability" needs to have considered the solder attachments, the package types, and the thermal capabilities of all the components in the assembly, taking into account:

1) The physical design parameters
2) Design lifetime
3) Mechanical and thermal-mechanical history from manufacture to the end of the design life
4) The acceptable failure probability

### 7.4 Solder Joint Reliability Test

The electronics industry uses many test methods, but the most common are powered functional cycling, pre-assembly package qualification, thermal cycling, and mechanical cycling. Which test method should be chosen for qualifying the solder reliability of the joints? Choose a test method that closely resembles the field application. This gives the most representative results. The functional cyclic test on a product resembles operating conditions best.

To test solder joint reliability, various types of thermal cycles and different dwell times and temperatures have been used. The IPC document IPC-SM-785, "Guidelines for Accelerated Surface Mount Attachment Reliability Testing” gives comprehensive guidelines for accelerated reliability testing. Table 6-1 shows the accelerated testing criteria to verify the reliability of solder joints relative to the worst case environments. This table also identifies the typical number of cycles per any given service year, as well as the number of equivalent test cycles required for two different service lives.

Accelerated reliability tests should be carried out with daisy chained prototype assemblies. Daisy chains need to be continuously monitored during the testing to detect solder joint failures when they occur.

From these reliability tests, can we predict the field performance of the product accurately? Yes, but the inherent limitations of accelerated testing as well as the high sensitivity with regards to some of the parameters needs to be understood.
### Table 7-1

Worst-Case Use Environments for Surface Mounted Electronics and Recommended Accelerated Testing for Surface Mount Solder Attachments by Most Common Use Categories

(The actual thermal environments in use need to be established by thermal analysis or measurement)

<table>
<thead>
<tr>
<th>Use Category</th>
<th>Tmin °C</th>
<th>Tmax °C</th>
<th>ΔT°C</th>
<th>t₀ hrs</th>
<th>Cycles/ year</th>
<th>Typical Years of Service</th>
<th>Approx. Accept.</th>
<th>Failure Risk, %</th>
<th>Tmin °C</th>
<th>Tmax °C</th>
<th>ΔT°C(2) °C</th>
<th>t₀ min</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)Consumer</td>
<td>0</td>
<td>+60</td>
<td>35</td>
<td>12</td>
<td>365</td>
<td>1-3</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2)Computers</td>
<td>+15</td>
<td>+60</td>
<td>20</td>
<td>2</td>
<td>1460</td>
<td>5</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3)Telecom</td>
<td>-40</td>
<td>+85</td>
<td>35</td>
<td>12</td>
<td>365</td>
<td>7-20</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4)Commercial Aircraft</td>
<td>-55</td>
<td>+95</td>
<td>20</td>
<td>12</td>
<td>365</td>
<td>20</td>
<td>0.001</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5)Industrial &amp; Automotive Passenger Compartment</td>
<td>-55</td>
<td>+95</td>
<td>20</td>
<td>12</td>
<td>365</td>
<td>10</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6)Military Ground &amp; Ship</td>
<td>-55</td>
<td>+95</td>
<td>40</td>
<td>12</td>
<td>365</td>
<td>10</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7)Space leo</td>
<td>-55</td>
<td>+95</td>
<td>3</td>
<td>12</td>
<td>365</td>
<td>5-30</td>
<td>0.001</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8)Military Avionics</td>
<td>-55</td>
<td>+95</td>
<td>40</td>
<td>12</td>
<td>365</td>
<td>10</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9)Automotive Under Hood</td>
<td>-55</td>
<td>+125</td>
<td>60</td>
<td>12</td>
<td>365</td>
<td>5</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ΔT = in addition

1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT is not the difference between the possible minimum, Tₘᵦ and maximum, Tₘᵦ, operational temperature extremes; ΔT is typically significantly less.

2) All accelerated test cycles shall have temperature ramps, 20°C/minute and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~24 test cycles/day.

3) The failure/damage mechanism for solder changes at lower temperature; for assemblies seeing significant cold environment operations, additional “COLD” cycling, from perhaps -40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the “COLD” °C operational cycles in actual use is recommended.

4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain -20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate “LARGE ΔT” testing with cycles similar in nature and number to actual use is recommended.

### 7.5 Environmental Test Procedures

For designs, which easily meet the reliability requirements during the "Design for Reliability," it is not necessary to perform accelerated testing. However, for severe use conditions beyond the applicability of the design models as well as for designs barely meeting reliability requirements, accelerated testing is indicated.

Various companies and government agencies have instituted test procedures, which simulate the product field environment. Sometimes these stresses are properly applied, sometimes not. Even when a set of tests appears to
effectively sort good product from bad, there is still the problem of determining how damaging the procedure is to
good products.

It should be recognized that environmental testing of product could reduce the reliability of surface mount solder
attachment. Cases have been reported where surface mount solder attachments were systematically destroyed
during ill-advised environmental test procedures.

As discussed in IPC-SM-785, the validity of thermal shock tests to predict the life of surface mount solder joints
has been questioned. Many of today's use environments have not been adequately characterized.

Furthermore, present surface mount manufacturing environments may be the worst environment that the
components or assemblies will ever see. Nevertheless, the products must be capable of withstanding their intended
use environments after experiencing the manufacturing environment.

Environmental test procedures fall into 2 broad categories, each serving a substantially different purpose: Burn-In
and Environmental Stress Screening (ESS).

Burn-In should be an operational test of the assembly at the limits of realistic applicability to assure that random
defects affecting operation did not occur during manufacture.

ESS is a screening procedure to screen from the product population, assemblies with suspected manufacturing
defects of a specific nature. These ESS procedures need to be effective in causing the failure of these latent defects
in order to detect them, but at the same time, cannot substantially damage previously good product. The most
effective ESS procedures frequently bear little resemblance to product conditions.

Recognizing that a matrix was needed to determine the exact requirements and the testing necessary for
performance of various equipment, the Surface Mount Council has developed the following "Product Categories
and Use Environments." Table 6-2 attempts to relate seven product categories by typical application to the
thermal, mechanical, atmospheric, and electrical performance requirements that they must meet during typical
manufacturing processes, storage, and during operation.
<table>
<thead>
<tr>
<th>Product Category</th>
<th>Typical applications</th>
<th>Temperature, C</th>
<th>Mechanical</th>
<th>Atmospheric</th>
<th>Electrical</th>
</tr>
</thead>
<tbody>
<tr>
<td>II (Computers and Peripherals)</td>
<td></td>
<td>25/260</td>
<td>-40/85</td>
<td>0/55</td>
<td>Robust. (term) Th. Shock solder</td>
</tr>
<tr>
<td>III (Communications)</td>
<td></td>
<td>25/260</td>
<td>-40/85</td>
<td>0/55</td>
<td>Robust. (term) Th. Shock solder</td>
</tr>
<tr>
<td>IV (Industrial and transportation passenger compartment)</td>
<td></td>
<td>25/260</td>
<td>-55/85</td>
<td>40/85</td>
<td>Robust. (term) Th. Shock solder</td>
</tr>
<tr>
<td>V (Military, ground and shipboard, low altitude commercial aircraft)</td>
<td></td>
<td>25/260</td>
<td>-40/85</td>
<td>0/55</td>
<td>Robust. (term) Th. Shock solder</td>
</tr>
<tr>
<td>VI (Transportation under hood)</td>
<td></td>
<td>25/260</td>
<td>-55/125</td>
<td>0.32</td>
<td></td>
</tr>
<tr>
<td>VII (Military and space, high altitude commercial aircraft)</td>
<td></td>
<td>25/260</td>
<td>-40/85</td>
<td>0/55</td>
<td>Robust. (term) Th. Shock solder</td>
</tr>
</tbody>
</table>

**Table 7-2 Product Categories and Use Environments**
The Surface Mount Council (SMC) has been around for over twelve years and has had a significant influence on the Surface Mount industry. Many of its efforts have gone unnoticed by the general public because our role is one of influencing standards and trade organizations to perform a service that benefits the entire surface mount industry.

Now that the surface mount industry has matured, we thought it prudent that we ask ourselves if we should disband now that some of the reasons for our original creation have diminished. This would have been relatively easy to do since most if not all of our members already spend an inordinate amount of time traveling to various meetings. In addition our families would have been grateful since usually one of our meeting days is on a Saturday. After considerable deliberation we decided to remain in existence and expand our scope to include other advanced electronic packaging technologies coming on to the scene.

The Surface Mount Council is made up of key industry representatives dedicated to promoting the use of surface mount and advanced electronic packaging technology in the design and production of electronic hardware.

Council Members represent user, supplier and equipment manufacturing companies engaged in surface mount implementation for automotive, telecommunication, computer, instrument, government, consumer, and medical electronics.

The mission of this council is to facilitate, coordinate, and promote the orderly implementation of surface mount technology through standardization, the development of technical documents, and other means.

On an annual basis the Council publishes the "Status of the Technology: Industry Activities and Action Plan" which establishes key objectives, milestones, and accomplishments as a benefit to the electronics industry. The IPC, the EIA, and the SMTA jointly sponsor the Surface Mount Council.

One of the first things we attempted under our new mission statement was to perform a constructive review of the various industry roadmaps. This effort which was called: “Vision 2010 began in September 1997 and began with an open workshop that as held at Georgia Institute of Technology in February 1998. Invitees to this workshop were all of the affiliate members of the SMC and other interested individuals. The first results of the Vision 2010 were presented at SMI 1998.

One of the hot topics currently being monitored by the SMC is the status of the global drive toward lead free electronics assembly that is being driven by the European Community much to the chagrin of many large companies.

For the past several years the premier surface mount symposium and trade show was Surface Mount International which was held annually in San Jose California.

Shortly after last year’s show the founding partners for SMI decided to split up and the Surface Mount Technology Association (SMTA) agreed to carry on with a new show in San Jose which is now called SMTAI.

To help fill a perceived void in Symposia IPC – Association Connecting Electronics Industries has started a new symposium and trade show that is called APEX 2000. This show will be devoted to electronics manufacturing. It will be held in Long Beach during the week of 13 March 2000.

The SMC has agreed to try and participate in both the SMTAI and the APEX 2000 trade shows because they are the premier shows in our industry. The SMC is always looking for new opportunities and working to identify emerging technologies to help enable the Surface Mount Industry for the future.
## APPENDIX
### SUMMARY OF KEY COMPONENT, MATERIAL, PROCESS AND DESIGN STANDARDS

The following documents center on surface mount technology. These documents have been developed by standards organizations in the U.S. and internationally. The letters of each document indicate the organization that has responsibility for the document:

- **EIA** represents documents prepared by the Electronic Components, Assemblies, Equipment & Supplies Association (ECA) of the Electronic Industries Alliance
- **JEDEC** represents documents of the Solid State Technology Association of the Electronic Industries Alliance
- **IPC** represents documents prepared by the IPC – Association Connecting Electronics Industries
- **MIL** represents documents prepared by the Military
- **DoD** represents documents prepared by the Department of Defense
- **J-STD** Joint Industry Standards (more than one association)

### Surface Mount Council Publications
- **SMC-TR-001** An Introduction to Tape Automated Bonding Fine Pitch Technology
- **SMC-WP-001** Soldering Capability
- **SMC-WP-002** An Assessment of the Use of Lead in Electronic Assemblies
- **SMC-WP-003** Chip Mounting Technology
- **SMC-WP-004** Design for Excellence
- **SMC-WP-005** PWB Surface Finishes

### Components, General
- **EIA-625** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- **EIA-886-E** Standard Test Methods for Passive Electronic Component Parts - General Instructions and Index
- **EIA-481** A Taping of Surface Mount Components for Automatic Placement
- **EIA/IS-47** Contact Termination Finish Standard for Surface Mount Devices

1999 Status and Action Plan
EIA-PDP-100  Registered and Standard Mechanical Outlines for Electronic Parts
EIA-JEP-95  JEDEC Registered and Standard Mechanical Outlines for Semiconductor Devices
EIA-JESD30  Descriptive Designation System for Semiconductor Device Packages
EIA-JESD95-1 Design Requirements for Outlines of solid-state and Related Products
IPC-9501  Component Qualification for the Assembly Process
IPC-9502  PWB Assembly Soldering Process Guideline for Electronic Components
IPC-9503  Moisture Sensitivity Classification for Non-IC Components
IPC-9504  Assembly Process Simulation for Evaluation of Non-IC Components (Preconditioning Non-IC) Components
JEDEC Pub 124 Guidelines for the Packing, Handling, and Repacking of Moisture-Sensitive Components

**Components, Passive**

**Capacitors:**

EIA-198-D  Ceramic Dielectric Capacitors Classes I, II, III, and IV
EIA-469-B  Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors
EIA-479  Film-Paper, Film Dielectric Capacitors for Microwave Ovens
EIA-510  Standard Test Method for Destructive Physical Analysis of Industrial Grade Ceramic Monolithic Capacitors
EIA-535  Series of Detail Specifications on Fixed Tantalum Capacitors that have been adopted by the National Electronic Components Quality (NECQ) Assessment System.
EIA-595  Visual and mechanical inspection of multilayer ceramic chip capacitors
EIA-CB-11  Guidelines for the Surface Mounting of Multilayer Ceramic Chip Capacitors
EIA/IS-28  Fixed Tantalum Chip Capacitor Style 1 Protected - Standard Capacitance Range
EIA/IS-29  Fixed Tantalum Chip Capacitor Style 1 Protected - Extended Capacitance Range
EIA/IS-35  Two-Pin Dual In-Line Capacitors
EIA/IS-36  Chip Capacitors, Multi-Layer (Ceramic Dielectric)
EIA/IS-37  Multiple Layer High Voltage Capacitors (Radial Lead Chip Capacitors)
EIA/IS-717  Surface mount tantalum capacitor qualification specification
IEC-384-3  Sectional Specification, Tantalum Chip Capacitors
IEC-384-10 Sectional Specification, Fixed Multilayer Ceramic Chip Capacitors
IECQ Draft  Blank Detail Specification, Fixed Multilayer Ceramic Chip Capacitors
IECQ-PQC-31 Sectional Specification, Fixed Tantalum Chip Capacitors with Solid Electrolyte
IECQ-PQC-32 Blank Detail Specification, Fixed Tantalum Chip Capacitor

**Resistors:**

EIA-575  Resistors, Rectangular, Surface Mount, General Purpose
EIA-576  Resistors, Rectangular, Surface Mount, Precision
EIA/IS-34  Leaded Surface Mount Resistor Networks Fixed Film

**Components, Active**

EIA-JEP-95  JEDEC Registered and Standard Outlines for Semiconductor Devices
EIA-JESD11 Chip Carrier Pinouts Standardized for CMOS 4000, HC, and HCT Series of Logic Circuits
EIA-JESD21-C Configurations for Solid State Memories
EIA-JESD22-B Test Methods and Procedures for Solid State Devices Used in Transportation/Automotive Applications (Series format -- Consists of over 16 different test procedure documents.)
EIA-JESD-26A General Requirements, PEM, Rugged Environments
EIA-JESD30 Descriptive Designation System for Semiconductor Device Packages
EIA-JESD95-1 Design Requirements for Outlines of solid-state and Related Products
IPC/JEDEC J-STD-020A Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuits Surface Mount Devices
IPC/JEDEC-033 Standard for Handling, Packing, Shipping and Use of Moisture Reflow Sensitive Surface Mount Devices
JEDEC Pub 124 Guidelines for the Packing, Handling, and Repacking of Moisture-Sensitive Components
**Components, Electromechanical**

**Connectors:**

- **EIA-364-C** Electrical Connector Test Procedures Including Environmental Classifications (Series format consisting of over 60 Electrical Connector test procedures.)
- **EIA-506** Dimensional and Functional Characteristics Defining Sockets for Leadless Type A Chip Carriers (.050 Spacing)
- **EIA-507** Dimensional Characteristics Defining Edge Clips for Use with Hybrid and Chip Carriers
- **EIA/IS-47** Contact Termination Finish Standard for Surface Mount Devices
- **EIA/IS-64** Two Millimeter, two-part Connectors for Use with Printed Boards and Backplanes
- **IPC-CI-408** Design and Application Guidelines for the use of Solderless Surface Mount Connectors

**Sockets:**

- **EIA-5400000** Generic Specification for Sockets for Integrated Circuit (IC) Packages for Use in Electronic Equipment (Series format with over 20 Sectional, Blank Detail & Detail Specifications, approved for use in the NECQ System.)
- **EIA-540H000** Sectional specification for burn-in sockets used with ball grid array devices for use in electronic equipment

**Switches:**

- **IECQ-PQC-41** Detail Specification, Dual-in-Line Switch, Surface Mountable, Slide Actuated US0003
- **EIA-448-23** Surface Mountable Switches, Qualification Test
- **EIA-5200000-A** Generic Specification for Special-Use Electromechanical Switches of Certified Quality (Series format with over 25 Sectional, Blank Detail & Detail Specifications, approved for use in the NECQ System.)

**Printed Boards:**

- **IPC-6011** General Performance Requirements for Printed Boards
- **IPC-6012** Performance Specification for Rigid Printed Boards
- **IPC-6013** Performance Specification for Flexible Printed Boards
- **IPC-6105** Performance Specification for Organic Multichip Module Structures (MCM-L)
MIL-PRF-31032  Printed Circuit Board/ Printed Wiring Board Manufacturing, General Specification For
MIL-P-50884  Military Specification Printed Wiring, Flexible, and Rigid Flex

**Materials:**

IPC-4101  Laminate/Prepreg Materials standard for Printed Boards
IPC-CF-148  Resin Coated Metal for Multilayer Printed Boards
IPC-3406  Guidelines for Electrically Conductive Surface Mount Adhesive
IPC-3408  General Requirements for Anisotropically Conductive Adhesive Films
IPC-3407  General Requirements for Isotropically Conductive Adhesives
IPC-CF-152A  Metallic Foil Specification for Copper/Invar/Copper (CIC) for Printed Wiring and Other Related Applications
IPC-SM-817  General Requirements for SMT Adhesives
IPC-CC-830  Qualification and Performance of Electrical Insulation Compounds for Printed Board Assemblies
IPC-SM-840C  Qualification and Performance of Permanent Solder Mask for Printed Boards
J-STD-004  Requirements for Soldering Fluxes
J-STD-005  General Requirements and Test Methods for Electronic Grade Solder Paste
IPC-STD(P116)  Qualification and Performance of Flip Chip Underfill Materials

**Design Activities**

IPC-D-279  Reliability Design Guidelines for Surface Mount Technology Printed Board Assemblies
IPC-D-317  Design Standard for Electronic Packaging Utilizing High Speed Techniques
IPC-C-406  Design and Application Guidelines for Surface Mount Connectors
IPC-SM-782A  Surface Mount Land Patterns (Configuration and Design Rules)
IPC-H-855  Hybrid Microcircuit Design Guide
IPC-D-859  Design Standard for Multilayer Hybrid Circuits

1999 Status and Action Plan
IPC-2221  Generic Standard on PWB Design
IPC-2222  Sectional Standard on Rigid PWB Design
IPC-2223  Sectional Design Standard for Flexible Printed Boards
IPC-2225  Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
IPC-(P107) Design Standard for Advanced IC Interconnection Mounting Structures
IPC-(P111) Design Standard for Flip Chip/Chip Scale Assembly Configurations
IPC-STD(P201) Mechanical Outline Standard for Ball Grid Arrays and Other High Density Technology
IPC-(P207) Design Standard for High Density Array or Peripheral Leaded Component Mounting Structures
IPC-(P211) Design Standard for Assembling Array or Peripheral Leaded (BGA, QFP, etc.) Components for Printed Boards and Other Interconnecting Structures.
J-STD-026  Semiconductor Design Standard for Flip Chip Applications
J-STD - (P102) Mechanical Outline Standard for Flip Chip or Chip Scale Configurations
MIL-STD-2118  Design Standard for Flexible Printed Wiring

Component Mounting

EIA-CB-11  Guidelines for the Surface Mounting of Multilayer Ceramic Chip Capacitors
IPC-CM-770D  Guidelines for Printed Board Component Mounting
IPC-SM-784  Guidelines for Direct Chip Attachment
IPC-SM-780  Electronic Component Packaging and Interconnection with Emphasis on Surface Mounting
IPC-MC-790  Guidelines for Multichip Module Technology Utilization
J-STD-012  Implementation of Flip Chip and Chip Scale Technology
J-STD-013  Implementation of Ball Grid Array and other High Density Technology

Soldering and Solderability

EIA/IS-46  Test Procedure for Resistance to Soldering (Vapor Phase Technique) for Surface Mount Devices
EIA/IS-49-A  Solderability Test Method for Leads and Terminations

1999 Status and Action Plan

Appendix
Page 6
EIA-448-19  Method 19 Test Standard for Electromechanical Components Environmental Effects of Machine Soldering Using a Vapor Phase System

EIA-638  Surface Mount Solderability Test

EIA-534  Application Guide Soldering and Solderability Maintenance of Leaded Electronic Components

IPC-TR-460A  Trouble Shooting Checklist for Wave Soldering Printed Wiring Boards

IPC-TR-462  Solderability Evaluation of Printed Boards with Protective Coatings Over Long-term Storage

JESD22  B102B Solderability Test Methods

IPC-TR-464  Accelerated Aging for Solderability Evaluations

J-STD-001  Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002  Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003  Solderability Tests of Printed Boards

IPC-S-816  Troubleshooting for Surface Mount Soldering

IPC-AJ-820  Assembly and Joining Handbook

Quality Assessment

EIA-469-B  Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors

EIA-510  Standard Test Method for Destructive Physical Analysis of Industrial Grade Ceramic Monolithic Capacitors

IPC-A-600E  Acceptability of Printed Boards

IPC-A-610  Acceptability of Printed Board Assemblies

MIL-STD-883  Methods and Procedures for Microelectronics

J-STD-028  Performance Standard for Flip Chip/Chip Scale Bumps

IPC-STD-(P203)  Performance Standard for Ball Grid Array Bumps and Columns

IPC-A-20/21  Stencil Pattern for Solder Paste Slump Test

IPC-A-24  Flux/Board Interaction Board

1999 Status and Action Plan  Appendix Page 7
IPC-A-36  CFC Cleaning Alternatives Artwork
IPC-A-38  Fine Line Round Robin Test Pattern
IPC-A-48  Surface Mount Airforce Mantech Artwork
IPC/JEDEC J-STD-035  Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components

**Surface Mount Process**

IPC-SC-60  Post Solder Solvent Cleaning Handbook
IPC-SA-61  Post Solder Semi Aqueous Cleaning Handbook
IPC-AC-62  Post Solder Aqueous Cleaning Handbook

**Reliability**

IPC-SM-785  Guidelines for Accelerated Surface Mount Attachment Reliability Testing
IPC-D-279  Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

**Numerical Control Standards**

IPC-2511  Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology
IPC-2512  Sectional Requirements for Implementation of Administrative Methods for Manufacturing Data Description
IPC-2513  Sectional Requirements for Implementation of Drawing Methods for Manufacturing Data Description
IPC-2514  Sectional Requirements for Implementation of Printed Board Manufacturing Data Description
IPC-2515  Sectional Requirements for Implementation of Bare Board Product Electrical Testing Data Description
IPC-2516  Sectional Requirements for Implementation of Assembled Board Product Manufacturing Data Description
IPC-2517  Sectional Requirements for Implementation of Assembly Circuit Testing Data Description
IPC-2518  Sectional Requirements for Implementation of Bill of Material Product Data Description
EIA-224-B  Character Code for Numerical Machine Control Perforated Tape

1999 Status and Action Plan
EIA-227-A  One-Inch Perforated Tape
EIA-267-B  Axis and Motion Nomenclature for Numerically Controlled Machines
EIA-274-D  Interchangeable Variable Block Data Format for Positioning, Contouring, and Contouring/Positioning Numerically Controlled Machines
EIA-281-B  Electrical and Construction Standards for Numerical Machine Control
EIA-408  Interface Between Numerical Control Equipment on Data Terminal Equipment Employing Parallel Binary Data Interchange
EIA-431  Electrical Interface Between Numerical Control and Machine Tools
EIA-441  Operator Interface Function of Numerical Controls
EIA-474  Flexible Disk Format for Numerical Control Equipment Information Interchange
EIA-484  Electrical and Mechanical Interface Characteristics and Line Control Protocol Using Communication Control Characters for Serial Data Link Between a Direct Numerical Control System and Numerical Control Equipment Employing Asynchronous Full Duplex Transmission
EIA-494  32 BIT Binary CL Exchange (BCL) Input Format for Numerically Controlled Machines

Test Methods
EIA-JEDEC  Method B 105-A, Lead Integrity -- Plastic Leaded Chip Carrier (PLCC) Packages
EIA-JEDEC  Method B 102, Surface Mount Solderability Test (JESD22-B)
JESD22  Method B 108, Coplanarity (Test for Surface Mount Semiconductor Leads)
J-STD-(P104)  Test Methods for Flip Chip of Chip Scale Products
JEDEC Standard 22 Series, Test Methods

Repair
IPC-7711  Rework of Electronic Assemblies
IPC-7721  Repair and Modification of Printed Boards

1999 Status and Action Plan
Terms and Definitions

IPC-T-50F Terms and Definitions for Interconnecting and Packaging Electronic Circuits

How to Obtain These Documents

Following are the addresses of the IPC and EIA, as well as other sources for documents shown in this SMT listing.

IPC – Association Connecting Electronics Industries
2215 Sanders Rd. #250
Northbrook, IL 60062-6135

ELECTRONIC INDUSTRIES ALLIANCE (EIA)
2500 Wilson Blvd.
Arlington, VA 22201-3834

GLOBAL ENGINEERING DOCUMENTS
2805 McGaw Avenue
Irvine, CA 92713
Phone: 1-800-854-7179

Military documents are available from:

STANDARDIZATION DOCUMENTS
Order Desk, Building 4D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Central office of the IEC:
INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)
3 Rue de Varembe
1211 Geneva 20, Switzerland

IEC documents are available from:
AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)
11 West 42nd Street
New York, NY 10036