IPC/JEDEC-9702
Amendment 1
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Monotonic Bend Characterization of Board-Level Interconnects

A standard developed by IPC

Association Connecting Electronics Industries

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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FOREWORD

This amendment provides a clerical correction to section 8.7, *Test Board Daisy-Chain Links*, which better expresses the intent of the IPC and JEDEC committees to recommend avoiding stress artifacts and to offer strategies to that end.

8.7 Text Board Daisy-Chain Links

4th Paragraph, replace first sentence as follows:

Electrical monitoring traces should be routed so as to avoid the propensity for artifacts of the stress (trace/via cracks). Some strategies may include routing to the long side of the PCB whereby the traces are 45° - 90° from the bend direction or routing on internal PWB layers to reduce the likelihood of external trace contact damage during testing.